

Low Voltage CMOS Hex Schmitt Inverter with 5 V-Tolerant Inputs

MC74LCX14

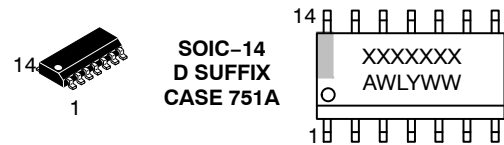
The MC74LCX14 is a high performance hex inverter with Schmitt-Trigger inputs operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers, while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX14 inputs to be safely driven from 5.0 V devices.

Pin configuration and function are the same as the MC74LCX04, but the inputs have hysteresis and, with its Schmitt trigger function, the LCX14 can be used as a line receiver which will receive slow input signals.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 5.0 V Tolerant Inputs – Interface Capability with 5.0 V TTL Logic
- LVTTTL Compatible
- LVC MOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- Current Drive Capability is 24 mA at Source/Sink
- Pin and Function Compatible with Other Standard Logic Families
- ESD Performance: Human Body Model >2000 V
- Chip Complexity: 41 Equivalent Gates
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAMS



XXXXXX = Specific Device Code
 A = Assembly Location
 L, WL = Wafer Lot
 Y, YY = Year
 W, WW = Work Week
 G or ■ = Pb-Free Package
 (Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

MC74LCX14

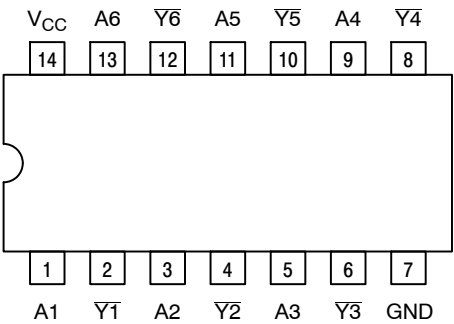


Figure 1. Pinout: 14-Lead (Top View)

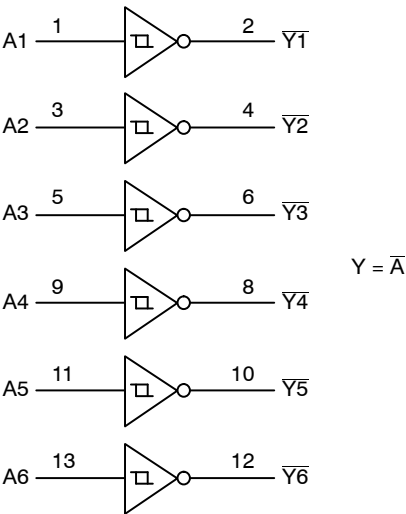


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
A _n	Data Inputs
$\overline{Y}_n$	Outputs

TRUTH TABLE

Inputs	Outputs
A	Y
L	H
H	L

MC74LCX14

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)	-0.5 to +6.5	V
V_O	DC Output Voltage (Note 1) Active-Mode (High or Low State) Tri-State Mode Power-Down Mode ($V_{CC} = 0$ V)	-0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5	V
I_{IK}	DC Input Diode Current $V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_O < GND$	-50	mA
I_O	DC Output Source/Sink Current	± 50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 1) SOIC-14 QFN14 TSSOP-14	116 130 150	°C/W
P_D	Power Dissipation in Still Air at 125°C SOIC-14 QFN14 TSSOP-14	1077 962 833	mW
MSL	Moisture Sensitivity	Level 1	-
F_R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	-
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	3.3	5.5	V
V_I	Digital Input Voltage	0	-	5.5	V
V_O	Output Voltage Active Mode (High or Low State) Tri-State Mode Power Down Mode ($V_{CC} = 0$ V)	0 0 0	- - -	V_{CC} 5.5 5.5	V
T_A	Operating Free-Air Temperature	-40	-	+125	°C
t_r, t_f	Input Transition Rise or Fall Rate	0	-	No Limit	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74LCX14

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		T _A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
V _{T+}	Positive-Input Threshold Voltage		1.65	–	1.4	–	1.4	V
			2.5	0.9	1.7	0.9	1.7	
			3.0	1.2	2.2	1.2	2.2	
			4.5	–	3.1	–	3.1	
			5.5	–	3.6	–	3.6	
V _{T–}	Negative-Input Threshold Voltage		1.65	0.2	–	0.2	–	V
			2.5	0.4	1.1	0.4	1.1	
			3.0	0.6	1.5	0.6	1.5	
			4.5	1	–	1	–	
			5.5	1.2	–	1.2	–	
V _H	Hysteresis Voltage		1.65	0.1	0.9	0.1	0.9	V
			2.5	0.3	1.0	0.3	1.0	
			3.0	0.4	1.2	0.4	1.2	
			4.5	0.6	1.5	0.6	1.5	
			5.5	0.7	1.7	0.7	1.7	
V _{OH}	High-Level Output Voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	V _{CC} – 0.1	–	V _{CC} – 0.1	–	V
		I _{OH} = –100 μA	1.65	1.29	–	1.29	–	
		I _{OH} = –4 mA	2.3	1.8	–	1.8	–	
		I _{OH} = –8 mA	2.7	2.2	–	2.2	–	
		I _{OH} = –12 mA	3.0	2.4	–	2.4	–	
		I _{OH} = –16 mA	3.0	2.2	–	2.2	–	
		I _{OH} = –24 mA	4.5	3.7	–	3.7	–	
V _{OL}	Low-Level Output Voltage	V _I = V _{IH} or V _{IL}	1.65 to 5.5	–	0.1	–	0.1	V
		I _{OL} = 100 μA	1.65	–	0.24	–	0.24	
		I _{OL} = 4 mA	2.3	–	0.3	–	0.3	
		I _{OL} = 8 mA	2.7	–	0.4	–	0.4	
		I _{OL} = 12 mA	3.0	–	0.4	–	0.4	
		I _{OL} = 16 mA	3.0	–	0.55	–	0.55	
		I _{OL} = 24 mA	4.5	–	0.6	–	0.6	
I _I	Input Leakage Current	V _I = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I _{OFF}	Power Off Leakage Current	V _I = 5.5 V or V _O = 5.5 V	0	–	10	–	10	μA
I _{CC}	Quiescent Supply Current	V _I = 5.5 V or GND	3.6	–	10	–	10	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} – 0.6 V	2.3 to 3.6	–	500	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74LCX14

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V _{CC} (V)	T _A = -40°C to +85°C		T _A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	See Figures 3 and 4	1.65 to 1.95	–	15.7	–	15.7	ns
			2.3 to 2.7	1.5	7.8	1.5	7.8	
			2.7	1.5	7.5	1.5	7.5	
			3.0 to 3.6	1.5	6.5	1.5	6.5	
			4.5 to 5.5	–	5.6	–	5.6	
t _{OSSL} , t _{OSLH}	Output to Output Skew		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			4.5 to 5.5	–	–	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = +25°C			Unit
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 5)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		0.8 0.6		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 5)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		–0.8 –0.6		V

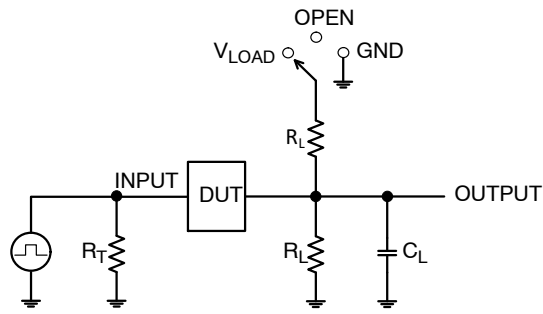
5. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition	Typical (T _A = 25°C)	Unit
C _{IN}	Input Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	25	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

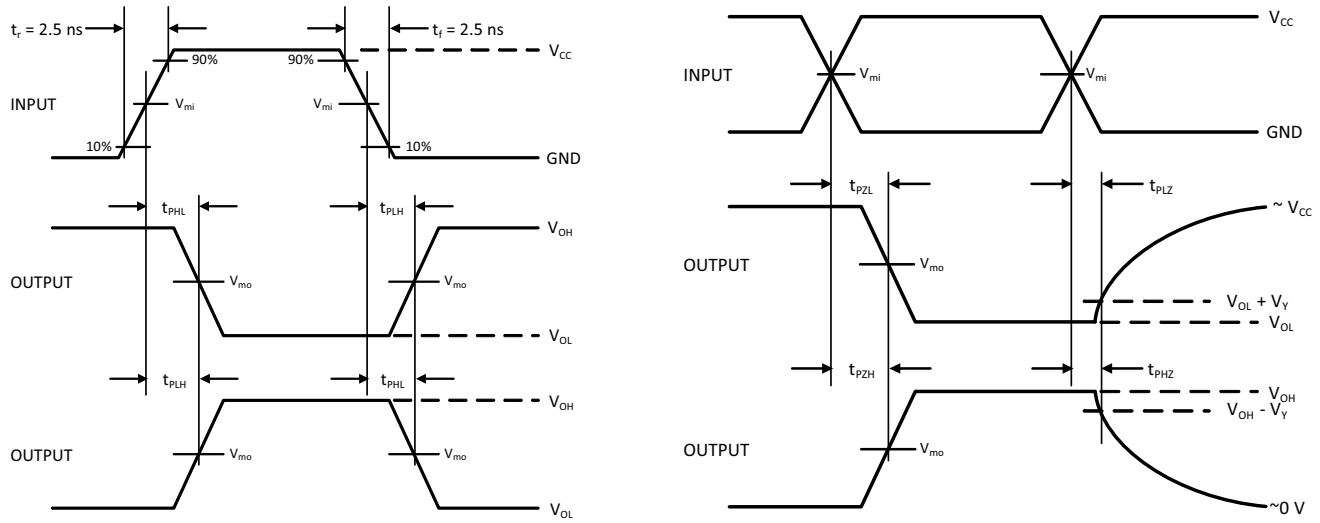
MC74LCX14



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

Figure 3. Test Circuit



V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_m, V	V_Y, V
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	$V_{CC}/2$	0.3

Figure 4. Switching Waveforms

MC74LCX14

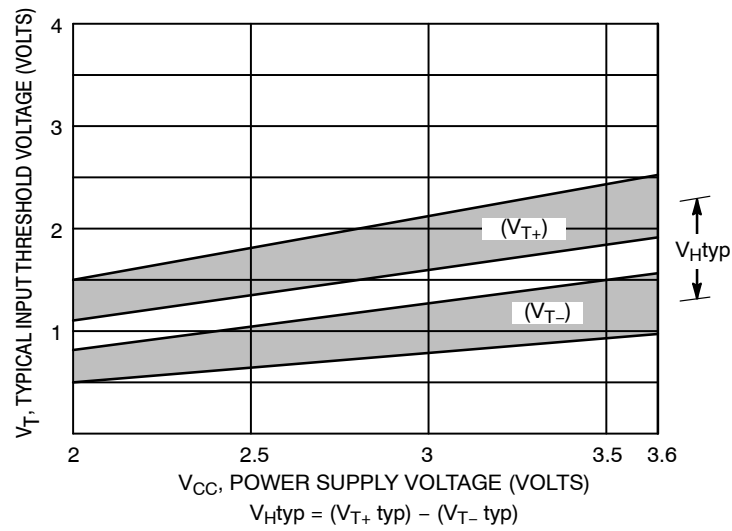
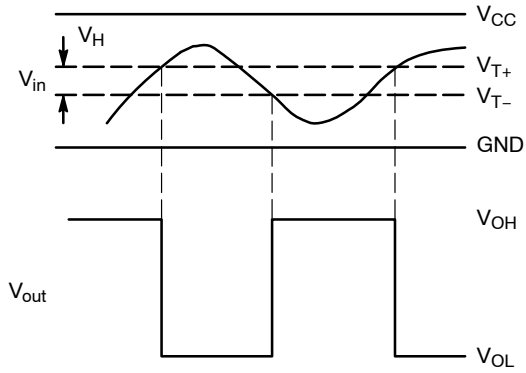


Figure 5. Typical Input Threshold, V_{T+} , V_{T-} versus Power Supply Voltage

(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

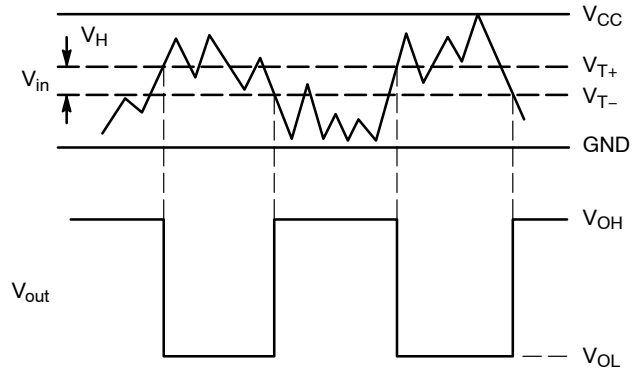


Figure 6. Typical Schmitt-Trigger Applications

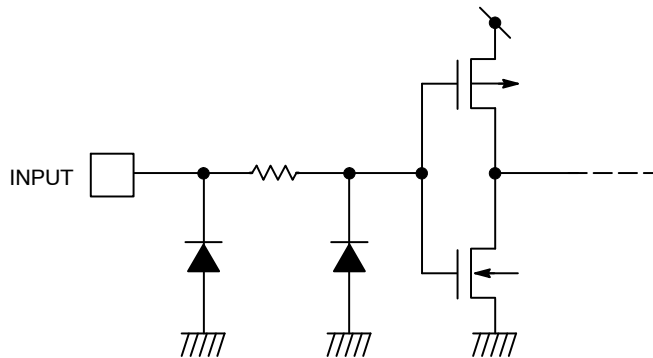


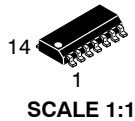
Figure 7. Input Equivalent Circuit

MC74LCX14

ORDERING INFORMATION

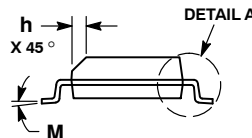
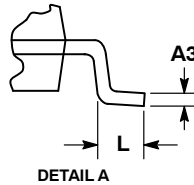
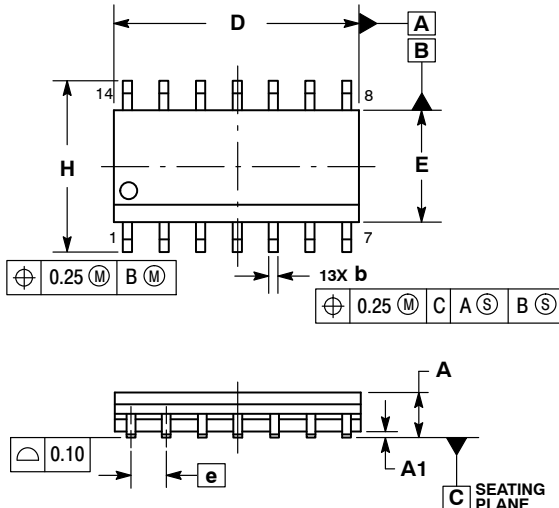
Device	Marking	Package	Shipping [†]
MC74LCX14DG	LCX14G	SOIC-14	55 Units / Rail
MC74LCX14DR2G	LCX14G	SOIC-14	2500 / Tape & Reel
MC74LCX14DTG	LCX 14	TSSOP-14	96 Units / Rail
MC74LCX14DTR2G	LCX 14	TSSOP-14	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

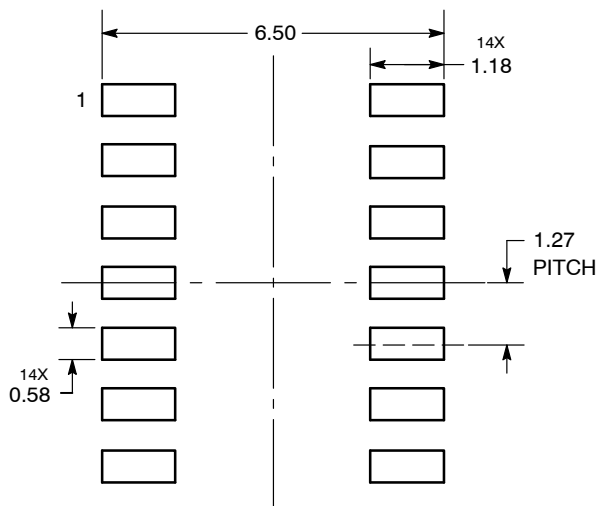


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

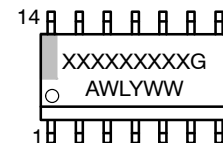
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

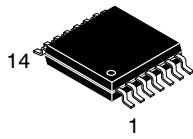
STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

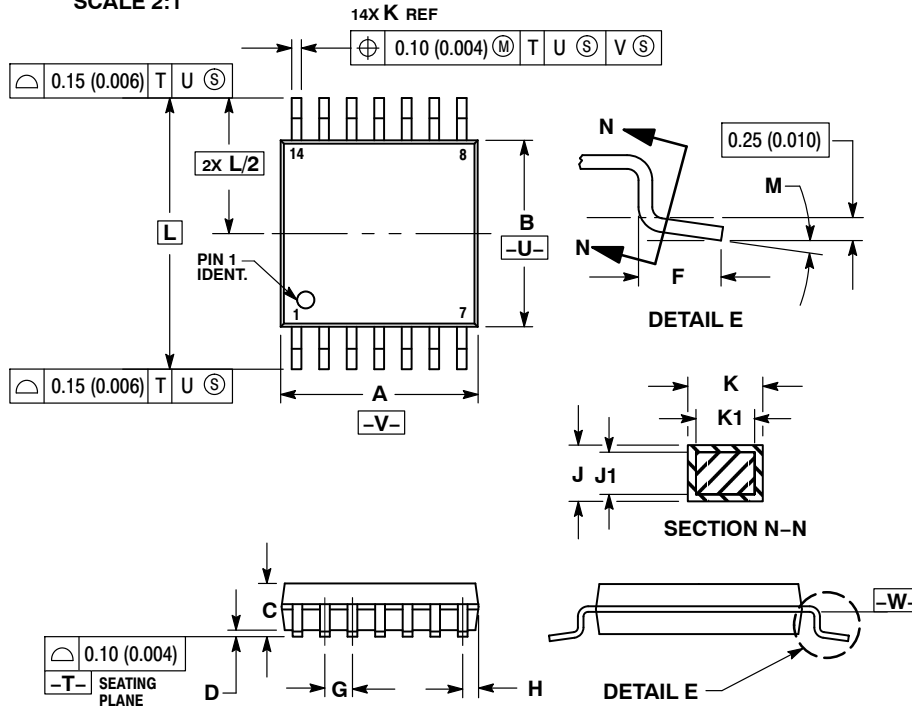
DOCUMENT NUMBER:	98ASB42565B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-14 NB	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.


TSSOP-14 WB
CASE 948G
ISSUE C

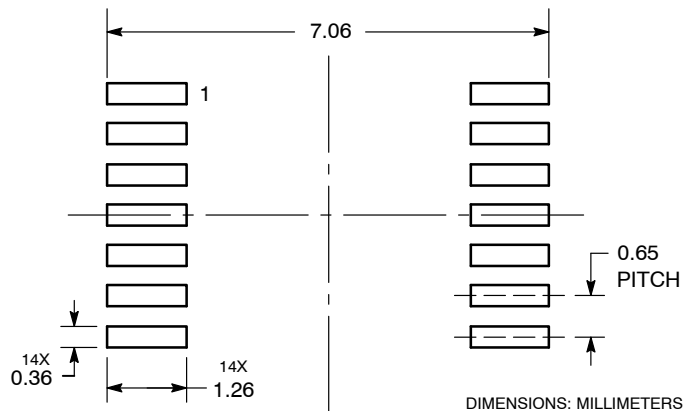
DATE 17 FEB 2016

SCALE 2:1

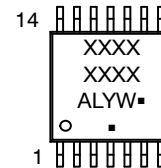

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER: 98ASH70246A

Electronic versions are uncontrolled except when accessed directly from the Document Repository.
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: TSSOP-14 WB

PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales