

NVMFD5485NL

MOSFET – Power, Dual N-Channel

60 V, 44 mΩ, 20 A



ON Semiconductor®

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Features

- Small Footprint (5x6 mm) for Compact Designs
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- 175°C Operating Temperature
- NVMFD5485NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	60	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 4)	Steady State	$T_C = 25^\circ\text{C}$	I_D 19.5 A
		$T_C = 100^\circ\text{C}$	13.8
		$T_C = 25^\circ\text{C}$	P_D 38.5 W
		$T_C = 100^\circ\text{C}$	19.2
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3 & 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D 5.3 A
		$T_A = 100^\circ\text{C}$	3.8
		$T_A = 25^\circ\text{C}$	P_D 2.9 W
		$T_A = 100^\circ\text{C}$	1.4
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	113 A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	37	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 25 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$)	E_{AS}	31	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

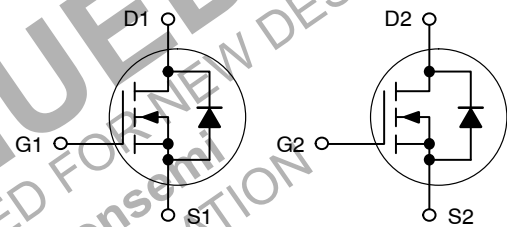
THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 2)	$R_{\theta JC}$	3.9	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	52	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted to an ideal (infinite) heat sink.
3. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
4. Maximum current for pulses as long as 1 second are higher but are dependent on pulse duration and duty cycle.

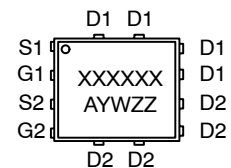
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	44 mΩ @ 10 V	20 A
	60 mΩ @ 4.5 V	

Dual N-Channel



DFN8 5x6 (SO8FL) CASE 506BT

MARKING DIAGRAM



XXXXXX = 5485NL
(NVMFD5485NL) or
5485LW
(NVMFD5485NLWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NVMFD5485NLT1G	DFN8 (Pb-Free)	1500/ Tape & Reel
NVMFD5485NLT3G	DFN8 (Pb-Free)	5000/ Tape & Reel
NVMFD5485NLWFT1G	DFN8 (Pb-Free)	1500/ Tape & Reel
NVMFD5485NLWFT3G	DFN8 (Pb-Free)	5000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVMFD5485NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to 25°C $I_D = 250\text{ }\mu\text{A}$		67		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V},$ $V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$		1.0 10	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5		2.5	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	Reference to 25°C $I_D = 250\text{ }\mu\text{A}$		-4.86		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		33	44	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		42	60	

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		560		pF
Output Capacitance	C_{oss}			126		
Reverse Transfer Capacitance	C_{rss}			58		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 10\text{ A}$		20		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.52		
Gate-to-Source Charge	Q_{GS}			1.9		
Gate-to-Drain Charge	Q_{GD}	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 10\text{ A}$		7.9		nC
Total Gate Charge	$Q_{G(TOT)}$			11.5		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 10\text{ A}, R_G = 2.5\text{ }\Omega$		9.5		ns
Rise Time	t_r			26.6		
Turn-Off Delay Time	$t_{d(off)}$			27.8		
Fall Time	t_f			23.7		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 15\text{ A}$	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$	0.93 0.83	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 10\text{ A}$		28.9		ns
Charge Time	t_a			23.2		
Discharge Time	t_b			5.6		
Reverse Recovery Charge	Q_{RR}			35.5		nC

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.93		nH
Drain Inductance	L_D			0.005		
Gate Inductance	L_G			1.84		
Gate Resistance	R_G			12		Ω

5. Pulse Test: pulse width = 300 μs , duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

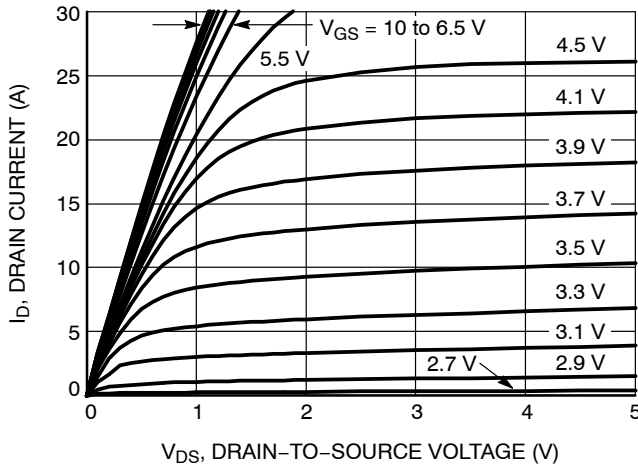


Figure 1. On-Region Characteristics

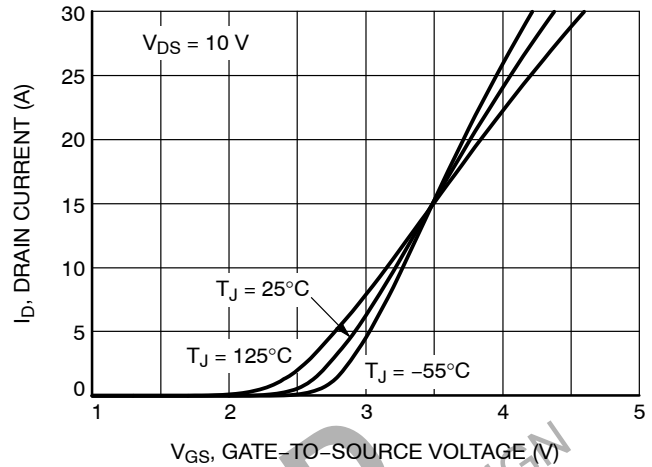


Figure 2. Transfer Characteristics

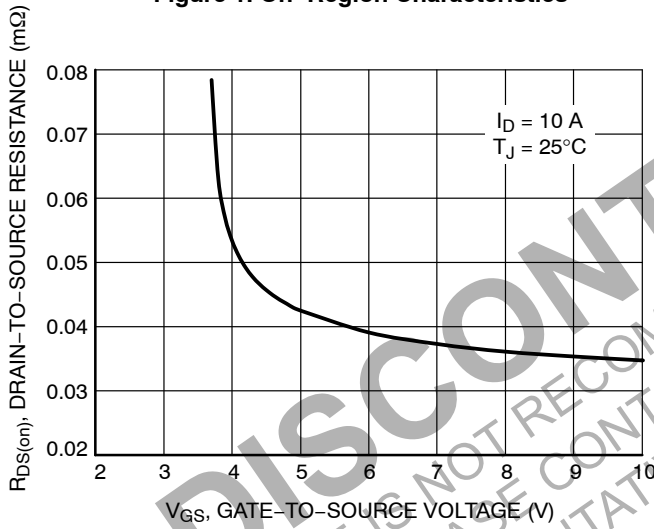


Figure 3. On-Resistance vs. V_{GS}

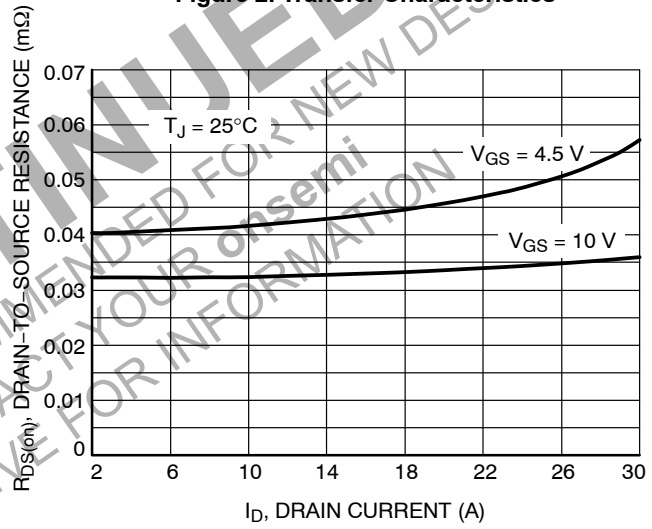


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

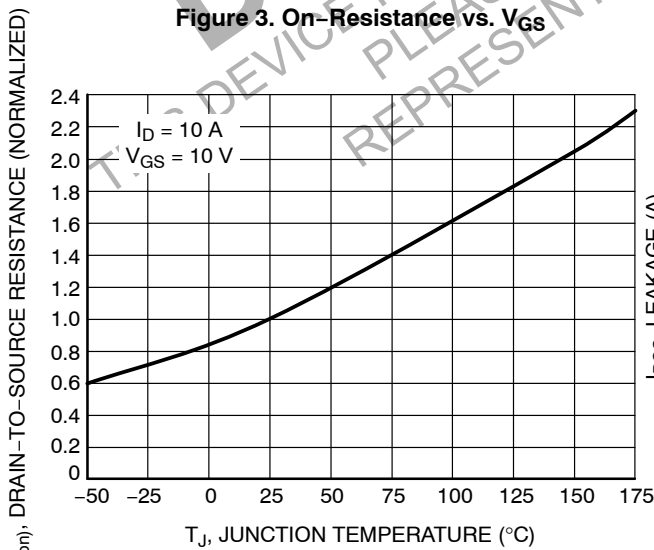


Figure 5. On-Resistance Variation with Temperature

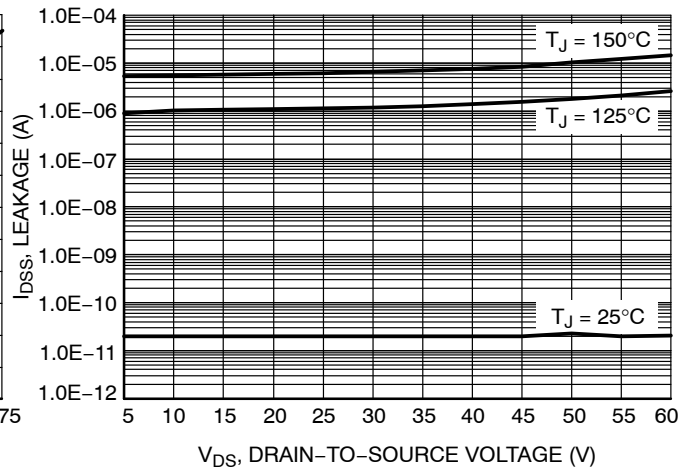


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

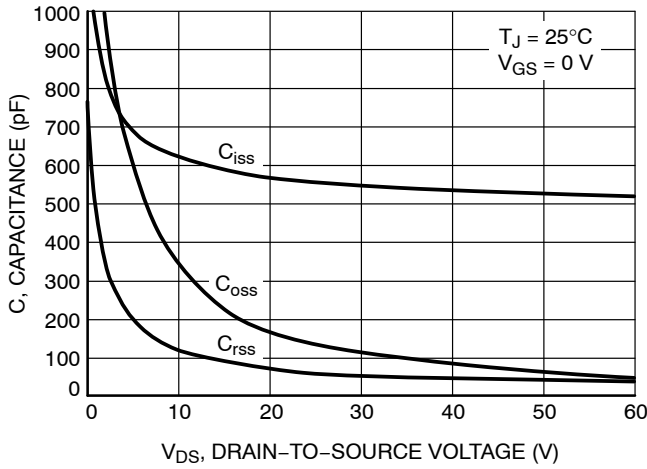


Figure 7. Capacitance Variation

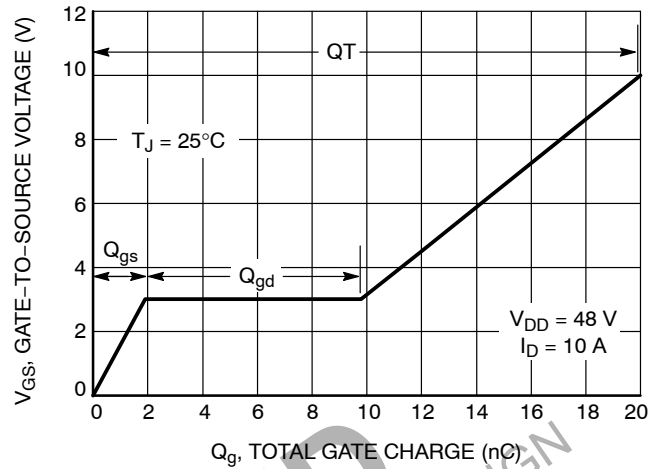


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

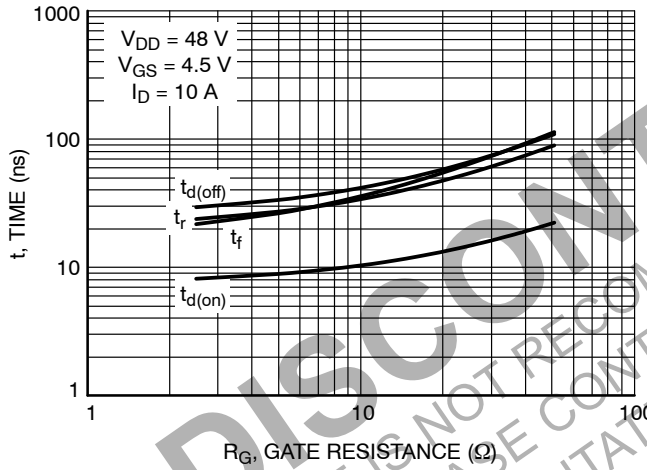


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

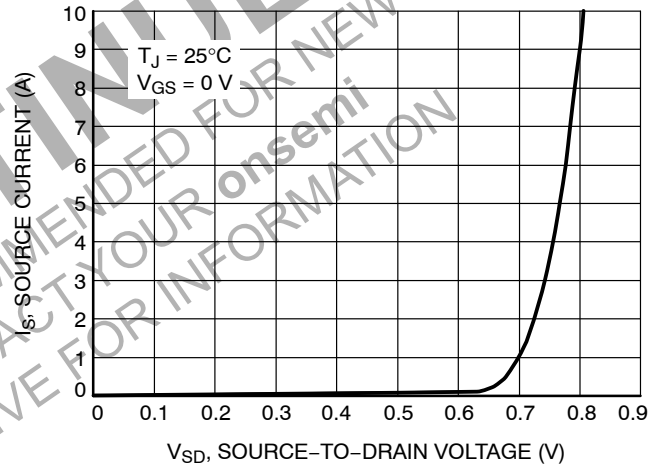


Figure 10. Diode Forward Voltage vs. Current

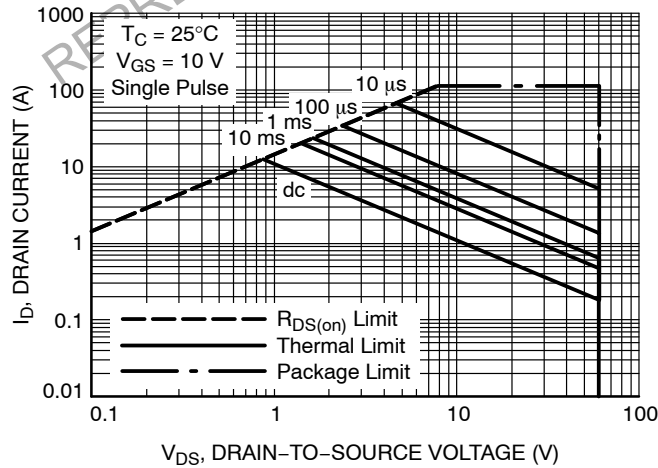


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL CHARACTERISTICS

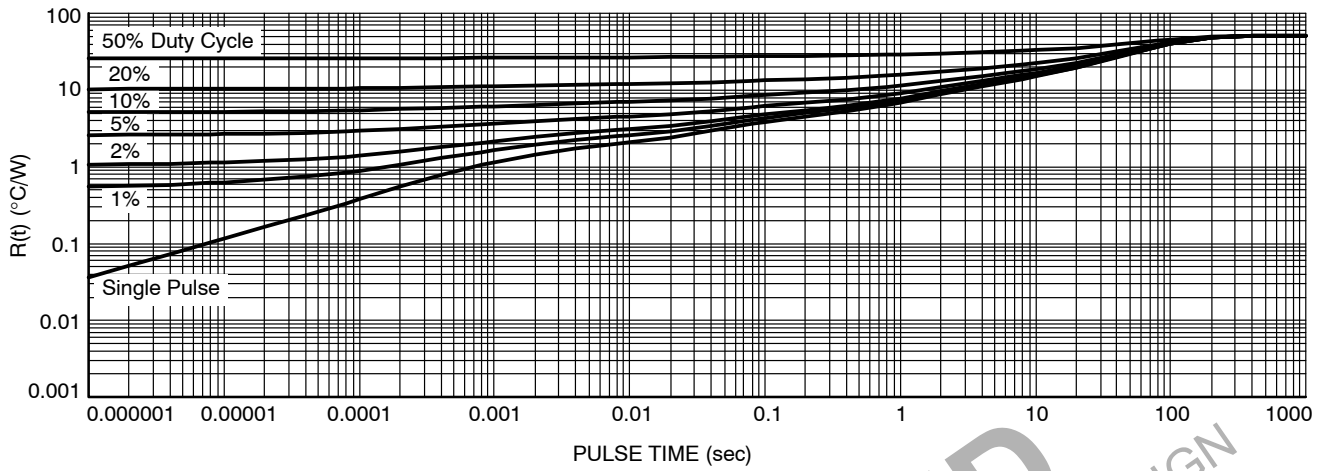
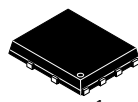


Figure 12. Thermal Response

DISCONTINUED
 THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
 PLEASE CONTACT YOUR onsemi
 REPRESENTATIVE FOR INFORMATION



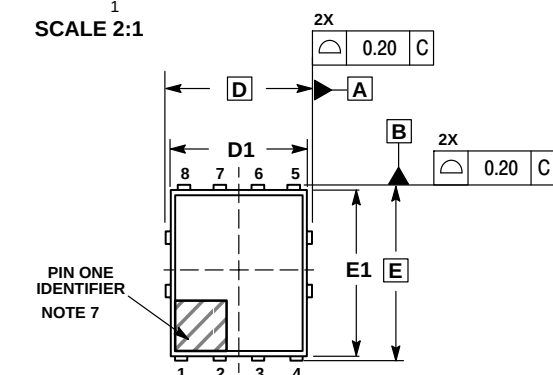
DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)

CASE 506BT

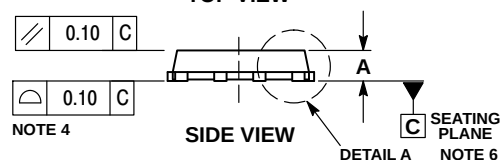
ISSUE F

DATE 23 NOV 2021

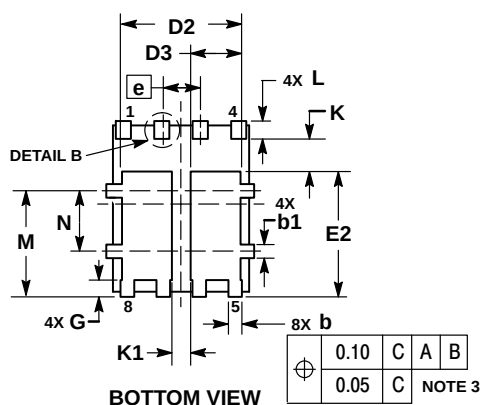
SCALE 2:1



TOP VIEW

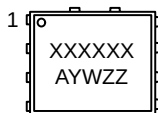


SIDE VIEW



BOTTOM VIEW

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code

A = Assembly Location

Y = Year

W = Work Week

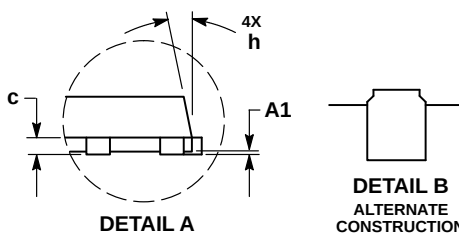
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "a", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

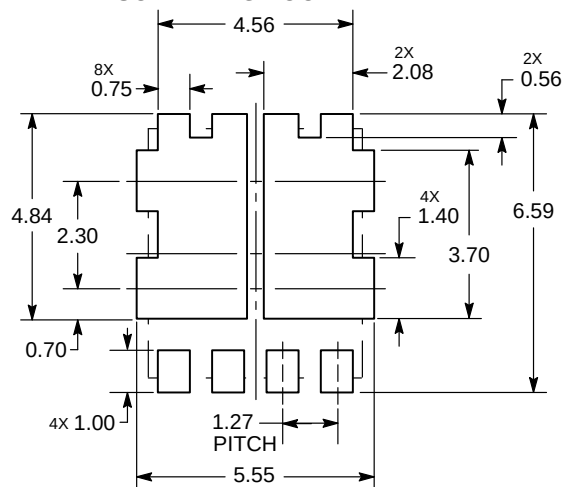
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	----	1.10
A1		----	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	----	0.33
D		5.15 BSC	
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E		6.15 BSC	
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e		1.27 BSC	
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	----	----
K1	0.56	----	----
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20



DETAIL B
ALTERNATE
CONSTRUCTION

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)	PAGE 1 OF 1

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