

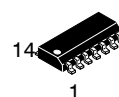
Low-Voltage CMOS Unbuffered Hex Inverter With 5 V-Tolerant Inputs

MC74LCXU04

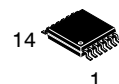
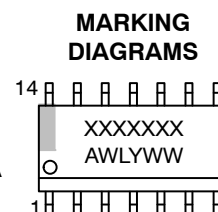
The MC74LCXU04 is a high performance unbuffered hex inverter operating from a 1.65 to 5.5 V supply. (High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance.) A V_I specification of 5.5 V allows MC74LCXU04 inputs to be safely driven from 5 V devices.

Features

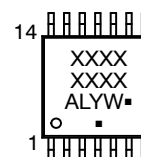
- Designed for 1.65 to 5.5 V V_{CC} Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTTL Compatible
- LVC MOS Compatible
- Near Zero Static Supply Current (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
 - ♦ Human Body Model >2000 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



XXXXXX = Specific Device Code
 A = Assembly Location
 L, WL = Wafer Lot
 Y, YY = Year
 W, WW = Work Week
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74LCXU04

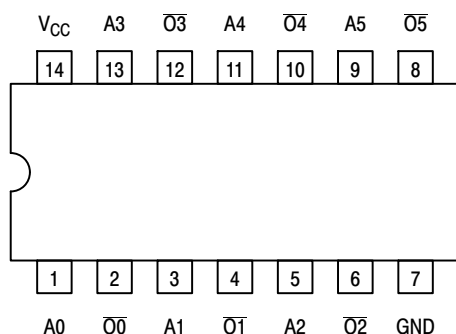


Figure 1. Pinout: 14-Lead (Top View)

PIN NAMES

Pins	Function
An	Data Inputs
$\overline{O_n}$	Outputs

TRUTH TABLE

An	$\overline{O_n}$
L	H
H	L

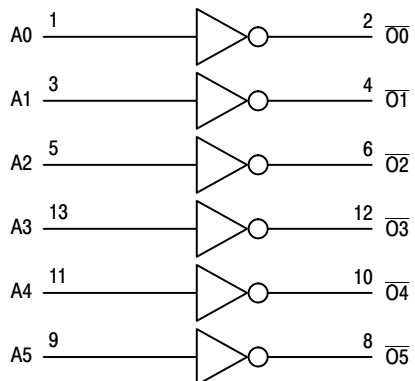


Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +6.5	V
V _I	DC Input Voltage (Note 1)	−0.5 to +6.5	V
V _O	DC Output Voltage (Note 1)	−0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current V _I < GND	−50	mA
I _{OK}	DC Output Diode Current V _O > V _{CC} , V _O < GND	±50	mA
I _O	DC Output Source/Sink Current	±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 1) SOIC−14 TSSOP−14	116 150	°C/W
P _D	Power Dissipation in Still Air at 125°C SOIC−14 TSSOP−14	1077 833	mW
MSL	Moisture Sensitivity	Level 1	–
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V _{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- I_O absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
- HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

MC74LCXU04

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	3.3 3.3	5.5 5.5	V
V _I	Digital Input Voltage	0	–	5.5	V
V _O	Output Voltage	0	–	V _{CC}	V
T _A	Operating Free-Air Temperature	–40	–	+125	°C
t _r , t _f	Input Rise or Fall Rate V _{CC} = 1.65 V to 1.95 V V _{CC} = 2.3 V to 2.7 V V _{IN} from 0.8 V to 2.0 V, V _{CC} = 3.0 V V _{CC} = 4.5 V to 5.5 V	0 0 0 0	– – – –	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = –40°C to +85°C		T _A = –40°C to +125°C		Unit
				Min	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		1.65	1.2	–	1.2	–	V
			2.3	1.7	–	1.7	–	
			2.7	2.1	–	2.1	–	
			3.0	2.2	–	2.2	–	
			3.6	2.7	–	2.7	–	
			4.5	3.4	–	3.4	–	
V _{IL}	LOW Level Input Voltage		1.65	–	0.4	–	0.4	V
			2.3	–	0.6	–	0.6	
			2.7	–	0.7	–	0.7	
			3.0	–	0.8	–	0.8	
			3.6	–	0.9	–	0.9	
			4.5	–	1.1	–	1.1	
V _{OH}	High-Level Output Voltage	V _I = GND I _{OH} = –100 µA I _{OH} = –4 mA I _{OH} = –8 mA I _{OH} = –12 mA I _{OH} = –18 mA I _{OH} = –24 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 4.5	V _{CC} – 0.2 1.29 1.8 2.2 2.4 3.7	– – – – – –	V _{CC} – 0.2 1.29 1.8 2.2 2.4 3.7	– – – – – –	V
V _{OL}	Low-Level Output Voltage	V _I = V _{CC} I _{OL} = 100 µA I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 18 mA I _{OL} = 24 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 4.5	– – – – – –	0.2 0.36 0.6 0.4 0.5 0.55	– – – – – –	0.3 0.36 0.6 0.4 0.55 0.55	V
I _I	Input Leakage Current	V _I = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	µA
I _{OFF}	Power Off Leakage Current	V _I = 5.5 V	0	–	10	–	10	µA
I _{CC}	Quiescent Supply Current	V _I = 5.5 V or GND	3.6	–	10	–	10	µA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} – 0.6 V	2.3 to 3.6	–	500	–	500	µA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

MC74LCXU04

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V _{CC} (V)	T _A = -40°C to +85°C		T _A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	See Figures 3 and 4	1.65 to 1.95	–	4.6	–	4.6	ns
			2.3 to 2.7	–	4.3	–	4.3	
			2.7	–	4.5	–	4.5	
			3.0 to 3.6	–	3.6	–	3.6	
			4.5 to 5.5	–	3.3	–	3.3	
t _{OSSL} , t _{OSLH}	Output to Output Skew		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			4.5 to 5.5	–	–	–	–	

5. These AC parameters are preliminary and may be modified.

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

DYNAMIC SWITCHING CHARACTERISTICS

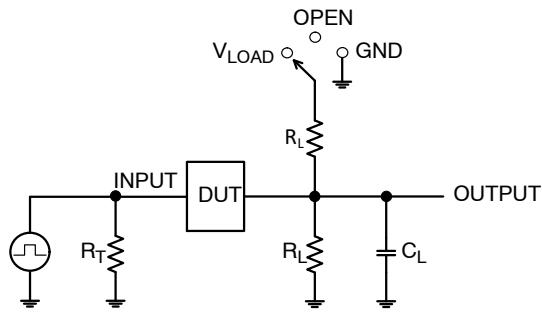
Symbol	Characteristic	Condition	T _A = +25°C			Units
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 7)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		0.8 0.6		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 7)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		–0.8 –0.6		V

7. Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	25	pF

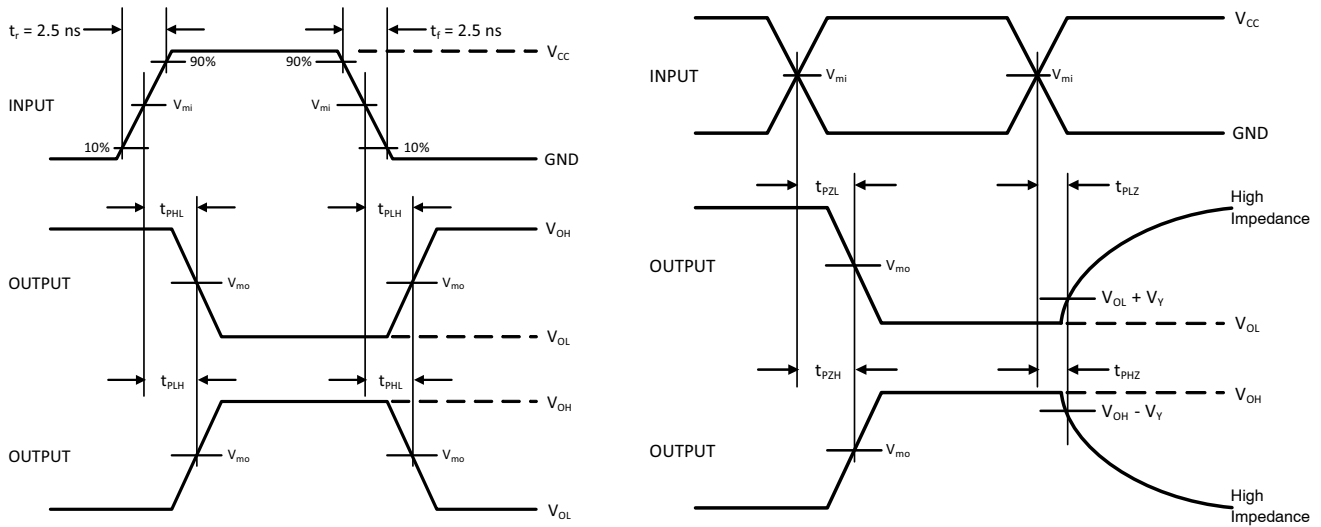
MC74LCXU04



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ MHz, $t_w = 500$ ns

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

Figure 3. Test Circuit



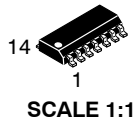
V_{CC} , V	R_L , Ω	C_L , pF	V_{LOAD}	V_m , V	V_Y , V
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	$V_{CC}/2$	0.3

Figure 4. Switching Waveforms

ORDERING INFORMATION

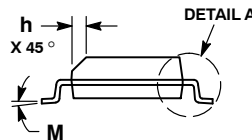
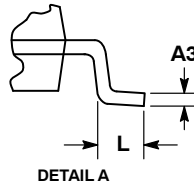
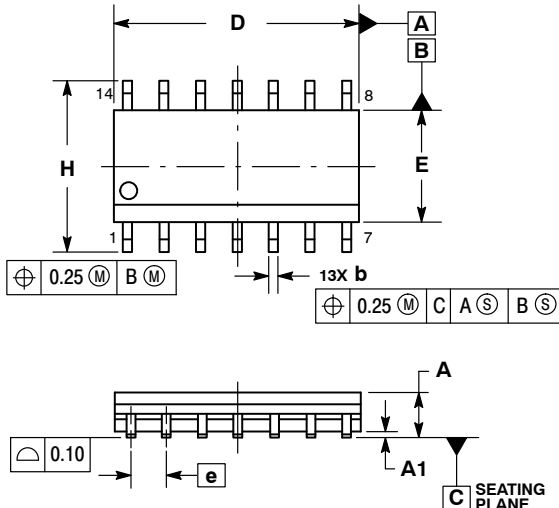
Device	Marking	Package	Shipping [†]
MC74LCXU04DG	LCXU04G	SOIC-14 (Pb-Free)	55 Units / Rail
MC74LCXU04DR2G	LCXU04G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74LCXU04DTR2G	LCX U04	TSSOP-14 (Pb-Free)	2500 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

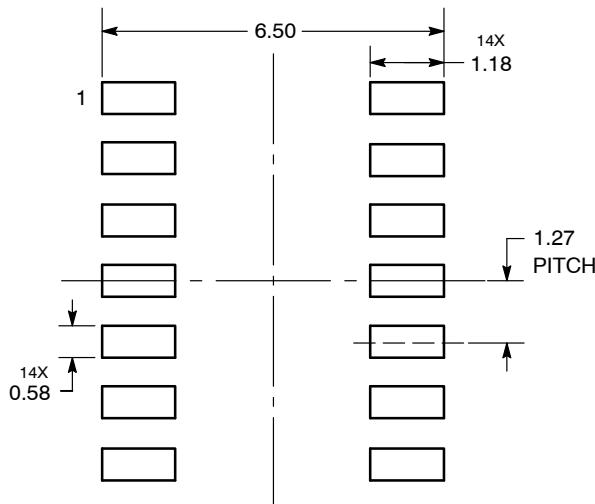


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

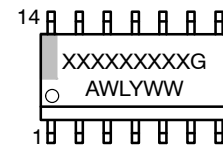
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

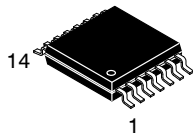
STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

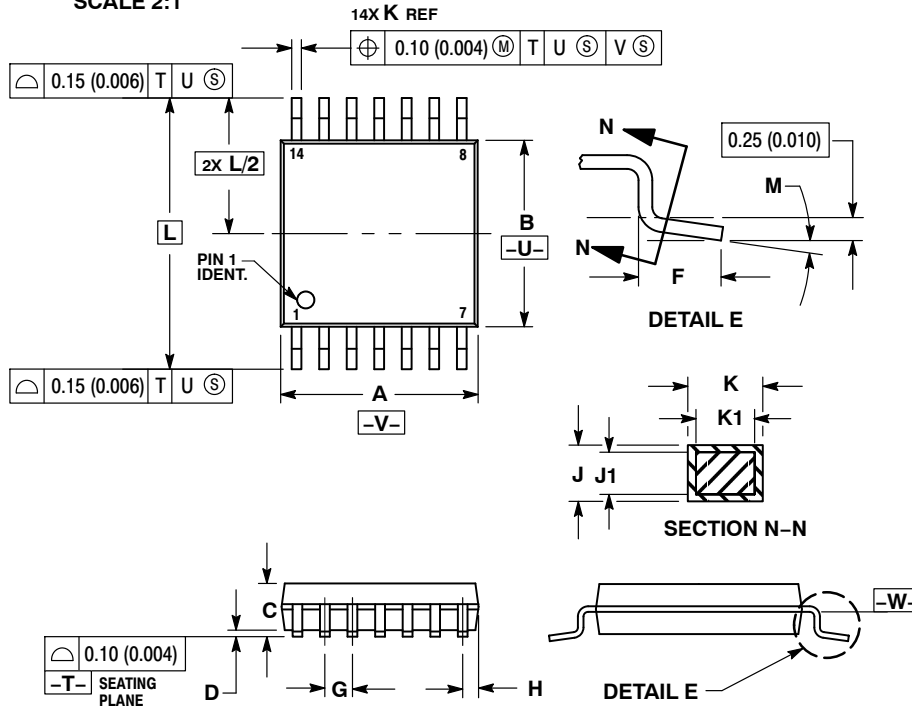
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TSSOP-14 WB
CASE 948G
ISSUE C

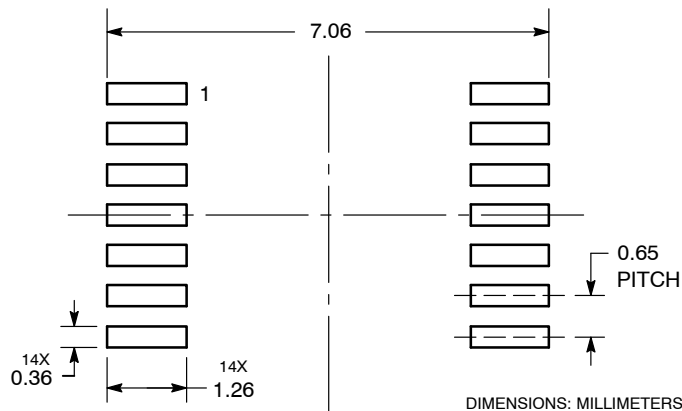
DATE 17 FEB 2016

SCALE 2:1

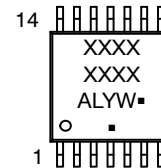

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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