

MOSFET – N-Channel, UniFET™, FRFET®

500 V, 20 A, 260 mΩ

FDP20N50F / FDPF20N50FT

Description

UniFET MOSFET is onsemi's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100 ns and the reverse dv/dt immunity is 15 V/ns while normal planar MOSFET's have over 200 ns and 4.5 V/ns respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

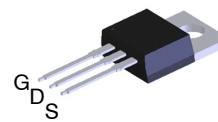
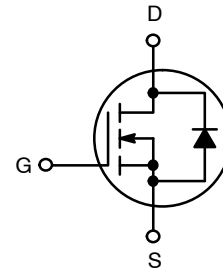
Features

- $R_{DS(on)} = 210 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 10 \text{ A}$
- Low Gate Charge (Typ. 50 nC)
- Low C_{rss} (Typ. 27 pF)
- 100% Avalanche Tested
- Improve dv/dt Capability
- These Devices are Pb-Free and are RoHS Compliant

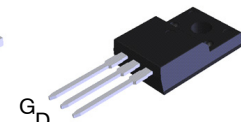
Applications

- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

V_{DS}	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
500 V	260 mΩ @ 10 V	20 A



TO-220-3LD
CASE 340AT



TO-220 Fullpack, 3-Lead
/ TO-220F-3SG
CASE 221AT

MARKING DIAGRAM

FDP 20N50F AYWWZZ

FDPF20 N50FT AYWWZZ

FDP20N50F,
FDPF20N50FT = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FDP20N50F	TO-220	1000 Units / Tube
FDPF20N50FT	TO-220F	1000 Units / Tube

FDP20N50F / FDPF20N50FT

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	FDP20N50F	FDPF20N50FT	Unit
V _{DSS}	Drain to Source Voltage	500		V
V _{GSS}	Gate to Source Voltage	±30		V
I _D	Drain Current – – Continuous (T _C = 25°C) – Continuous (T _C = 100°C)	20 12.9	20* 12.9*	A
I _{DM}	Drain Current – Pulsed (Note 1)	80	80*	A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	1110		mJ
I _{AR}	Avalanche Current (Note 1)	20		A
E _{AR}	Repetitive Avalanche Energy (Note 1)	25		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20		V/ns
P _D	Power Dissipation (T _C = 25°C) – Derate Above 25°C	250 2.0	38.5 0.3	W W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to +150		°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Second	300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 5 mH, I_{AS} = 20 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 20 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP20N50F	FDPF20N50FT	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case, Max.	0.5	3.3	°C/W
R _{θCS}	Thermal Resistance, Case-to-sink, Typ.	0.5	–	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V, T _J = 25°C	500	–	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.7	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	–	–	10	μA
		V _{DS} = 400 V, T _C = 125°C	–	–	100	
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	3.0	–	5.0	V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10 V, I _D = 10 A	–	0.22	0.26	Ω
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 10 A	–	25	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	2550	3390	pF
C _{oss}	Output Capacitance		–	350	465	pF
C _{rss}	Reverse Transfer Capacitance		–	27	40	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 20 A, V _{GS} = 10 V (Note 4)	–	50	65	nC
Q _{gs}	Gate to Source Gate Charge		–	14	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	20	–	nC

FDP20N50F / FDPF20N50FT

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}$, $I_D = 20\text{ A}$, $R_G = 25\ \Omega$ (Note 4)	–	45	100	ns
t_r	Turn-On Rise Time		–	120	250	ns
$t_{d(off)}$	Turn-Off Delay Time		–	100	210	ns
t_f	Turn-Off Fall Time		–	60	130	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	80	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 20\text{ A}$	–	–	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_{SD} = 20\text{ A}$ $dI_F/dt = 100\text{ A}/\mu\text{s}$	–	154	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

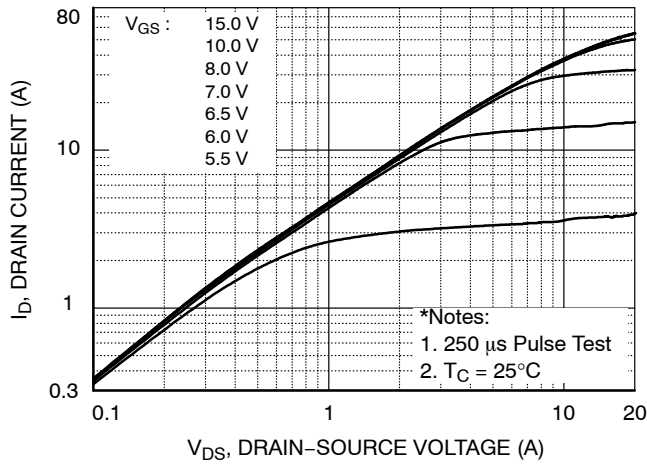


Figure 1. On-Region Characteristics

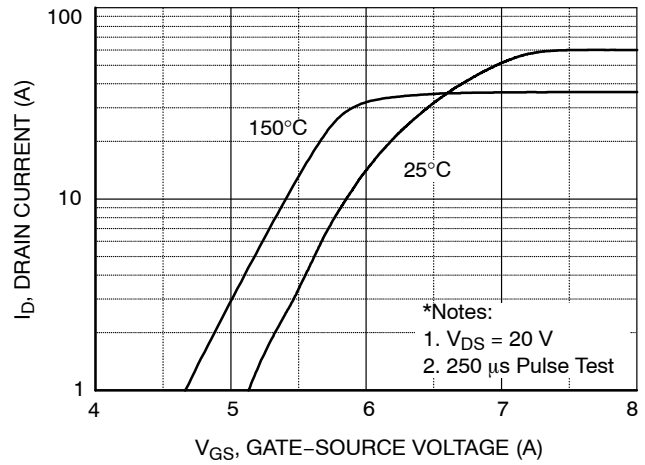


Figure 2. Transfer Characteristics

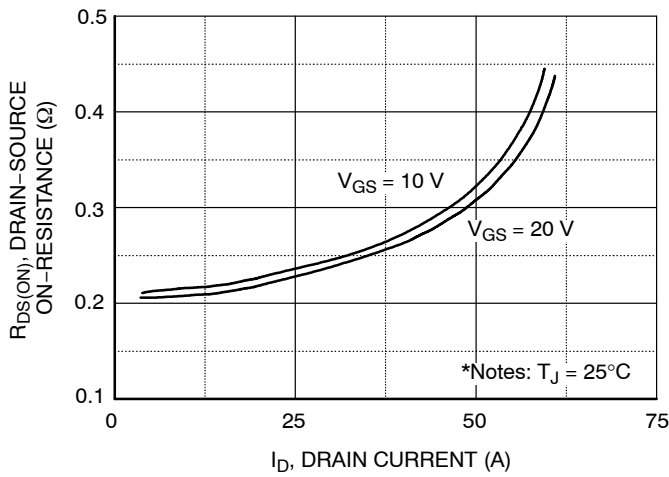


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

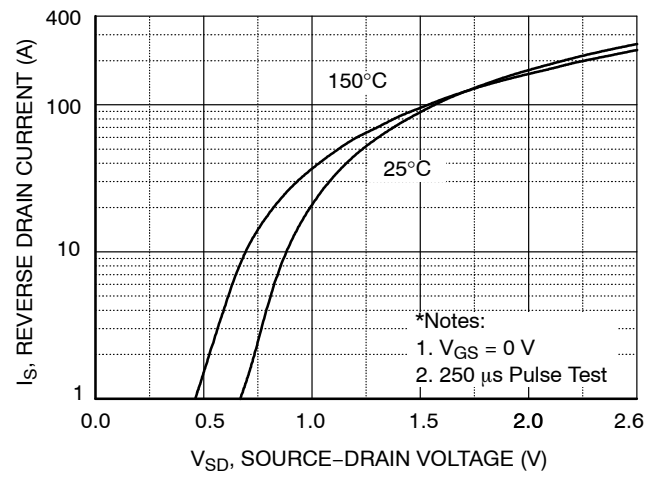


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

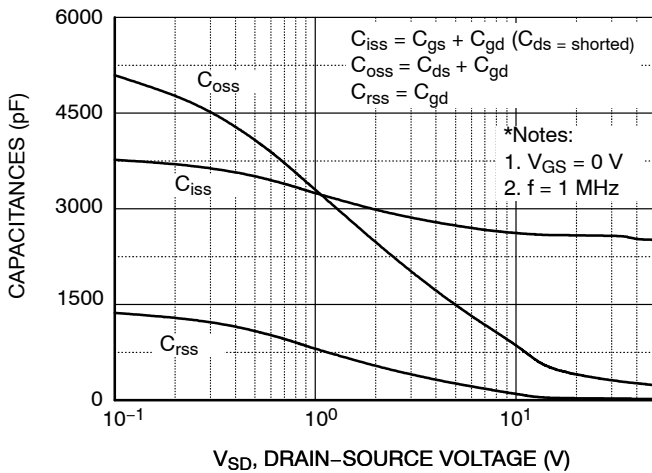


Figure 5. Capacitance Characteristics

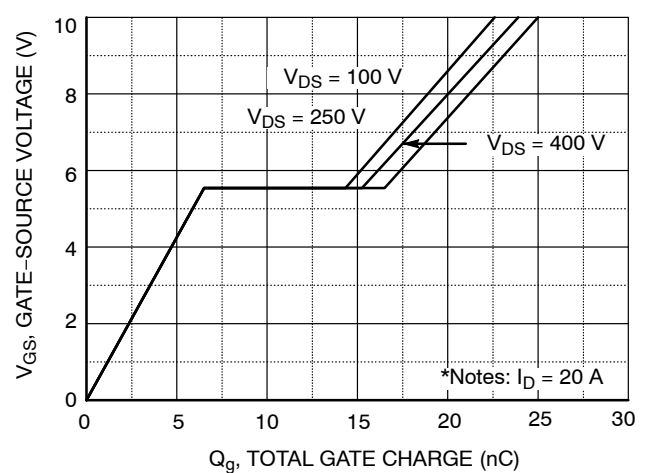


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (continued)

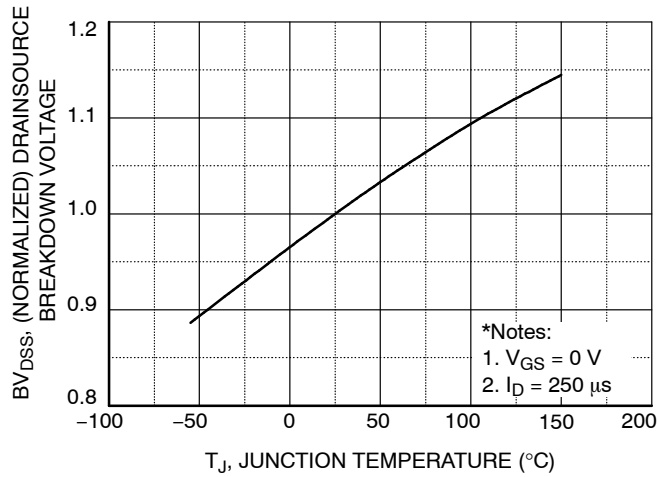


Figure 7. Breakdown Voltage Variation vs. Temperature

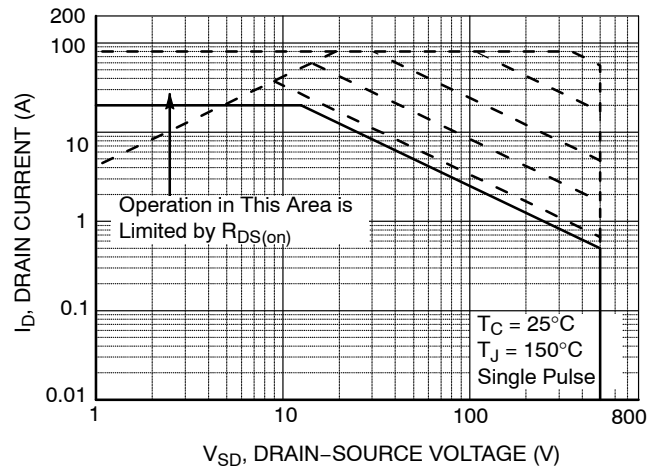


Figure 8. Maximum Safe Operating Area - FDP20N50F

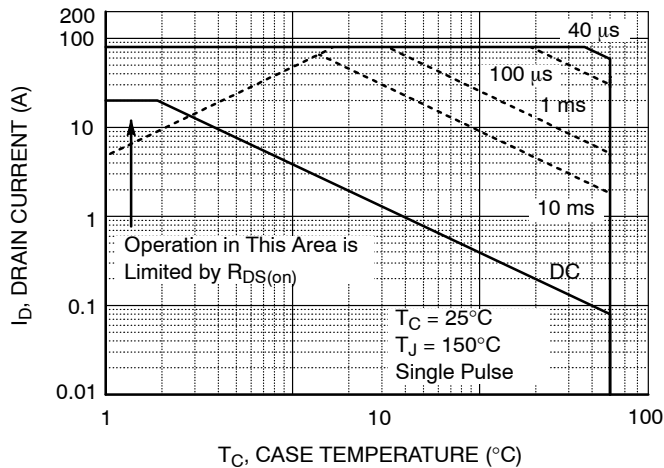


Figure 9. Maximum Safe Operating Area - FDP20N50F

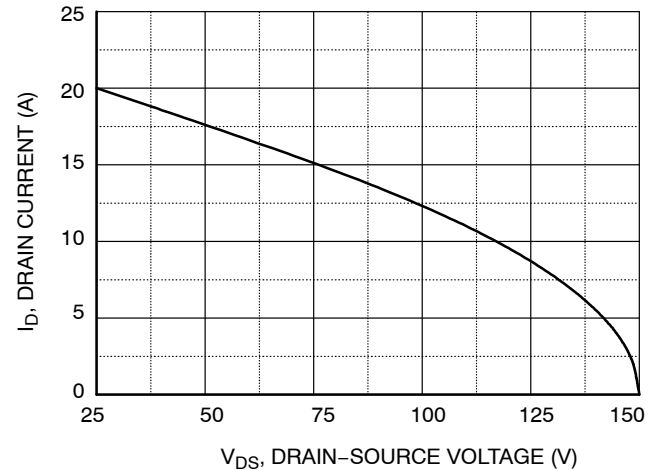


Figure 10. Maximum Drain Current vs. Case Temperature

FDP20N50F / FDPF20N50FT

Typical Performance Characteristics (continued)

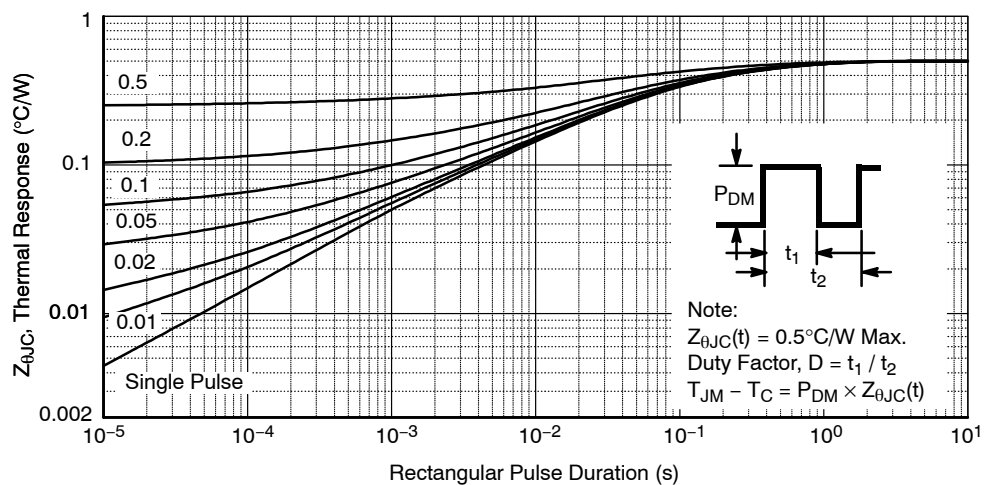


Figure 11. Transient Thermal Response Curve for FDP20N50F

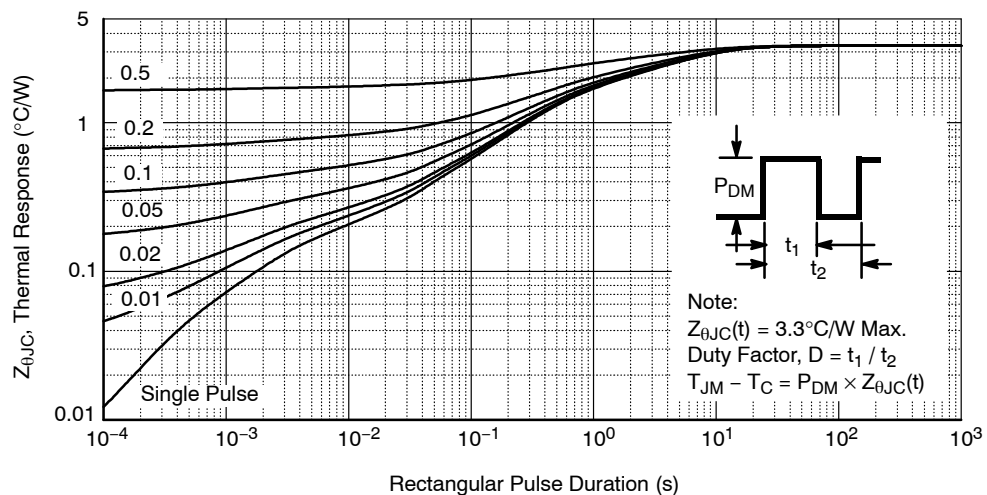


Figure 12. Transient Thermal Response Curve for FDPF20N50FT

FDP20N50F / FDPF20N50FT

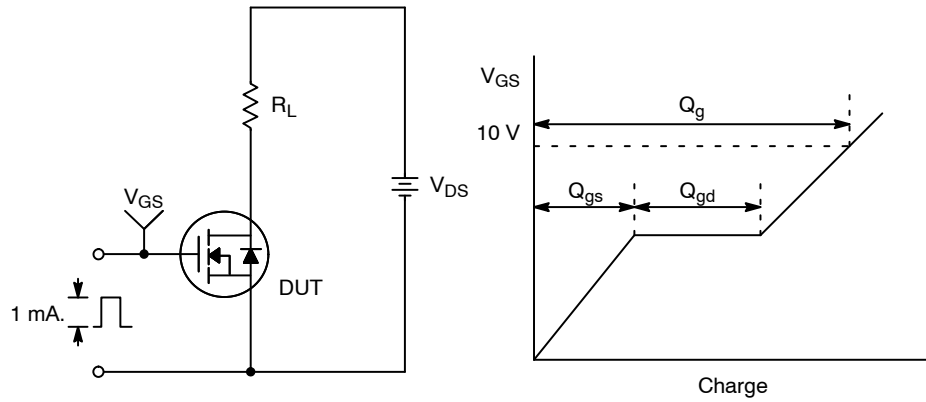


Figure 13. Gate Charge Test Circuit & Waveform

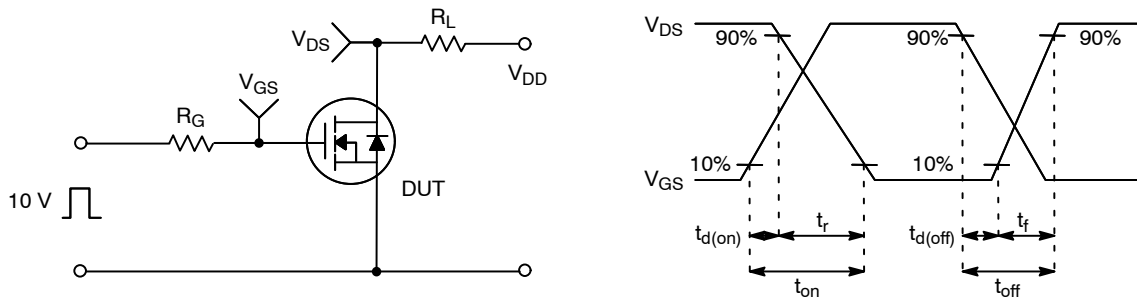


Figure 14. Resistive Switching Test Circuit & Waveforms

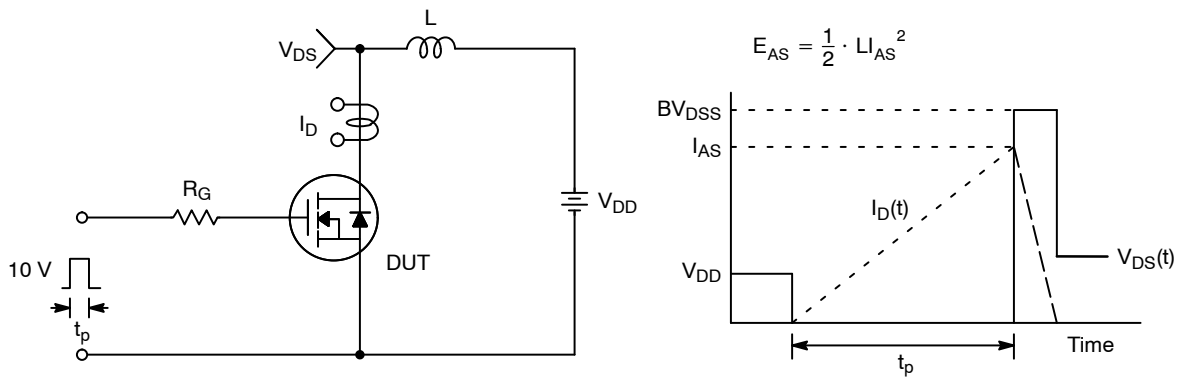


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

FDP20N50F / FDPF20N50FT

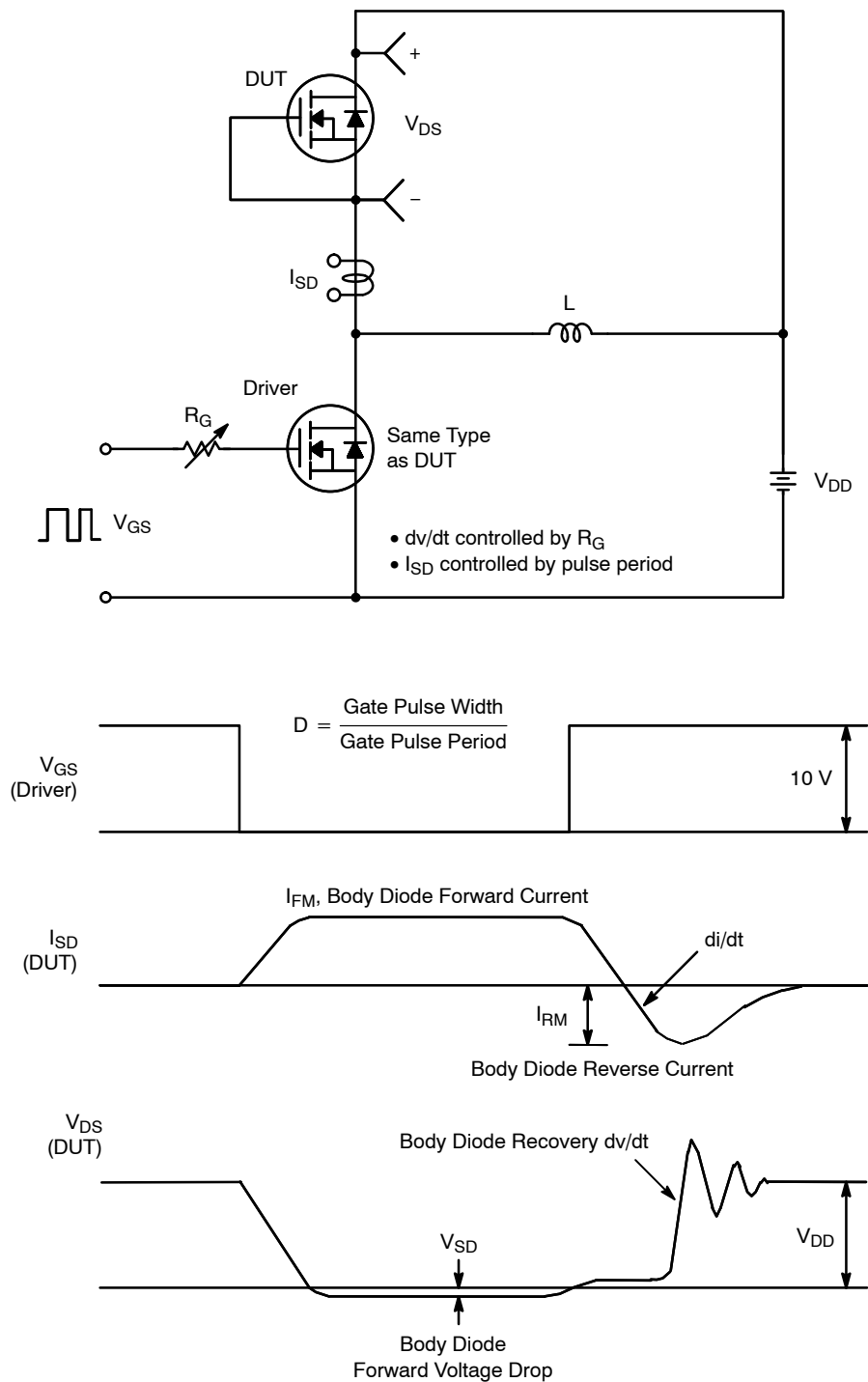


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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TO-220 Fullpack, 3-Lead / TO-220F-3SG
CASE 221AT
ISSUE B

DATE 19 JAN 2021



Scale 1:1



OPTION1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
Ø P	2.98	3.18	3.38
Ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:

A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009

B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.

C. OPTION 1 - WITH SUPPORT PIN HOLE

OPTION 2 - NO SUPPORT PIN HOLE

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TO-220-3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

IF PRESENT, SEE NOTE "D"

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
- G) PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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