

# Low-Voltage CMOS 3-to-8 Decoder/Demultiplexer

With 5 V-Tolerant Inputs

### **MC74LCX138**

The MC74LCX138 is a high performance, 3-to-8 decoder/demultiplexer operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_{\rm I}$  specification of 5.5 V allows MC74LCX138 inputs to be safely driven from 5 V devices. The MC74LCX138 is suitable for memory address decoding and other TTL level bus-oriented applications.

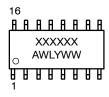
The MC74LCX138 high-speed 3–to–8 decoder/demultiplexer accepts three binary weighted inputs (A0, A1, A2) and, when enabled, provides eight mutually exclusive active-LOW outputs  $(\overline{O0}-\overline{O7})$ . The LCX138 features three Enable inputs, two active-LOW  $(\overline{E1},\overline{E2})$  and one active-HIGH (E3). All outputs will be HIGH unless  $\overline{E1}$  and  $\overline{E2}$  are LOW, and E3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1–of–32 (5 lines to 32 lines) decoder with just four LCX138 devices and one inverter (see Figure 1). The LCX138 can be used as an 8–output demultiplexer by using one of the active-LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Current drive capability is 24 mA at the outputs at 3 V.

#### **Features**

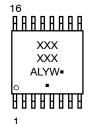
- Designed for 1.65 V to 5.5 V V<sub>CC</sub> Operation
- 5 V Tolerant Inputs Interface Capability With 5 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability at 3 V
- Near Zero Static Supply Current (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model >2000 V
- –Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant





MARKING DIAGRAMS





A = Assembly Location

WL, L = Wafer Lot Y = Year WW, W = Work Week G or = Pb-Free Package

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

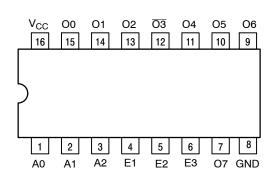


Figure 1. Pinout: 16-Lead (Top View)

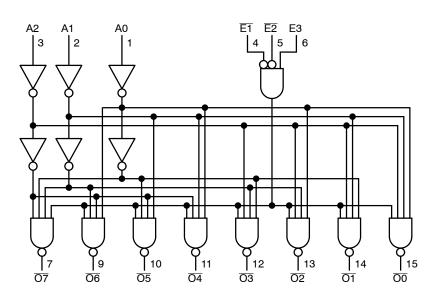


Figure 2. Logic Diagram

#### **PIN NAMES**

Pins	Function
<u>A0-A2</u>	Address Inputs
E1-E2	Enable Inputs
<u>E3</u>	Enable Input
00-07	Outputs

#### **TRUTH TABLE**

		Inp	uts			Outputs							
E1	E2	E3	A0	A1	A2	00	01	02	O3	04	O5	O6	07
Н	Х	Х	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
X	Н	Х	X	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
X	X	L	Х	Х	Х	Н	Н	Н	Н	Н	Н	Н	Н
L	L	Н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	L	Н	Н	L	L	Н	L	Н	Н	Н	Н	Н	Н
L	L	Н	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н
L	L	Н	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н
L	L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н
L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
L	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L

H = High Voltage Level

L = Low Voltage Level

X = High or Low Voltage Level and Transitions are Acceptable

For  $I_{\mbox{\footnotesize{CC}}}$  reasons, DO NOT FLOAT Inputs

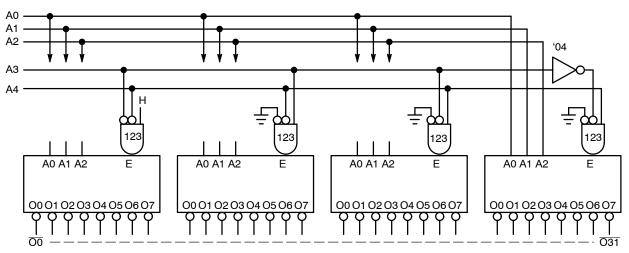


Figure 3. Expansion to 1-of-32 Decoding

#### **MAXIMUM RATINGS**

Symbol	Parameter		Value	Unit
V <sub>CC</sub>	DC Supply Voltage		-0.5 to +6.5	V
VI	DC Input Voltage (Note 1)		-0.5 to +6.5	V
Vo		le (High or Low State)  Tri-State Mode own Mode (V <sub>CC</sub> = 0 V)	-0.5 to V <sub>CC</sub> + 0.5 -0.5 to +6.5 -0.5 to +6.5	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>I</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current	V <sub>O</sub> < GND	-50	mA
I <sub>O</sub>	DC Output Source/Sink Current		±50	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T <sub>STG</sub>	Storage Temperature Range		-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs		260	°C
$T_J$	Junction Temperature Under Bias		+150	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 1)	SOIC-16 WQFN-16 TSSOP-16	126 114 159	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 25°C	SOIC-16 WQFN-16 TSSOP-16	995 1094 787	mW
MSL	Moisture Sensitivity		Level 1	-
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in	-
V <sub>ESD</sub>	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	٧

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. I<sub>O</sub> absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
   HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol		Parameter	Min	Тур	Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating Data Retention Only	1.65 1.5	3.3 3.3	5.5 5.5	V
VI	Digital Input Voltage		0	_	5.5	V
Vo	Output Voltage	Active Mode (High or Low State) Tri-State Mode Power Down Mode ( $V_{CC} = 0 V$ )	0 0 0	- - -	V <sub>CC</sub> 5.5 5.5	٧
T <sub>A</sub>	Operating Free-Air Temperature		-40	_	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Rate	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V} \\ V_{CC} = 2.3 \text{ V to } 2.7 \text{ V} \\ V_{I} \text{ from } 0.8 \text{ V to } 2.0 \text{ V, } V_{CC} = 3.0 \text{ V} \\ V_{CC} = 4.5 \text{ V to } 5.5 \text{ V} \\ \end{cases}$	0 0 0 0	- - -	20 20 10 5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

#### DC ELECTRICAL CHARACTERISTICS

				T <sub>A</sub> = -40 °C	c to +85 °C	T <sub>A</sub> = -40 °C	to +125 °C	
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Min	Max	Unit
V <sub>IH</sub> HIGH Level Input Voltag	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V <sub>CC</sub>	-	0.65 x V <sub>CC</sub>	_	V
			2.3 – 2.7	1.7	-	1.7	-	
			3.0 – 3.6	2.0	_	2.0	-	
			4.5 – 5.5	0.70 x V <sub>CC</sub>	-	0.70 x V <sub>CC</sub>	_	
V <sub>IL</sub>	LOW Level Input Voltage		1.65 – 1.95	-	0.35 x V <sub>CC</sub>	-	0.35 x V <sub>CC</sub>	V
			2.3 – 2.7	-	0.7	-	0.7	
			3.0 – 3.6	-	0.8	-	0.8	
			4.5 – 5.5	_	0.30 x V <sub>CC</sub>	-	0.30 x V <sub>CC</sub>	
V <sub>OH</sub>	High-Level Output Voltage	$V_I = V_{IH}$ or $V_{IL}$						V
		$I_{OH} = -100 \mu A$	1.65 to 5.5	V <sub>CC</sub> – 0.1	-	$V_{CC} - 0.1$	-	
		$I_{OH} = -4 \text{ mA}$	1.65	1.29	_	1.29	-	
		$I_{OH} = -8 \text{ mA}$	2.3	1.8	-	1.8	-	
		$I_{OH} = -12 \text{ mA}$	2.7	2.2	_	2.2	-	
		$I_{OH} = -16 \text{ mA}$	3.0	2.4	_	2.4	-	
		I <sub>OH</sub> = -24 mA	3.0	2.2	_	2.2	-	
		I <sub>OH</sub> = −32 mA	4.5	3.7		3.7	-	
$V_{OL}$	Low-Level Output Voltage	$V_I = V_{IH}$ or $V_{IL}$						V
		I <sub>OL</sub> = 100 μA	1.65 to 5.5	_	0.1	_	0.1	
		$I_{OL} = 4 \text{ mA}$	1.65	_	0.24	_	0.24	
		$I_{OL} = 8 \text{ mA}$	2.3	_	0.3	_	0.3	
		I <sub>OL</sub> = 12 mA	2.7	_	0.4	_	0.4	
		I <sub>OL</sub> = 16 mA	3.0	_	0.4	_	0.4	
		I <sub>OL</sub> = 24 mA	3.0	_	0.55		0.55	
		I <sub>OL</sub> = 32 mA	4.5	_	0.6	_	0.6	
IĮ	Input Leakage Current	V <sub>I</sub> = 0 to 5.5 V	3.6	_	±5.0	-	±5.0	μΑ
I <sub>OFF</sub>	Power Off Leakage Current	V <sub>I</sub> = 5.5 V or V <sub>O</sub> = 5.5 V	0	-	10	-	10	μΑ

#### DC ELECTRICAL CHARACTERISTICS (continued)

				T <sub>A</sub> = -40 °C	c to +85 °C	T <sub>A</sub> = -40 °C	to +125 °C	
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Min	Max	Unit
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = 5.5 V or GND	3.6	-	10	-	10	μΑ
$\Delta I_{CC}$	Increase in I <sub>CC</sub> per Input	$V_{IH} = V_{CC} - 0.6 V$	2.3 to 3.6	-	500	-	500	μΑ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### **AC ELECTRICAL CHARACTERISTICS**

				T <sub>A</sub> = -40 °	C to +85 °C	T <sub>A</sub> = -40 °C	C to +125 °C	
Symbol	Parameter	Test Condition	V <sub>CC</sub> (V)	Min	Max	Min	Max	Unit
$t_{PLH}$ , $t_{PHL}$	Propagation Delay,	See Figures 4 and 5	1.65 to 1.95	-	11.5	-	11.5	ns
	An to On		2.3 to 2.7	-	7.2	-	7.2	
		2.7 - 7.0	7.0	-	7.0			
			3.0 to 3.6	-	6.0	-	6.0	
			4.5 to 5.5	-	5.0	-	5.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay,	See Figures 4 and 5	1.65 to 1.95	-	12.0	-	12.0	ns
	E1, E2 to On		2.3 to 2.7	-	8.4	-	8.4	
		2.7	-	7.5	-	7.5		
			3.0 to 3.6	-	6.5	-	6.5	
			4.5 to 5.5	-	5.5	-	5.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay,	See Figures 4 and 5	1.65 to 1.95	-	11.5	-	11.5	ns
	E3 to On		2.3 to 2.7	-	7.2	-	7.2	
			2.7	-	7.0	-	7.0	
			3.0 to 3.6	-	6.0	-	6.0	
			4.5 to 5.5	-	5.0	-	5.0	
t <sub>OSHL</sub> ,	Output to Output Skew		1.65 to 1.95	-	-	-	-	ns
toslh	(Note 5)		2.3 to 2.7	-	-	-	-	
			2.7	-	-	-	-	
			3.0 to 3.6	-	1.0	-	1.0	
			4.5 to 5.5	-	-	-	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product

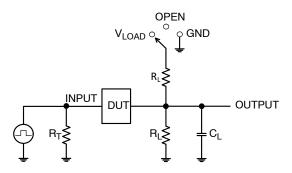
#### **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Units
C <sub>IN</sub>	Input Capacitance	$V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$	7	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC}$ = 3.3 V, $V_{I}$ = 0 V or $V_{CC}$	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10 MHz, $V_{CC}$ = 3.3 V, $V_I$ = 0 V or $V_{CC}$	25	pF

performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.

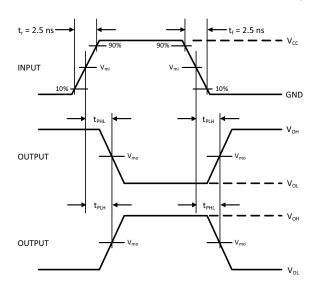
The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

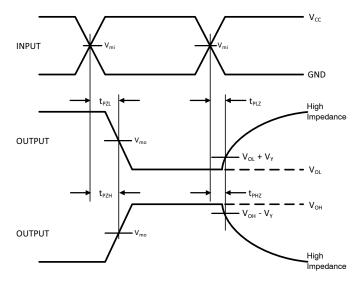


Test	Switch Position
t <sub>PLH</sub> / t <sub>PHL</sub>	Open
t <sub>PLZ</sub> / t <sub>PZL</sub>	$V_{LOAD}$
t <sub>PHZ</sub> / t <sub>PZH</sub>	GND

 $C_L$  includes probe and jig capacitance  $R_T$  is  $Z_{OUT}$  of pulse generator (typically 50  $\Omega)$  f = 1 MHz

Figure 4. Test Circuit





V <sub>CC</sub> , V	$R_L,\Omega$	C <sub>L</sub> , pF	V <sub>LOAD</sub>	V <sub>m</sub> , V	V <sub>Y</sub> , V
1.65 to 1.95	500	30	2 x V <sub>CC</sub>	V <sub>CC</sub> /2	0.15
2.3 to 2.7	500	30	2 x V <sub>CC</sub>	V <sub>CC</sub> /2	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	2 x V <sub>CC</sub>	V <sub>CC</sub> /2	0.3

Figure 5. Switching Waveforms

#### **ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
MC74LCX138DR2G	LCX138	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LCX138DR2G-Q*	LCX138	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LCX138DTG	LCX 138	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74LCX138DTR2G	LCX 138	TSSOP-16 (Pb-Free)	2500 Tape & Reel

#### **DISCONTINUED** (Note 6)

NLV74LCX138DR2G* LCX138	SOIC-16 (Pb-Free)	2500 Tape & Reel
-------------------------	----------------------	------------------

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*-</sup>Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

<sup>6.</sup> **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on <a href="https://www.onsemi.com">www.onsemi.com</a>.



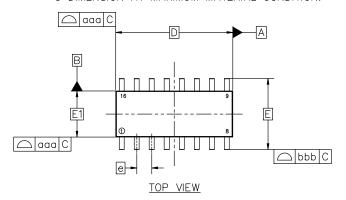


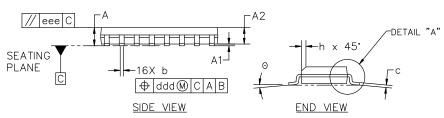
#### SOIC-16 9.90x3.90x1.37 1.27P CASE 751B ISSUE M

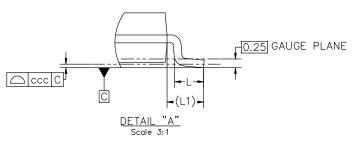
**DATE 18 OCT 2024** 

#### NOTES:

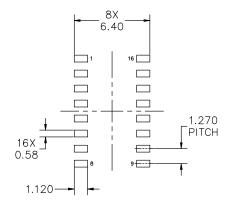
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
- 5. DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE 6 DIMENSION AT MAXIMUM MATERIAL CONDITION.







MILLIMETERS					
DIM	MIN	NOM	MAX		
А	1.35	1.55	1.75		
A1	0.10	0.18	0.25		
A2	1.25	1.37	1.50		
b	0.35	0.42	0.49		
С	0.19	0.22	0.25		
D	9.90 BSC				
E	6.00 BSC				
E1	3.90 BSC				
е	1.27 BSC				
h	0.25		0.50		
L	0.40	0.83	1.25		
L1	1.05 REF				
Θ	0 2.				
TOLERANCE OF FORM AND POSITION					
aaa	0.10				
bbb	0.20				
ccc	0.10				
ddd	0.25				
eee	0.10				



#### RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE onsemi SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P		PAGE 1 OF 2	

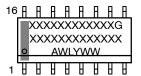
onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

#### **SOIC-16 9.90x3.90x1.37 1.27P** CASE 751B

ISSUE M

**DATE 18 OCT 2024** 

## GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code

A = Assembly Location
WL = Wafer Lot

Y = Year
WW = Work Week
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:		STYLE 2:		STYLE 3:	S	TYLE 4:	
	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
	BASE	2.	ANODE	2.	BASE. #1	2.	
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER. #1	3.	
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	
	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	
13.	BASE	13.		13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1
STYLE 5:		STYLE 6:		STYLE 7:			
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH		
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)		
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)		
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH		
5.	DRAIN, #3	5.		5.	COMMON DRAIN (OUTPUT)		
6.	DRAIN, #3	6.		6.	COMMON DRAIN (OUTPUT)		
7.	DRAIN, #4		CATHODE	7.	COMMON DRAIN (OUTPUT)		
8.	DRAIN, #4		CATHODE	8.	SOURCE P-CH		
a							
٥.	GATE, #4		ANODE	9.	SOURCE P-CH		
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)		
10. 11.	SOURCE, #4 GATE, #3	10. 11.	ANODE ANODE	10. 11.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
10. 11. 12.	SOURCE, #4 GATE, #3 SOURCE, #3	10. 11. 12.	ANODE ANODE ANODE	10. 11. 12.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
10. 11. 12. 13.	SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	10. 11. 12. 13.	ANODE ANODE ANODE ANODE	10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH		
10. 11. 12. 13. 14.	SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2	10. 11. 12. 13.	ANODE ANODE ANODE ANODE ANODE	10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT)		
10. 11. 12. 13. 14. 15.	SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 GATE, #1	10. 11. 12. 13. 14.	ANODE ANODE ANODE ANODE ANODE ANODE	10. 11. 12. 13. 14.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GOMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
10. 11. 12. 13. 14.	SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2	10. 11. 12. 13.	ANODE ANODE ANODE ANODE ANODE	10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT)		

DOCUMENT NUMBER:	98ASB42566B	B Electronic versions are uncontrolled except when accessed directly from the Document Repositor Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P		PAGE 2 OF 2	

onsemi and ONSEMi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

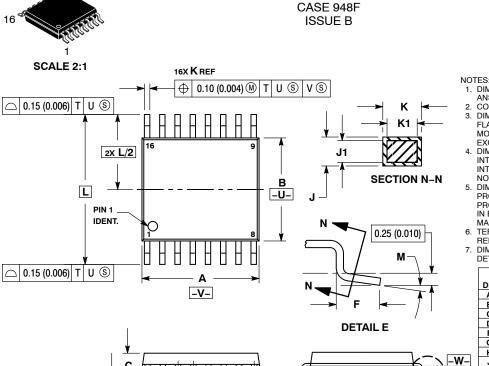
**DATE 19 OCT 2006** 



☐ 0.10 (0.004)

SEATING PLANE

D

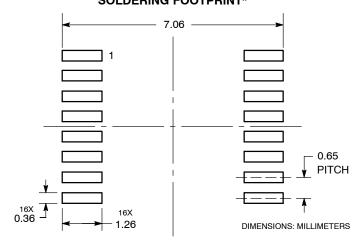


TSSOP-16 WB

- DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT
- EXCEED 0.15 (0.006) PER SIDE.
  DIMENSION B DOES NOT INCLUDE
  INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL
- IN TERLEAD FLASH OH PROTHOSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65 BSC		0.026 BSC		
Н	0.18	0.28	0.007	0.011	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40 BSC		0.252 BSC		
М	0 °	8°	0°	8 °	

#### **RECOMMENDED** SOLDERING FOOTPRINT\*



<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### **GENERIC** MARKING DIAGRAM\*



XXXX = Specific Device Code Α = Assembly Location

= Wafer Lot L = Year W = Work Week G or • = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repositor Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.		
DESCRIPTION:	TSSOP-16		PAGE 1 OF 1	

**DETAIL E** 

onsemi and ONSEMi, are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, ONSEMI., and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at <a href="www.onsemi.com/site/pdf/Patent-Marking.pdf">www.onsemi.com/site/pdf/Patent-Marking.pdf</a>. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems. or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

#### ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

 $\textbf{Technical Library:} \ \underline{www.onsemi.com/design/resources/technical-documentation}$ 

onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at

www.onsemi.com/support/sales