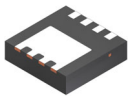
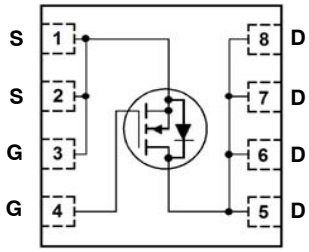
# MOSFET – N-Channel, Shielded Gate, POWER TRENCH®

## 100 V, 57 A, 8.5 mΩ

# FDMC86184



WDFN8 3.3X3.3, 0.65P
CASE 483AW




### Description

This N−Channel logic MV MOSFETs is produced using onsemi advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimize on−state resistance and yet maintain superior switching performance with best in class soft body diode.

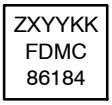
### Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 8.5 mΩ at $V_{GS}$ = 10 V, $I_D$ = 21 A
- Max $R_{DS(on)}$ = 24.8 mΩ at $V_{GS}$ = 6.5 V, $I_D$ = 10 A
- 50% Lower Qrr than Osther MOSFET Supplier
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- ESD Protection Level : HBM>1kV, CDM>2kV
- These Device is Pb−Free and RoHS Compliant

### Typical Applications or Applications

- Primary DC−DC MOSFET
- Synchronous Rectifier in DC−DC and AC−DC
- Motor Drive
- Solar

### MARKING DIAGRAM




FDMC86184 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDMC86184 | PQFN−8 | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

### MOSFET MAXIMUM RATINGS $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | 100 | V |
| $V_{GS}$ | Gate to Source Voltage | ±20 | V |
| $I_D$ | Drain Current<br>−Continuous ($T_A$ = 25°C) (Note 5)<br>−Continuous ($T_A$ = 100°C) (Note 5)<br>−Continuous ($T_A$ = 25°C) (Note 1)<br>−Pulsed (Note 4) | <br>57<br>36<br>12<br>266 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 3) | 121 | mJ |
| $P_D$ | Power Dissipation ($T_C$ = 25°C)<br>Power Dissipation ($T_A$ = 25°C) (Note 1) | 54<br>2.3 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 2.3 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1) | 53 | |

## ELECTRICAL CHARACTERISTICS $T_J$ = 25 °C unless otherwise noted.

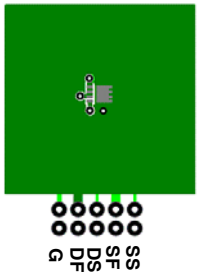
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 100 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | 59 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 110 μA | 2.0 | 3.1 | 4.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 110 μA, referenced to 25 °C | – | −9 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 21 A | – | 6.4 | 8.5 | mΩ |
| | | $V_{GS}$ = 6 V, $I_D$ = 10 A | – | 11 | 24.8 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 21 A, $T_J$ = 125 °C | – | 11 | 18 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 21 A | – | 49 | – | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 1490 | 2090 | pF |
| $C_{oss}$ | Output Capacitance | | – | 906 | 1270 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 13 | 25 | pF |
| $R_g$ | Gate Resistance | | 0.1 | 0.4 | 1.2 | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 21 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 12 | 22 | ns |
| $t_r$ | Rise Time | | – | 4 | 10 | ns |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 17 | 31 | ns |
| $t_f$ | Fall Time | | – | 4 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 50 V, $I_D$ = 21 A | – | 21 | 30 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 6 V, $V_{DD}$ = 50 V, $I_D$ = 21 A | – | 14 | 20 | nC |
| $Q_{gs}$ | Total Gate Charge | $V_{DD}$ = 50 V, $I_D$ = 21 A | – | 6.5 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 50 V, $I_D$ = 21 A | – | 4.6 | – | nC |
| $Q_{oss}$ | Output Charge | $V_{DD}$ = 50 V, $V_{GS}$ = 0 V | – | 61 | – | nC |

**ELECTRICAL CHARACTERISTICS** (continued)$T_J$ = 25 °C unless otherwise noted.

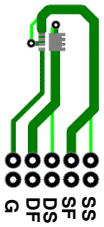
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Drain−Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | – | 0.7 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 21 A (Note 2) | – | 0.8 | 1.3 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 10 A, di/dt = 300 A/μs | – | 27 | 44 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 46 | 74 | nC |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 10 A, di/dt = 1000 A/μs | – | 21 | 34 | ns |
| $Q_{rr}$ | Reverse Recovery Time | | – | 96 | 154 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material $R_{\theta CA}$ is determined by the user's board design.




a. 53 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper




b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%
3. $E_{AS}$ of 121 mJ is based on starting $T_J$ = 25 °C; N−ch: L = 3 mH, $I_{AS}$ = 9 A, $V_{DD}$ = 100 V, $V_{GS}$ =10 V. 100% test at L = 0.3 mH, $I_{AS}$ = 21 A.
4. Pulsed Id please refer to Figure 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

## TYPICAL CHARACTERISTICS

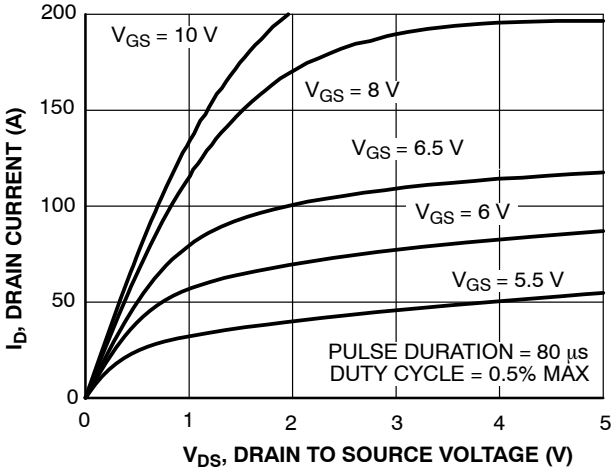



Figure 1. On−Region Characteristics

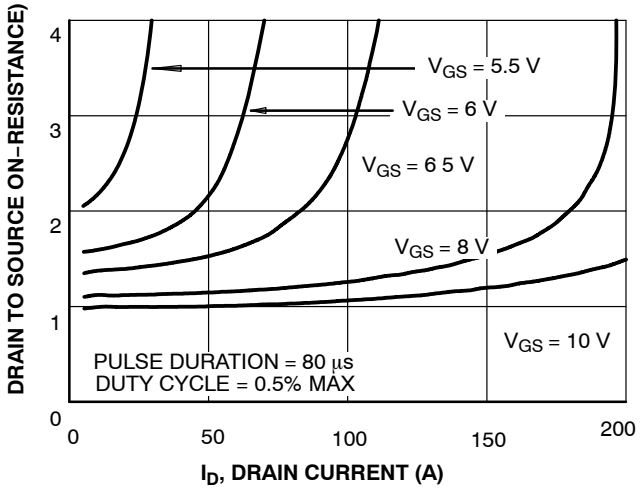



Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

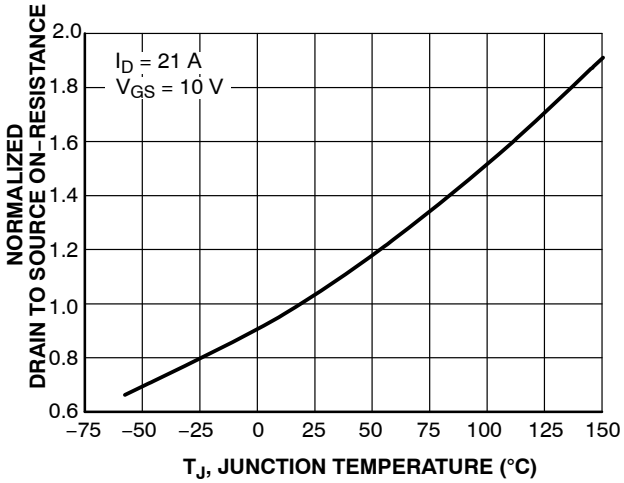



Figure 3. Normalized On−Resistance vs. Junction Temperature

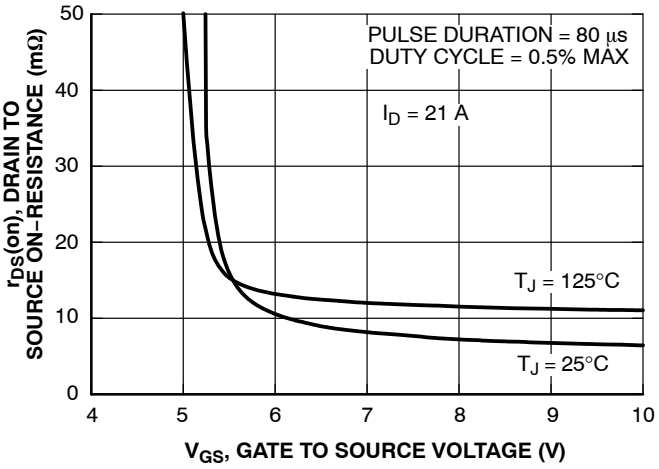



Figure 4. On−Resistance vs. Gate to Source Voltage

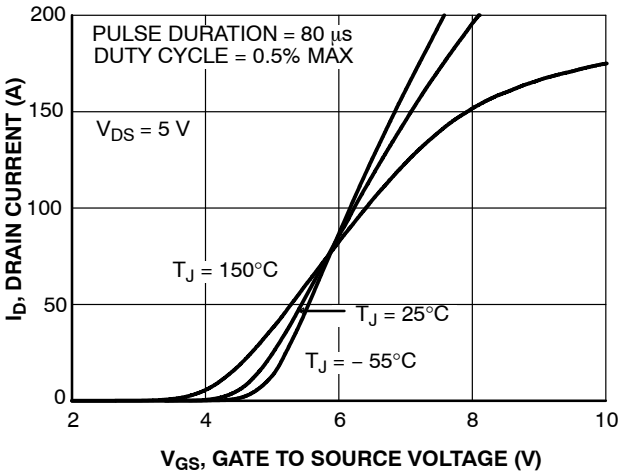



Figure 5. Transfer Characteristics

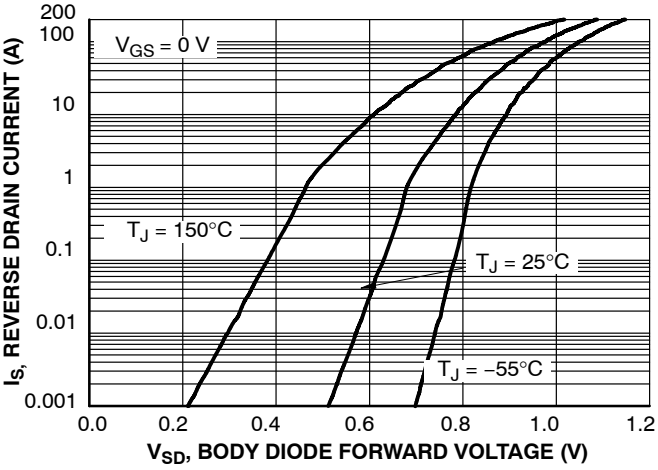



Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

## TYPICAL CHARACTERISTICS (CONTINUED)

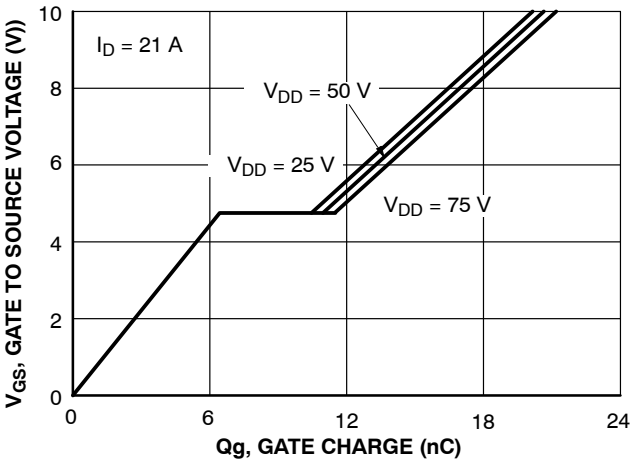



Figure 7. Gate Charge Characteristics

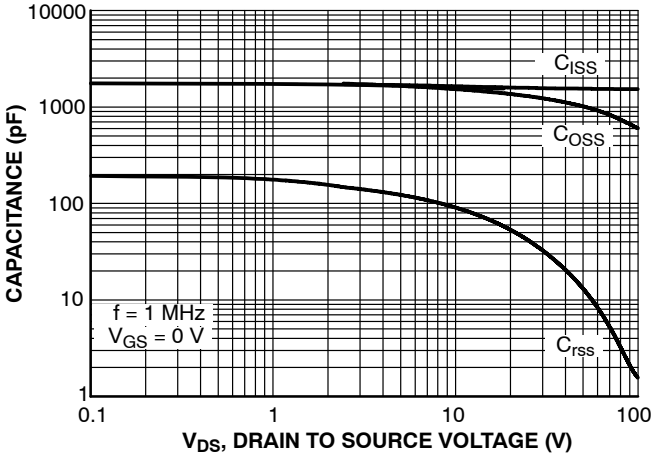



Figure 8. Capacitance vs. Drain to Source Voltage

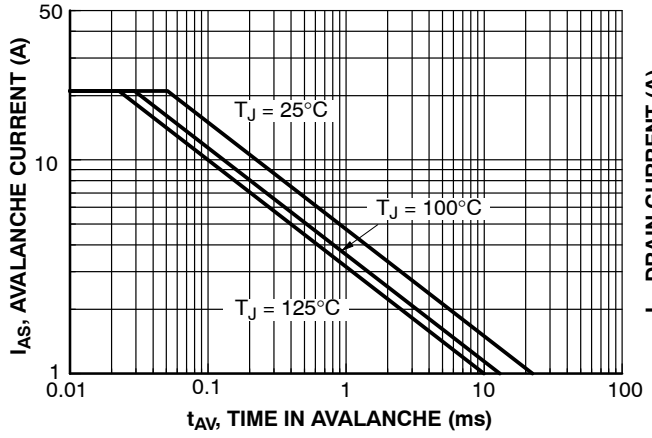



Figure 9. Unclamped Inductive Switching Capability

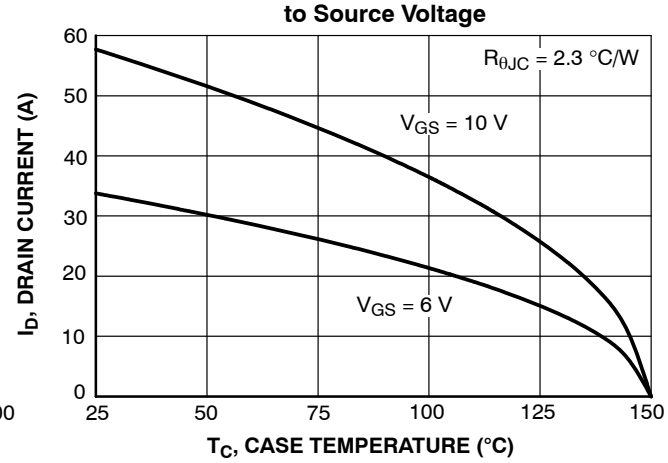



Figure 10. Maximum Continuous Drain Current vs. Case Temperature

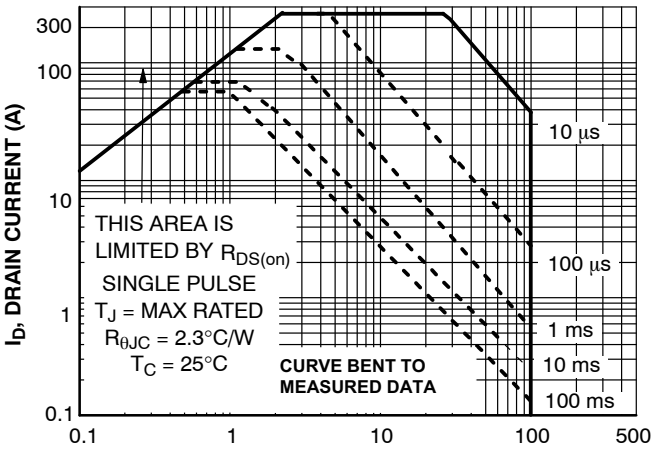



Figure 11. Forward Bias Safe Operating Area

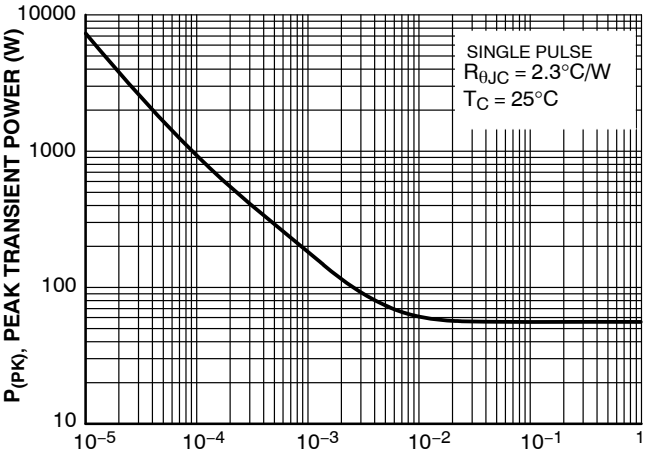



Figure 12. Single Pulse Maximum Power Dissipation

## TYPICAL CHARACTERISTICS (CONTINUED)

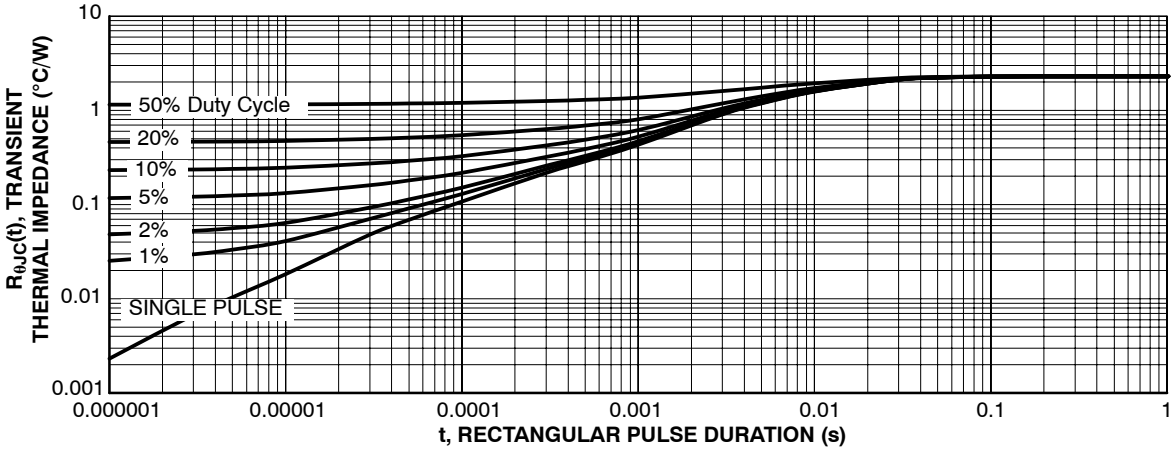
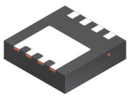
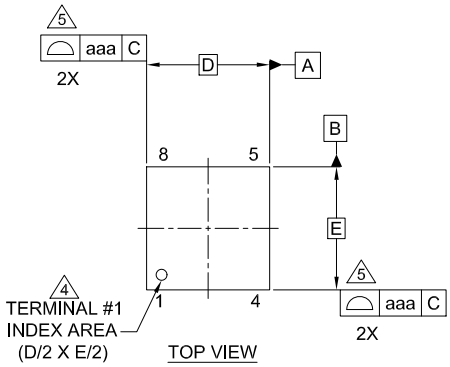


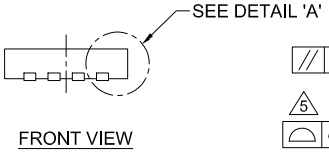

**Figure 13. Junction−to−Case Transient Thermal Response Curve**

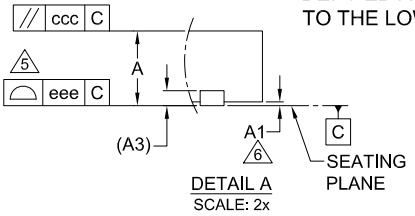


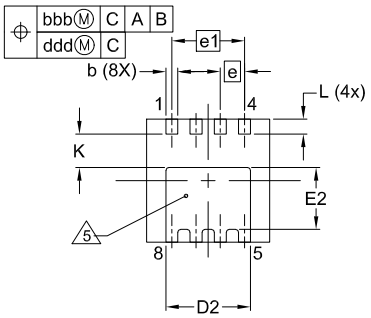
**WDFN8 3.30x3.30x0.75, 0.65P**
CASE 483AW
ISSUE B

DATE 22 MAR 2024



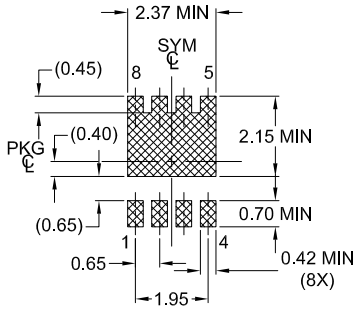




NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | -- | -- | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.27 | 0.32 | 0.37 |
| D | | 3.30 BSC | |
| D2 | 2.17 | 2.27 | 2.37 |
| E | | 3.30 BSC | |
| E2 | 1.56 | 1.66 | 1.76 |
| e | | 0.65 BSC | |
| e1 | | 1.95 BSC | |
| K | 0.90 | -- | -- |
| L | 0.30 | 0.40 | 0.50 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.05 | |

## LAND PATTERN RECOMMENDATION




*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON13672G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **WDFN8 3.30x3.30x0.75, 0.65P** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales