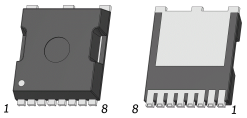
# Silicon Carbide (SiC) Cascode JFET – EliteSiC, Power N-Channel, TOLL, 750 V, 10.7 mohm

# UJ4SC075010L8S



H-PDSO-F8
CASE 740AA

## Description

The UJ4SC075010L8S is a 750 V, 10.7 mΩ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows use of off-the-shelf gate drivers hence requiring minimal redesign when replacing Si IGBTs, Si superjunction devices or SiC MOSFETs. Available in the space-saving H-PDSO-F8 package which enables automated assembly, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

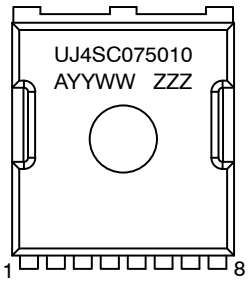
## Features

- On-resistance $R_{DS(on)}$: 10.7 mΩ (Typ)
- Operating Temperature: 175 °C (Max)
- Excellent Reverse Recovery: $Q_{rr}$ = 274 nC
- Low Body Diode $V_{FSD}$: 1.1 V
- Low Gate Charge: $Q_G$ = 75 nC
- Threshold Voltage $V_{G(th)}$: 4.5 V (Typ) Allowing 0 to 15 V Drive
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2
- H-PDSO-F8 Package for Faster Switching, Clean Gate Waveforms
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

## Typical Applications

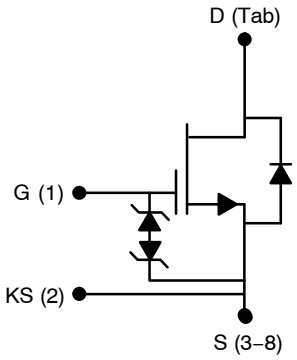
- Solid State Relays and Circuit-Breakers
- Line Rectification and Active-Bridge Rectification Circuits in AC-DC Front-ends
- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating

## MARKING DIAGRAM




| | |
|---|---|
| UJ4SC075010 | = Specific Device Code |
| A | = Assembly Location |
| YY | = Year |
| WW | = Work Week |
| ZZZ | = Lot ID |

## PIN CONNECTIONS




## ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

## MAXIMUM RATINGS

| Parameter | Symbol | Test Conditions | Value | Unit |
|---|---|---|---|---|
| Drain-source Voltage | $V_{DS}$ | | 750 | V |
| Gate-source Voltage | $V_{GS}$ | DC | −20 to +20 | V |
| | | AC (f > 1 Hz) | −25 to +25 | |
| Continuous Drain Current (Note 1) | $I_D$ | $T_C$ < 75 °C | 106 | A |
| | | $T_C$ = 100 °C | 92 | |
| Pulsed Drain Current (Note 2) | $I_{DM}$ | $T_C$ = 25 °C | 300 | A |
| Single Pulsed Avalanche Energy (Note 3) | $E_{AS}$ | L = 15 mH, $I_{AS}$ = 4.5 A | 151 | mJ |
| SiC FET dv/dt Ruggedness | dv/dt | $V_{DS}$ < 500 V | 100 | V/ns |
| Power Dissipation | $P_{tot}$ | $T_C$ = 25 °C | 556 | W |
| Maximum Junction Temperature | $T_{J,max}$ | | 175 | °C |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | | −55 to 175 | °C |
| Reflow Soldering Temperature | $T_{solder}$ | Reflow MSL 1 | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by bondwires.
2. Pulse width $t_p$ limited by $T_{J,max}$
3. Starting $T_J$ = 25 °C

## THERMAL CHARACTERISTICS

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | | – | 0.21 | 0.27 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = +25 °C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **TYPICAL PERFORMANCE – STATIC** | | | | | | |
| Drain-source Breakdown Voltage | $BV_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 750 | – | – | V |
| Total Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = 750 V, $V_{GS}$ = 0 V, $T_J$ = 25 °C | – | 3.5 | 60 | μA |
| | | $V_{DS}$ = 750 V, $V_{GS}$ = 0 V, $T_J$ = 175 °C | – | 45 | – | |
| Total Gate Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $T_J$ = 25 °C, $V_{GS}$ = −20 V / +20 V | – | 2 | 20 | μA |
| Drain-source On-resistance | $R_{DS(on)}$ | $V_{GS}$ = 12 V, $I_D$ = 60 A, $T_J$ = 25 °C | – | 10.7 | 14.2 | mΩ |
| | | $V_{GS}$ = 12 V, $I_D$ = 60 A, $T_J$ = 125 °C | – | 18.1 | – | |
| | | $V_{GS}$ = 12 V, $I_D$ = 60 A, $T_J$ = 175 °C | – | 24 | – | |
| Gate Threshold Voltage | $V_{G(th)}$ | $V_{DS}$ = 5 V, $I_D$ = 10 mA | 3.5 | 4.5 | 5.5 | V |
| Gate Resistance | $R_G$ | f = 1 MHz, open drain | – | 2.3 | – | Ω |
| **TYPICAL PERFORMANCE – REVERSE DIODE** | | | | | | |
| Diode Continuous Forward Current (Note 1) | $I_S$ | $T_C$ < 75 °C | – | – | 106 | A |
| Diode Pulse Current (Note 2) | $I_{S,pulse}$ | $T_C$ = 25 °C | – | – | 300 | A |
| Forward Voltage | $V_{FSD}$ | $V_{GS}$ = 0 V, $I_S$ = 30 A, $T_J$ = 25 °C | – | 1.1 | 1.24 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 30 A, $T_J$ = 175 °C | – | 1.2 | – | |
| Reverse Recovery Charge | $Q_{rr}$ | $V_{DS}$ = 400 V, $I_S$ = 60 A, $V_{GS}$ = 0 V, $R_G$ = 30 Ω, di/dt = 2500 A/μs, $T_J$ = 25 °C | – | 274 | – | nC |
| Reverse Recovery Time | $t_{rr}$ | | – | 18.5 | – | ns |
| Reverse Recovery Charge | $Q_{rr}$ | $V_{DS}$ = 400 V, $I_S$ = 60 A, $V_{GS}$ = 0 V, $R_G$ = 30 Ω, di/dt = 2500 A/μs, $T_J$ = 150 °C | – | 290 | – | nC |
| Reverse Recovery Time | $t_{rr}$ | | – | 20 | – | ns |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = +25 °C unless otherwise specified) (continued)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **TYPICAL PERFORMANCE – DYNAMIC** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V, f = 100 kHz | – | 3245 | – | pF |
| Output Capacitance | $C_{oss}$ | | – | 178 | – | |
| Reverse Transfer Capacitance | $C_{rss}$ | | – | 1.2 | – | |
| Effective Output Capacitance, Energy Related | $C_{oss(er)}$ | $V_{DS}$ = 0 V to 400 V, $V_{GS}$ = 0 V | – | 225 | – | pF |
| Effective Output Capacitance, Time Related | $C_{oss(tr)}$ | $V_{DS}$ = 0 V to 400 V, $V_{GS}$ = 0 V | – | 470 | – | pF |
| $C_{OSS}$ Stored Energy | $E_{oss}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V | – | 18 | – | μJ |
| Total gate Charge | $Q_G$ | $V_{DS}$ = 400 V, $I_D$ = 60 A, $V_{GS}$ = 0 V to 15 V | – | 75 | – | nC |
| Gate-drain Charge | $Q_{GD}$ | | – | 13 | – | |
| Gate-source Charge | $Q_{GS}$ | | – | 22 | – | |
| Turn-on Delay Time | $t_{d(on)}$ | (Note 4) and (Note 5) $V_{DS}$ = 400 V, $I_D$ = 60 A, Gate Driver = 0 V to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 5 Ω Inductive Load, FWD: same device with $V_{GS}$ = 0 V, $R_G$ = 5 Ω and RC snubber: $R_S$ = 5 Ω and $C_S$ = 440 pF, $T_J$ = 25 °C | – | 17.6 | – | ns |
| Rise Time | $t_r$ | | – | 22.4 | – | |
| Turn-off Delay Time | $t_{d(off)}$ | | – | 65 | – | |
| Fall Time | $t_f$ | | – | 12.8 | – | |
| Turn-on Energy Including RS Energy | $E_{ON}$ | | – | 173 | – | μJ |
| Turn-off Energy Including RS Energy | $E_{OFF}$ | | – | 132 | – | |
| Total Switching Energy | $E_{TOTAL}$ | | – | 305 | – | |
| Snubber $R_S$ Energy During Turn-on | $E_{RS\_ON}$ | | – | 11 | – | μJ |
| Snubber $R_S$ Energy During Turn-off | $E_{RS\_OFF}$ | | – | 37 | – | |
| Turn-on Delay Time | $t_{d(on)}$ | (Note 4) and (Note 5) $V_{DS}$ = 400 V, $I_D$ = 60 A, Gate Driver = 0 V to +15 V, Turn-on $R_{G,EXT}$ = 1 Ω, Turn-off $R_{G,EXT}$ = 5 Ω Inductive Load, FWD: same device with $V_{GS}$ = 0 V, $R_G$ = 5 Ω and RC snubber: $R_S$ = 5 Ω and $C_S$ = 440 pF, $T_J$ = 150 °C | – | 18 | – | ns |
| Rise Time | $t_r$ | | – | 25 | – | |
| Turn-off Delay Time | $t_{d(off)}$ | | – | 68 | – | |
| Fall Time | $t_f$ | | – | 13.6 | – | |
| Turn-on Energy Including RS Energy | $E_{ON}$ | | – | 203 | – | μJ |
| Turn-off Energy Including RS Energy | $E_{OFF}$ | | – | 145 | – | |
| Total Switching Energy | $E_{TOTAL}$ | | – | 348 | – | |
| Snubber $R_S$ Energy During Turn-on | $E_{RS\_ON}$ | | – | 11 | – | μJ |
| Snubber $R_S$ Energy During Turn-off | $E_{RS\_OFF}$ | | – | 37 | – | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Measured with the switching test circuit in Figure 26.
5. In this table, the switching energies (turn-on energy, turn-off energy and total energy) presented include the device RC snubber energy losses.

## TYPICAL PERFORMANCE DIAGRAMS

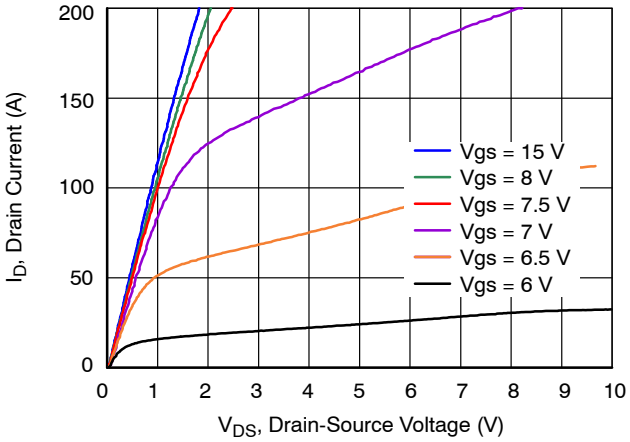



**Figure 1. Typical Output Characteristics at $T_J$ = −55 °C, $t_p$ < 250 μs**

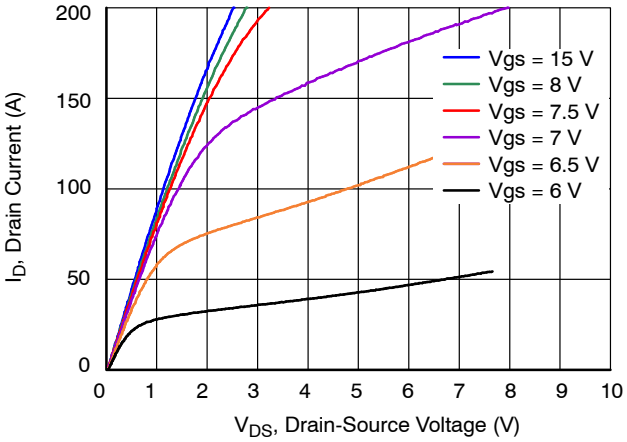



**Figure 2. Typical Output Characteristics at $T_J$ = 25 °C, $t_p$ < 250 μs**

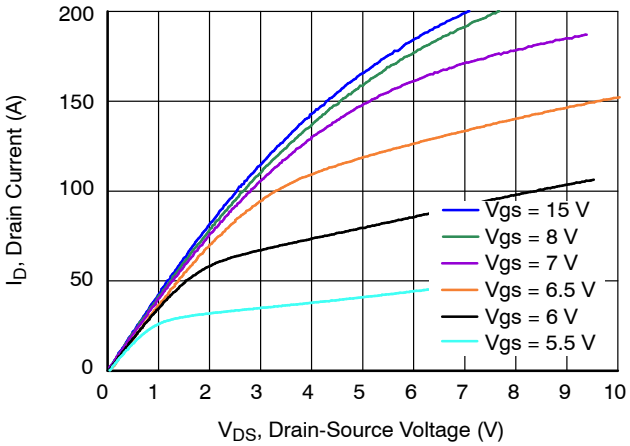



**Figure 3. Typical Output Characteristics at $T_J$ = 175 °C, $t_p$ < 250 μs**

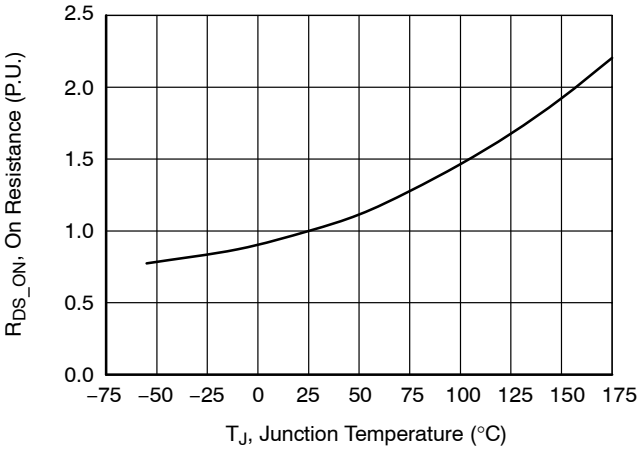



**Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS}$ = 12 V and $I_D$ = 60 A**

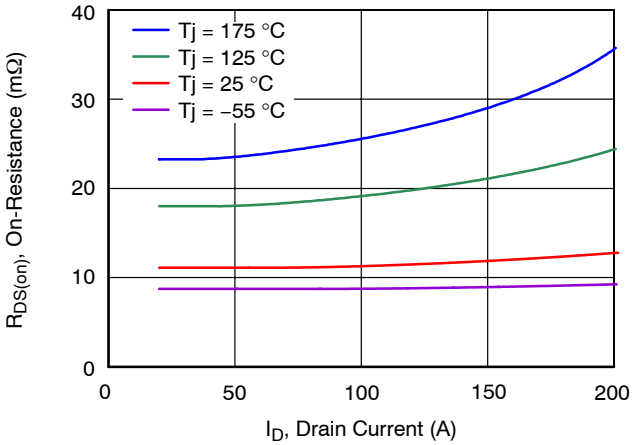



**Figure 5. Typical Drain-Source On-Resistances at $V_{GS}$ = 12 V**

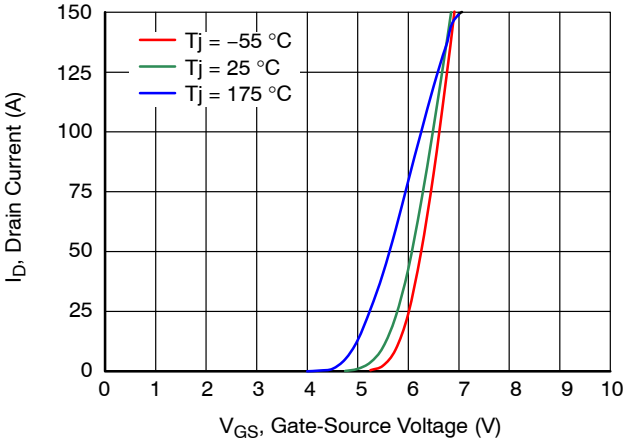



**Figure 6. Typical Transfer Characteristics at $V_{DS}$ = 5 V**

## TYPICAL PERFORMANCE DIAGRAMS (continued)

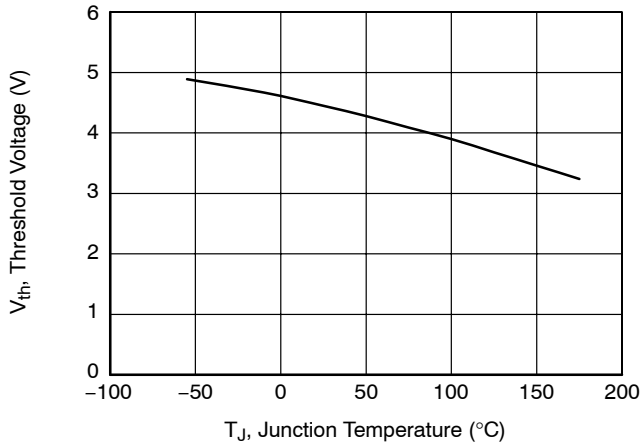



**Figure 7. Threshold Voltage vs. Junction Temperature at $V_{DS}$ = 5 V and $I_D$ = 10 mA**

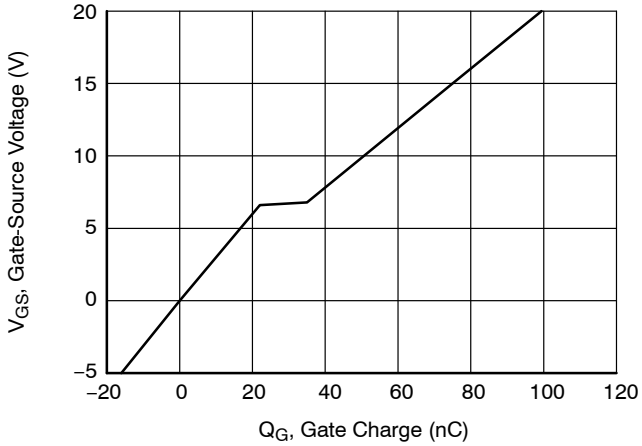



**Figure 8. Typical Gate Charge at $V_{DS}$ = 400 V and $I_D$ = 60 A**

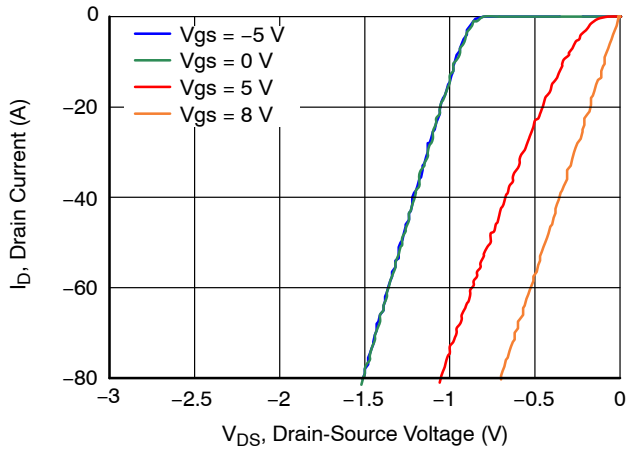



**Figure 9. 3rd Quadrant Characteristics at $T_J$ = −55 °C**

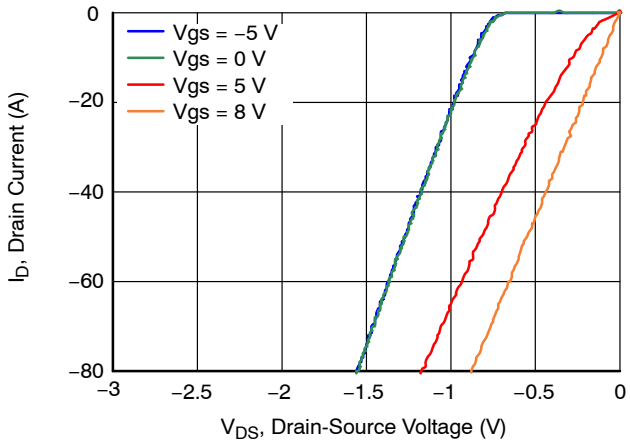



**Figure 10. 3rd Quadrant Characteristics at $T_J$ = 25 °C**

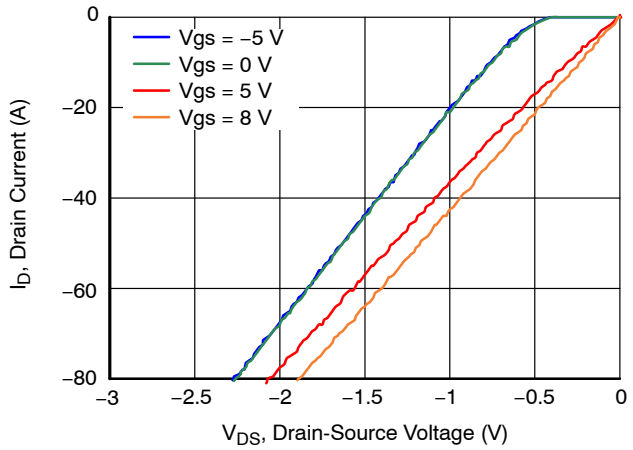



**Figure 11. 3rd Quadrant Characteristics at $T_J$ = 175 °C**

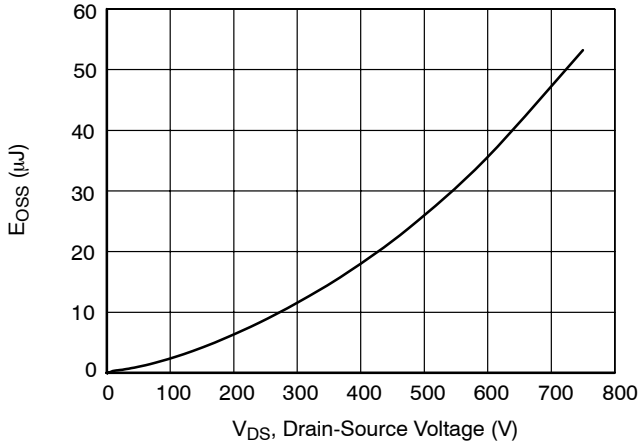



**Figure 12. Typical Stored Energy in $C_{OSS}$ at $V_{GS}$ = 0 V**

## TYPICAL PERFORMANCE DIAGRAMS (continued)

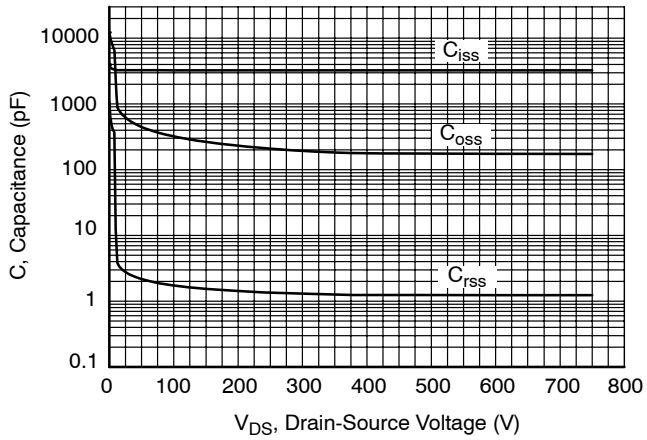



**Figure 13. Typical Capacitances at f = 100 kHz and $V_{GS}$ = 0 V**

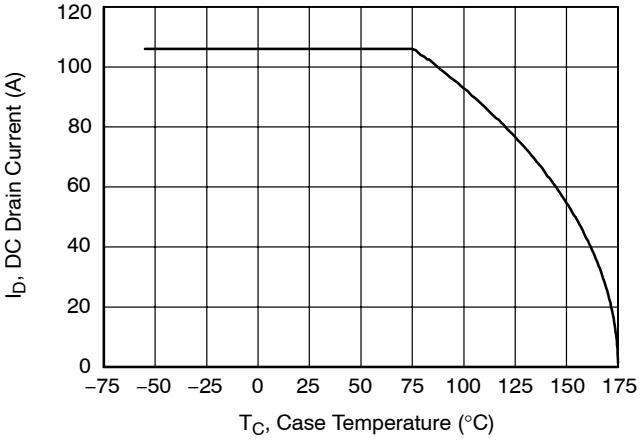



**Figure 14. DC Drain Current Derating**

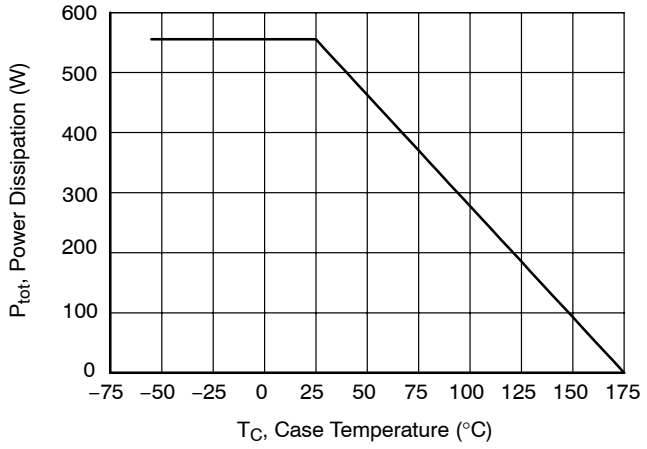



**Figure 15. Total Power Dissipation**

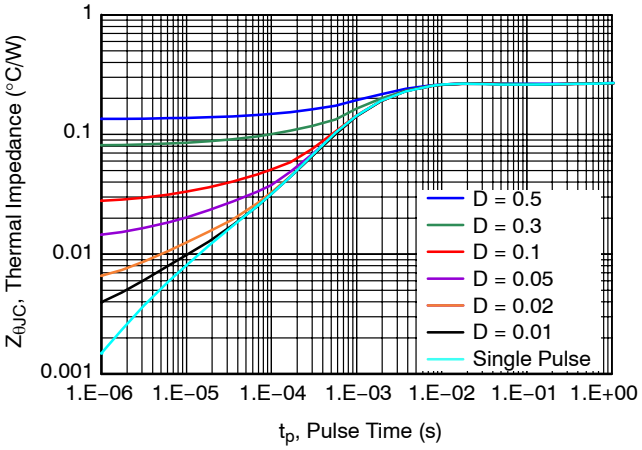



**Figure 16. Maximum Transient Thermal Impedance**

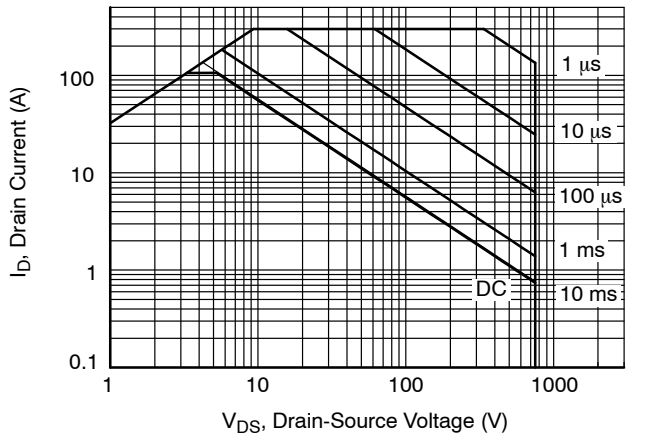



**Figure 17. Safe Operation Area at $T_C$ = 25 °C, D = 0, Parameter $t_p$**

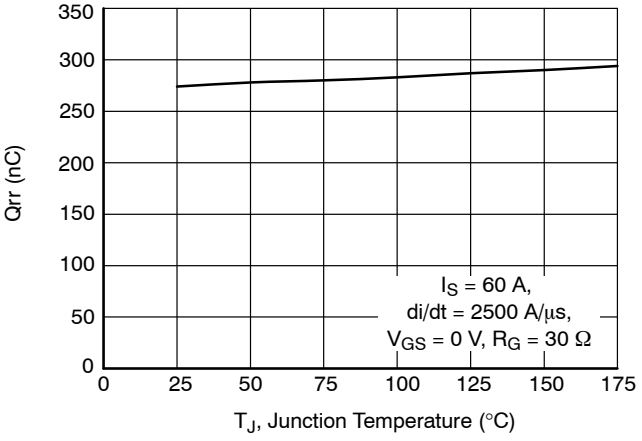



**Figure 18. Reverse Recovery Charge Qrr vs. Junction Temperature at $V_{DS}$ = 400 V**

## TYPICAL PERFORMANCE DIAGRAMS (continued)

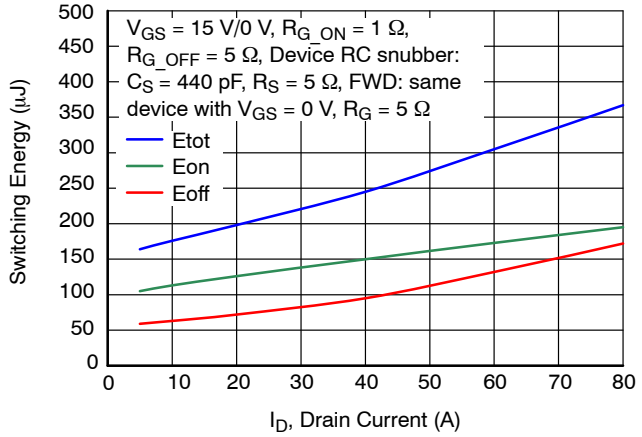



**Figure 19. Clamped Inductive Switching Energy vs. Drain Current at $V_{DS}$ = 400 V and $T_J$ = 25 °C**

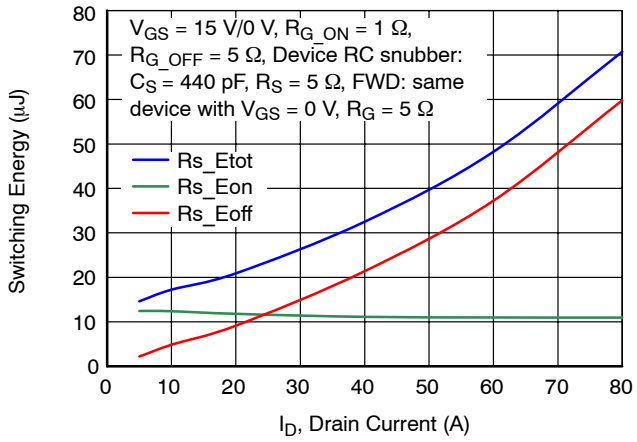



**Figure 20. RC Snubber Energy Loss vs. Drain Current at $V_{DS}$ = 400 V and $T_J$ = 25 °C**

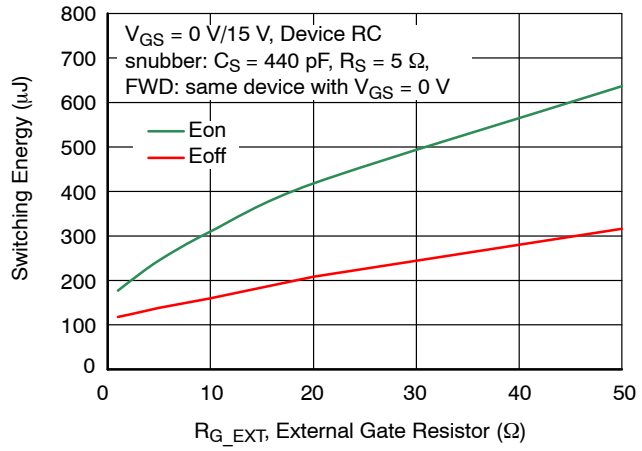



**Figure 21. Clamped Inductive Switching Energy vs. $R_{G\_EXT}$ at $V_{DS}$ = 400 V, $I_D$ = 60 A, and $T_J$ = 25 °C**

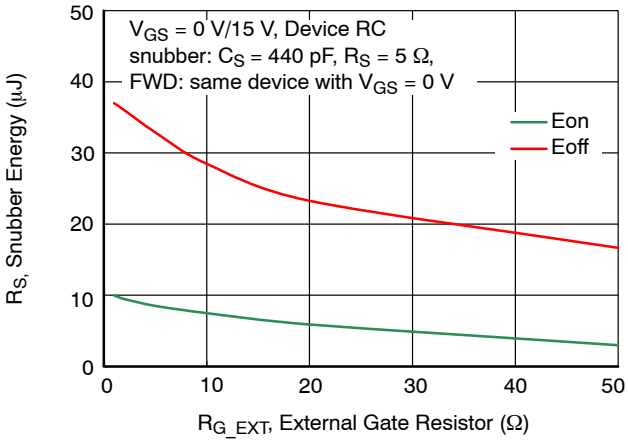



**Figure 22. RC Snubber Energy Losses vs. $R_{G\_EXT}$ at $V_{DS}$ = 400 V, $I_D$ = 60 A, and $T_J$ = 25 °C**

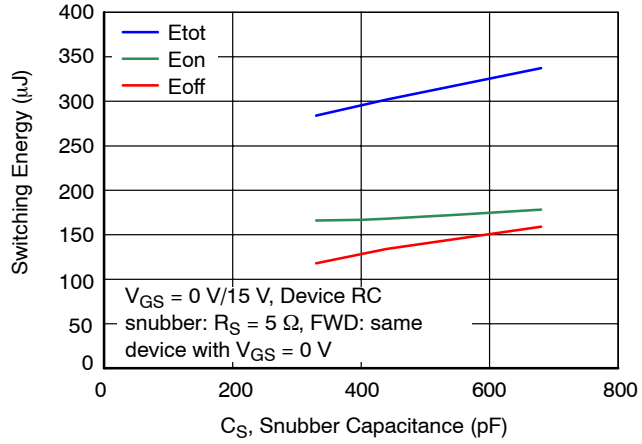



**Figure 23. Clamped Inductive Switching Energy vs. Snubber Capacitance Cs at $V_{DS}$ = 400 V, $I_D$ = 60 A, and $T_J$ = 25 °C**

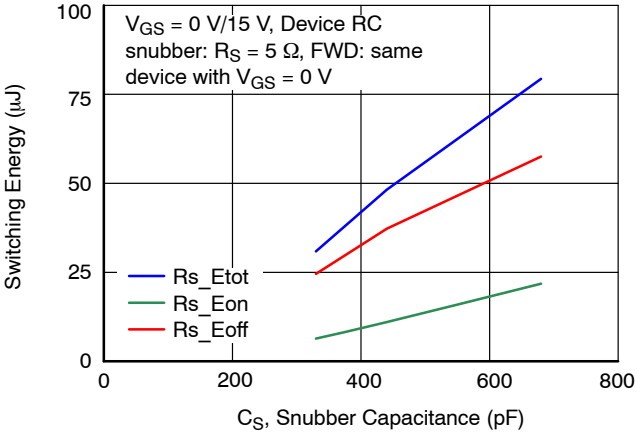



**Figure 24. RC Snubber Energy Loss vs. Snubber Capacitance Cs at $V_{DS}$ = 400 V, $I_D$ = 60 A, and $T_J$ = 25 °C**

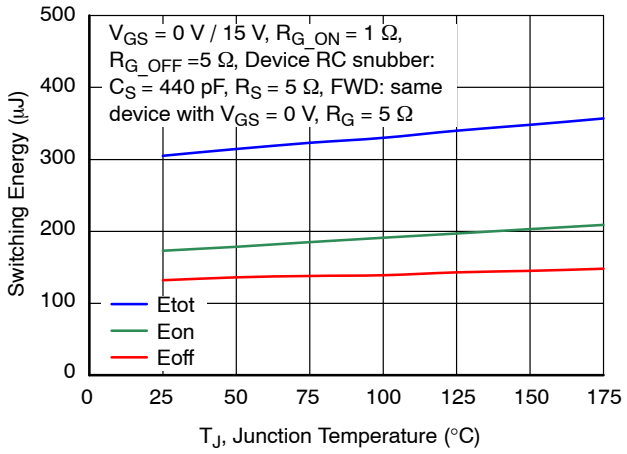



**Figure 25. Clamped Inductive Switching Energies vs. Junction Temperature $T_J$ at $V_{DS}$ = 400 V and $I_D$ = 60 A**

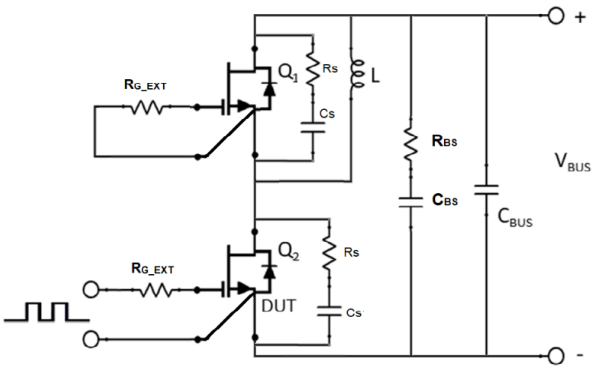



**Figure 26. Schematic of the Half-Bridge Mode Switching Test Circuit. Note, Device Snubber (Rs = 5 Ω, Cs = 440 pF) and Bus RC Snubber ($R_{BS}$ = 1 Ω, $C_{BS}$ = 100 nF) is Used to Reduce the Power Loop High Frequency Oscillations**

## APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance ($C_{oss}$), gate charge ($Q_G$), and reverse recovery charge ($Q_{rr}$) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti−parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com.

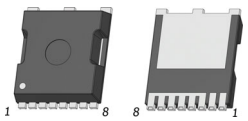
### ORDERING INFORMATION

| Part Number | Marking | Package | Shipping† |
|---|---|---|---|
| UJ4SC075010L8S | UJ4SC075010 | H-PDSO-F8<br>(Pb-Free, Halogen Free) | 2000 / Tape and Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| C | Acquired the original Qorvo JFET Division Data Sheet and updated the main document title to comply with **onsemi** standards for SiC products. | 1/15/2025 |
| 3 | Converted the Data Sheet to **onsemi** format. | 6/12/2025 |



**H−PDSO−F8 9.90x10.38x2.30, 1.20P**
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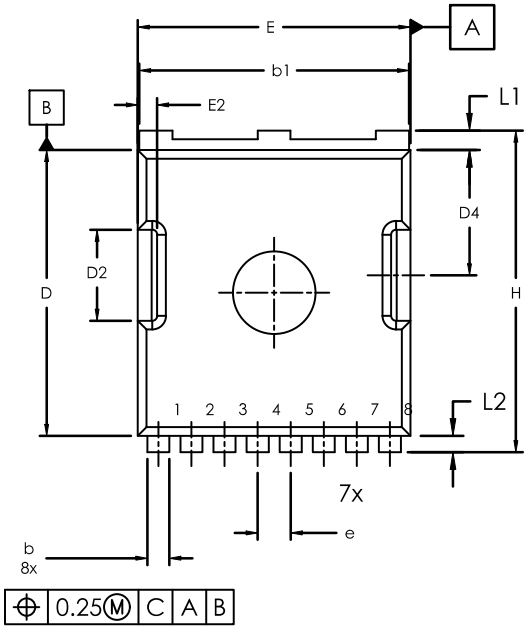


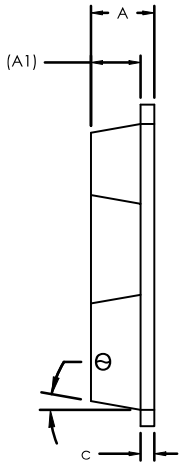


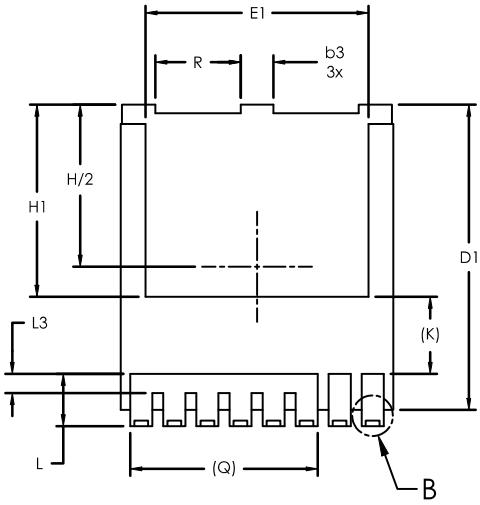


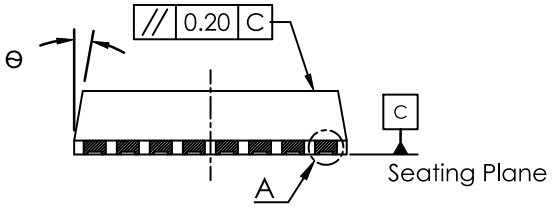


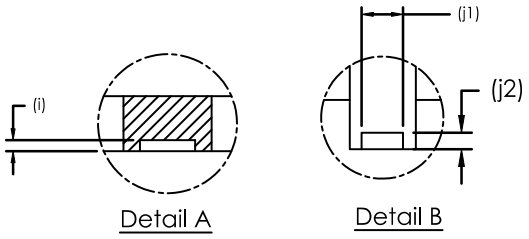


Note:
1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Dimensions does not include Burrs and Mold Flashes

| TO-LL | | | |
|---|---|---|---|
| SYMBOL | Value | | |
| | Min | Nom | Max |
| A | 2.15 | 2.30 | 2.45 |
| A1 | | 1.80 REF | |
| b | 0.65 | 0.80 | 0.90 |
| b1 | 9.65 | 9.80 | 9.95 |
| b3 | 1.10 | 1.20 | 1.30 |
| c | 0.40 | 0.50 | 0.60 |
| D | 10.18 | 10.38 | 10.58 |
| D1 | 10.88 | 11.08 | 11.28 |
| D2 | 3.15 | 3.30 | 3.45 |
| D4 | 4.40 | 4.55 | 4.70 |
| E | 9.70 | 9.90 | 10.10 |
| E1 | 7.95 | 8.10 | 8.25 |
| E2 | 0.60 | 0.70 | 0.80 |
| e | | 1.20 BSC | |
| H | 11.48 | 11.68 | 11.88 |
| H1 | 6.80 | 6.95 | 7.10 |
| i | | 0.10 REF | |
| j1 | | 0.46 REF | |
| j2 | | 0.20 REF | |
| K | | 2.80 REF | |
| L | 1.40 | 1.90 | 2.10 |
| L1 | 0.50 | 0.70 | 0.90 |
| L2 | 0.48 | 0.60 | 0.72 |
| L3 | 0.30 | 0.70 | 0.80 |
| Q | | 6.80 REF | |
| R | 3.00 | 3.10 | 3.20 |
| θ | | 10° | |

| | | | |
|---|---|---|---|
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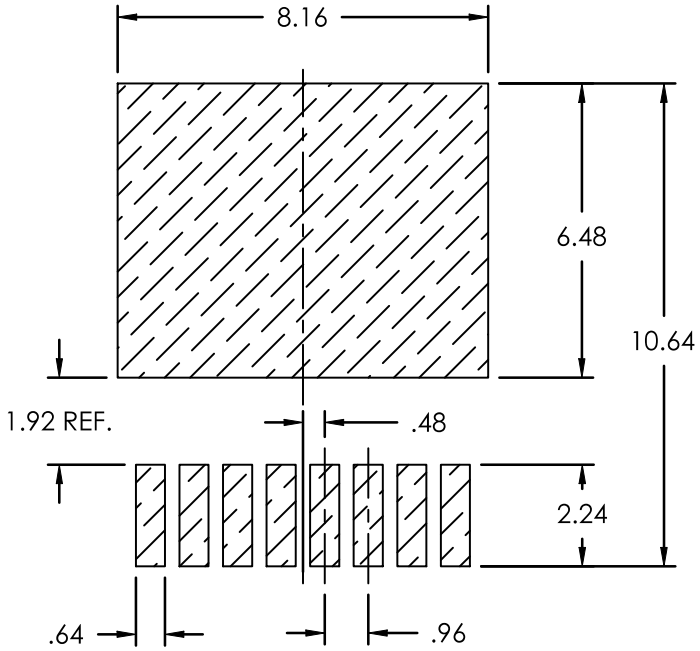
## RECOMMENDED PCB LAND PATTERN




NOTE: LAND PATTERN AND THROUGH HOLE DIMENSIONS SERVE ONLY AS AN INITIAL GUIDE.
END-USER PCB DESIGN RULES AND TOLERANCES SHOULD ALWAYS PREVAIL.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98AON26704H** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **H−PDSO−F8 9.90x10.38x2.30, 1.20P** | | **PAGE 2 OF 2** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales