

NCP5181

High Voltage High and Low Side Driver

The NCP5181 is a High Voltage Power MOSFET Driver providing two outputs for direct drive of 2 N-channel power MOSFETs arranged in a half-bridge (or any other high-side + low-side) configuration.

It uses the bootstrap technique to insure a proper drive of the High-side power switch. The driver works with 2 independent inputs to accommodate any topology (including half-bridge, asymmetrical half-bridge, active clamp and full-bridge...).

Features

- High Voltage Range: up to 600 V
- dV/dt Immunity ± 50 V/nsec
- Gate Drive Supply Range from 10 V to 20 V
- High and Low DRV Outputs
- Output Source / Sink Current Capability 1.4 A / 2.2 A
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{CC} Swing on Input Pins
- Matched Propagation Delays between Both Channels
- Outputs in Phase with the Inputs
- Independent Logic Inputs to Accommodate All Topologies
- Under V_{CC} LockOut (UVLO) for Both Channels
- Pin to Pin Compatible with IR2181(S)
- These are Pb-Free Devices

Applications

- High Power Energy Management
- Half-bridge Power Converters
- Any Complementary Drive Converters (asymmetrical half-bridge, active clamp)
- Full-bridge Converters
- Bridge Inverters for UPS Systems

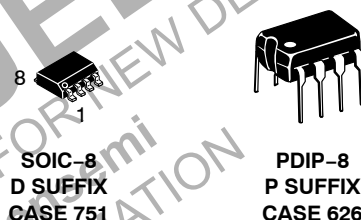
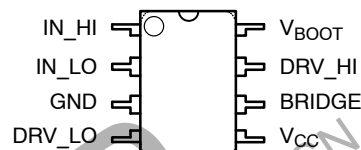
PIN ASSIGNMENT

PIN	FUNCTION
IN_HI	Logic Input for High Side Driver Output In Phase
IN_LO	Logic Input for Low Side Driver Output In Phase
GND	Ground
DRV_LO	Low Side Gate Drive Output
V_{CC}	Low Side and Main Power Supply
V_{BOOT}	Bootstrap Power Supply
DRV_HI	High Side Gate Drive Output
BRIDGE	Bootstrap Return or High Side Floating Supply Return

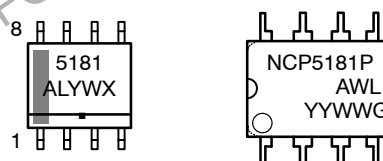


ON Semiconductor®

www.onsemi.com



MARKING DIAGRAMS



NCP5181P,
5181 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5181PG	PDIP-8 (Pb-Free)	50 Units/Tube
NCP5181DR2G	SOIC-8 (Pb-Free)	2,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP5181

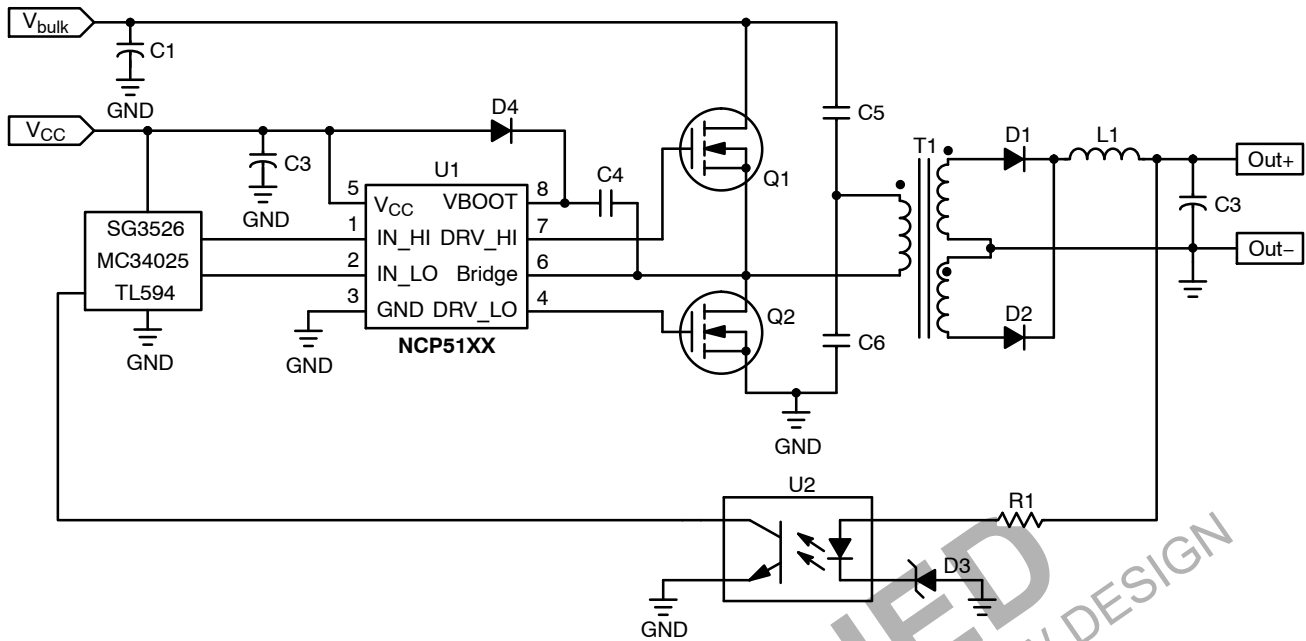


Figure 1. Typical Application

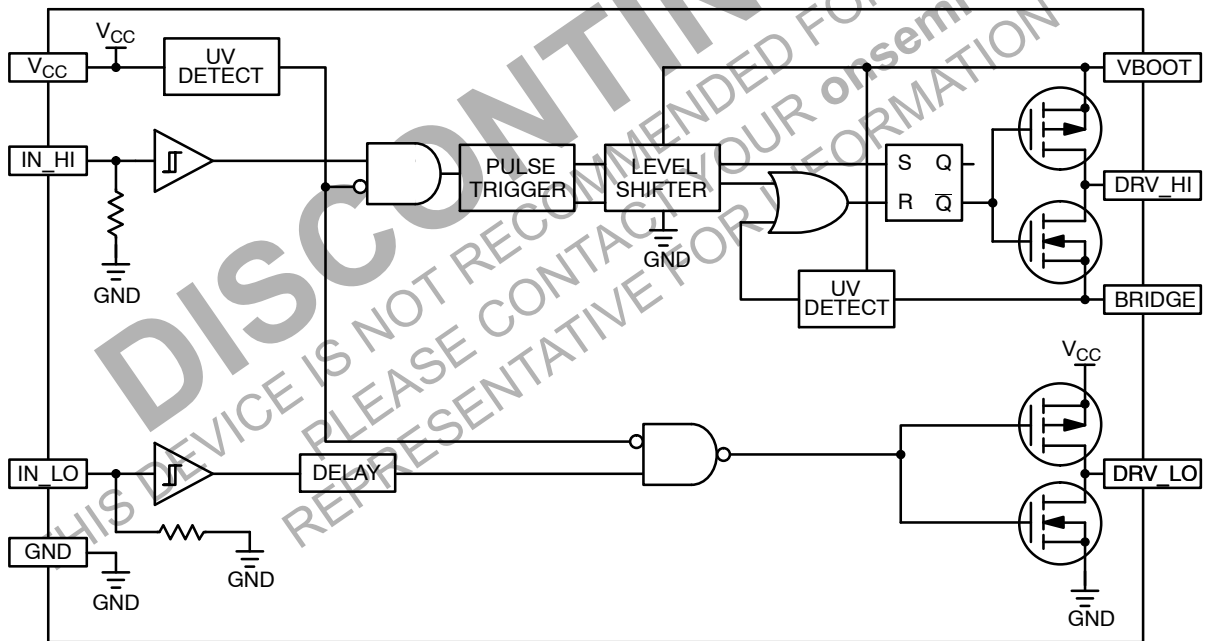


Figure 2. Detailed Block Diagram

NCP5181

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Main Power Supply Voltage	V_{CC}	-0.3 to 20	V
VHV: High Voltage BOOT Pin	V_{BOOT}	-1 to 620	V
VHV: High Voltage BRIDGE Pin	V_{BRIDGE}	-1 to 600	V
VHV: Floating Supply Voltage	$V_{BOOT} - V_{BRIDGE}$	0 to 20	V
VHV: High Side Output Voltage	V_{DRV_HI}	$V_{BRIDGE}-0.3$ to $V_{BOOT}+0.3$	V
Low Side Output Voltage	V_{DRV_LO}	-0.3 to $V_{CC}+0.3$	V
Allowable Output Slew Rate	dV_{BRIDGE}/dt	50	V/ns
Inputs IN_HI, IN_LO	V_{IN_XX}	-1.0 to $V_{CC}+0.3$	V
ESD Capability: Human Body Model (All Pins Except Pins 6-7-8) Machine Model (All Pins Except Pins 6-7-8)		2.0 200	kV V
Latchup Capability per Jedec JESD78			
Power Dissipation and Thermal Characteristics PDIP8: Thermal Resistance, Junction-to-Air SO-8: Thermal Resistance, Junction-to-Air	$R_{\theta JA}$ $R_{\theta JA}$	100 178	°C/W
Maximum Operating Junction Temperature	T_{J_max}	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NCP5181

ELECTRICAL CHARACTERISTICS ($V_{CC} = V_{boot} = 15\text{ V}$, $V_{gnd} = V_{bridge}$, $-40^{\circ}\text{C} < T_A < 125^{\circ}\text{C}$, Outputs loaded with 1 nF)

Rating	Symbol	$T_A -40^{\circ}\text{C to } 125^{\circ}\text{C}$			Units
--------	--------	---	--	--	-------

OUTPUT SECTION

		Min	Typ	Max	
Output High Short Circuit pulsed Current $V_{DRV} = 0\text{ V}$, $PW \leq 10\text{ }\mu\text{s}$, (Note 1)	$I_{DRVhigh}$	–	1.4	–	A
Output Low Short Circuit Pulsed Current $V_{DRV} = V_{CC}$, $PW \leq 10\text{ }\mu\text{s}$, (Note 1)	I_{DRVlow}	–	2.2	–	A
Output Resistor (Typical Value @ 25°C Only) Source	R_{OH}	–	5	12	Ω
Output Resistor (Typical Value @ 25°C Only) Sink	R_{OL}	–	2	8	Ω

DYNAMIC OUTPUT SECTION

Rating	Symbol	Min	Typ	Max	Units
Turn-on Propagation Delay ($V_{bridge} = 0\text{ V}$)	t_{ON}	–	100	170	ns
Turn-off Propagation Delay ($V_{bridge} = 0\text{ V or } 50\text{ V}$) (Note 2)	t_{OFF}	–	100	170	ns
Output Voltage Risetime (from 10% to 90% @ $V_{CC} = 15\text{ V}$) with 1 nF Load	t_r	–	40	60	ns
Output Voltage Falling Edge (from 90% to 10% @ $V_{CC} = 15\text{ V}$) with 1 nF Load	t_f	–	20	40	ns
Propagation Delay Matching between the High Side and the Low Side @ 25°C (Note 3)	Δ_t	–	20	35	ns
Minimum Input Pulse Width that Changes the Output	t_{PW}	–	–	100	ns

INPUT SECTION

Low Level Input Voltage Threshold	V_{IN}	–	–	0.8	V
Input Pulldown Resistor ($V_{IN} < 0.5\text{ V}$)	R_{IN}	–	200	–	k Ω
High Level Input Voltage Threshold	V_{IH}	2.3	–	–	V

SUPPLY SECTION

V_{CC} UV Startup Voltage Threshold	V_{CC_stup}	7.9	8.9	9.8	V
V_{CC} UV Shutdown Voltage Threshold	V_{CC_shtdwn}	7.3	8.2	9.0	V
Hysteresis on V_{CC}	V_{CC_hyst}	0.3	0.7	–	V
V_{boot} Startup Voltage Threshold Reference to Bridge Pin ($V_{boot_stup} = V_{boot} - V_{bridge}$)	V_{boot_stup}	7.9	8.9	9.8	V
V_{boot} UV Shutdown Voltage Threshold	V_{boot_shtdwn}	7.3	8.2	9.0	V
Hysteresis on V_{boot}	V_{boot_shtdwn}	0.3	0.7	–	V
Leakage Current on High Voltage Pins to GND ($V_{BOOT} = V_{BRIDGE} = DRV_HI = 600\text{ V}$)	I_{HV_LEAK}	–	0.5	40	μA
Consumption in Active Mode ($V_{CC} = V_{boot}$, $f_{sw} = 100\text{ kHz}$ and 1 nF Load on Both Driver Outputs)	I_{CC1}	–	4.5	6.5	mA
Consumption in Inhibition Mode ($V_{CC} = V_{boot}$)	I_{CC2}	–	250	400	μA
V_{CC} Current Consumption in Inhibition Mode	I_{CC3}	–	215	–	μA
V_{boot} Current Consumption in Inhibition Mode	I_{CC4}	–	35	–	μA

*Note: see also characterization curves

1. Guaranteed by design.
2. Turn-off propagation delay @ $V_{bridge} = 600\text{ V}$ is guaranteed by design
3. See characterization curve for Δ_t parameters variation on the full range temperature.
4. Timing diagram definition see Figures 4, 5 and 6.

NCP5181

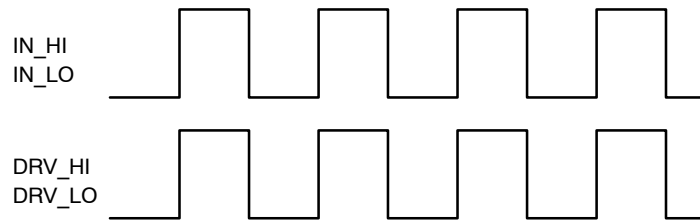


Figure 3. Input/Output Timing Diagram

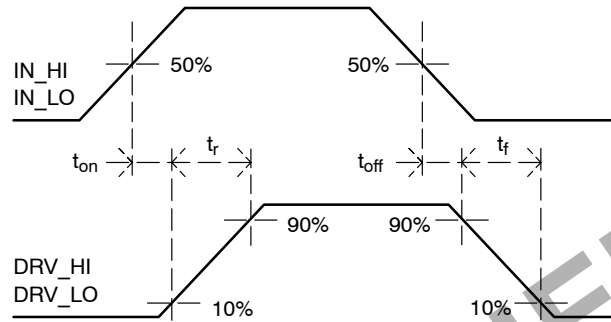


Figure 4. Switching Time Waveform Definitions

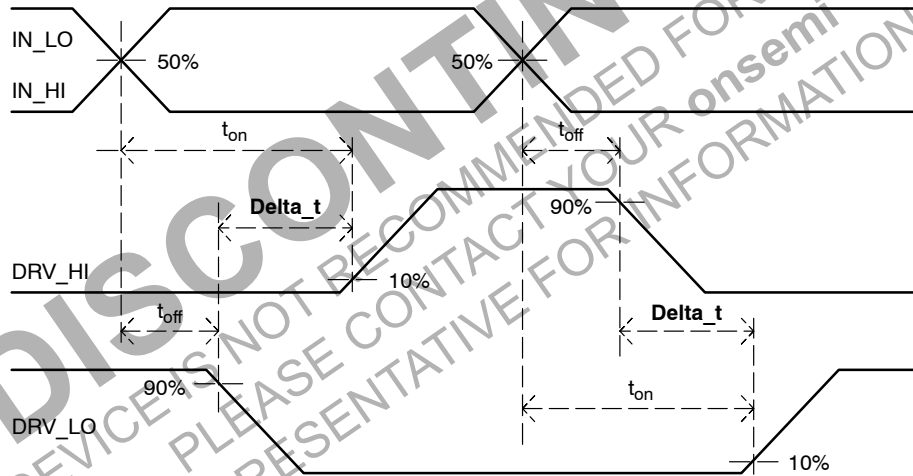


Figure 5. Delay Matching Waveforms Definition

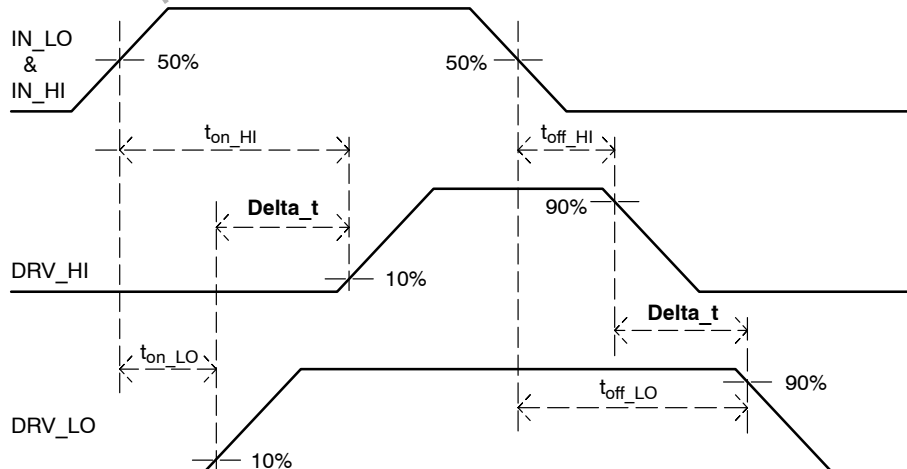


Figure 6. Other Delay Matching Waveforms Definition

TYPICAL CHARACTERISTICS

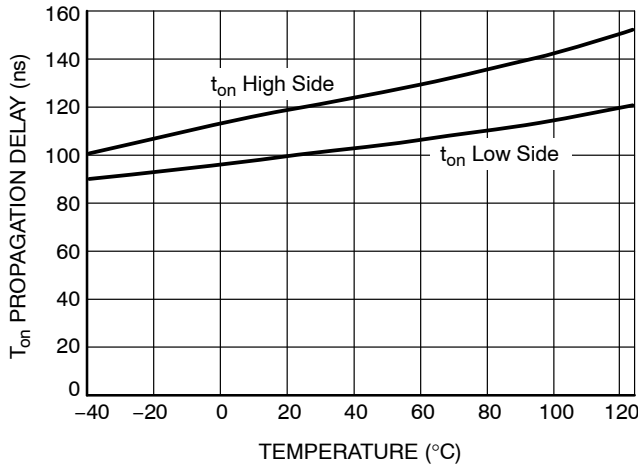


Figure 7. Turn-on Propagation Delay vs. Temperature

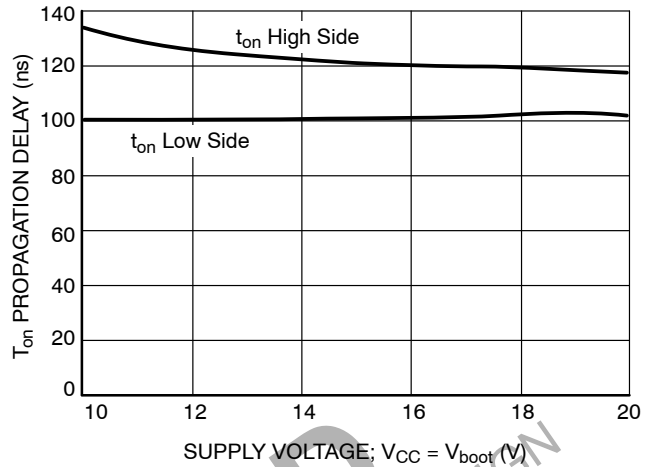


Figure 8. Turn-on Propagation Delay vs. V_{CC} Voltage (V_{CC} = V_{boot})

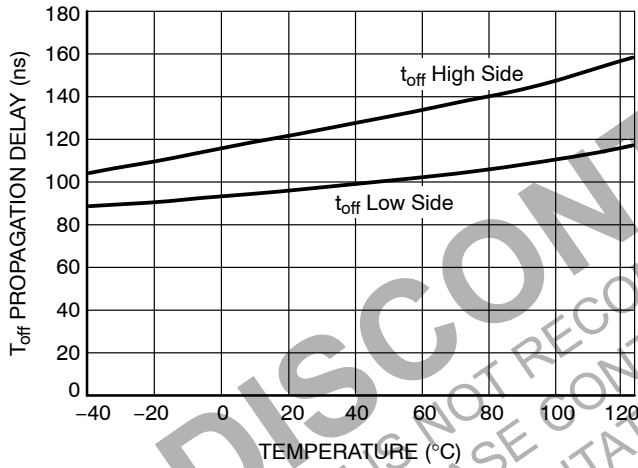


Figure 9. Turn-off Propagation Delay vs. Temperature

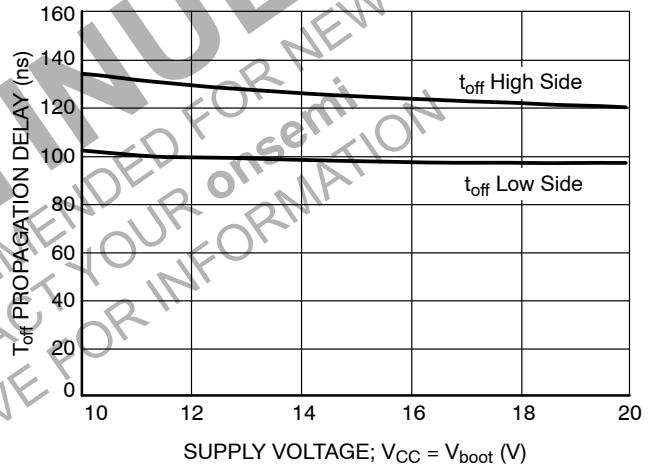


Figure 10. Turn-off Propagation Delay vs. V_{CC} Voltage (V_{CC} = V_{boot})

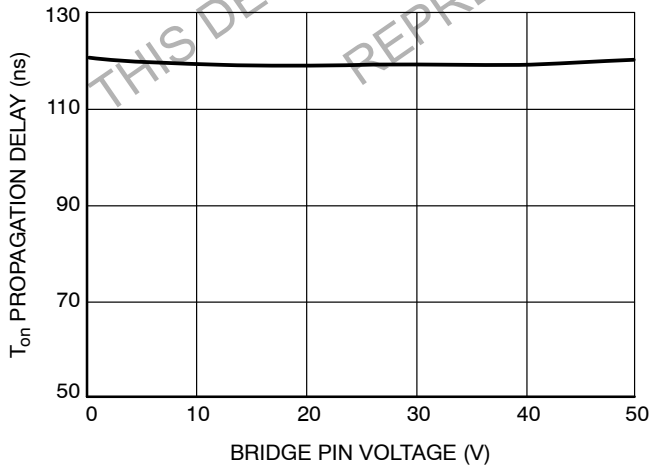


Figure 11. High Side Turn-on Propagation Delay vs. V_{BRIDGE} Voltage

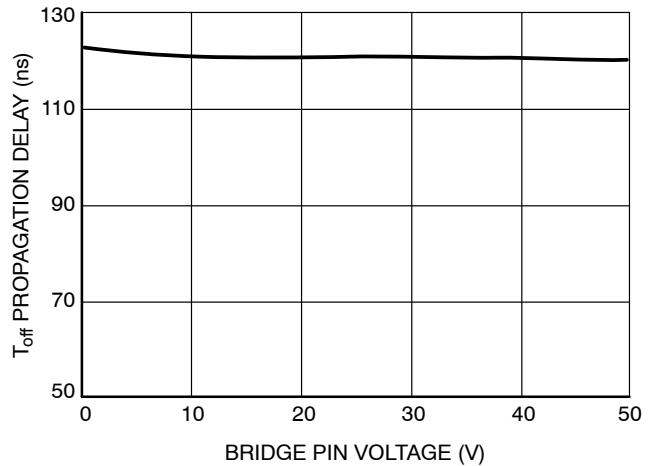


Figure 12. High Side Turn-off Propagation Delay vs. V_{BRIDGE} Voltage

TYPICAL CHARACTERISTICS

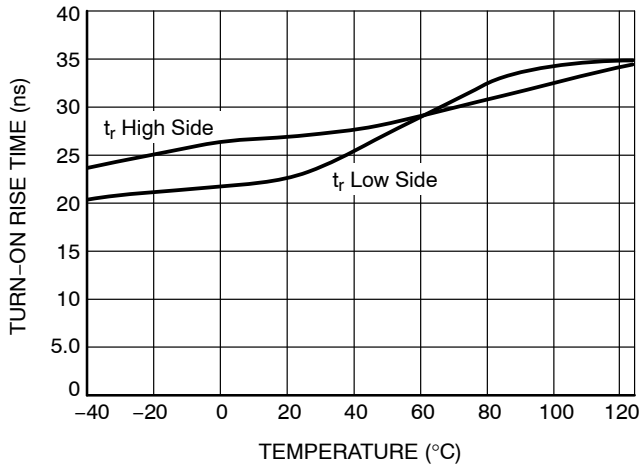


Figure 13. Turn-on Rise Time vs. Temperature

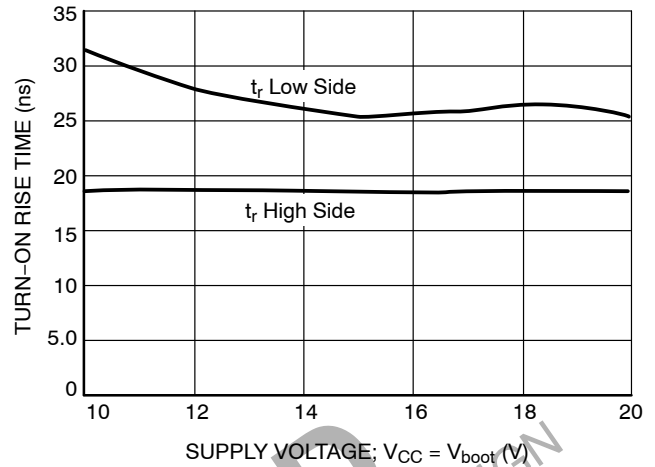


Figure 14. Turn-on Rise Time vs. V_{CC} Voltage ($V_{CC} = V_{boot}$)

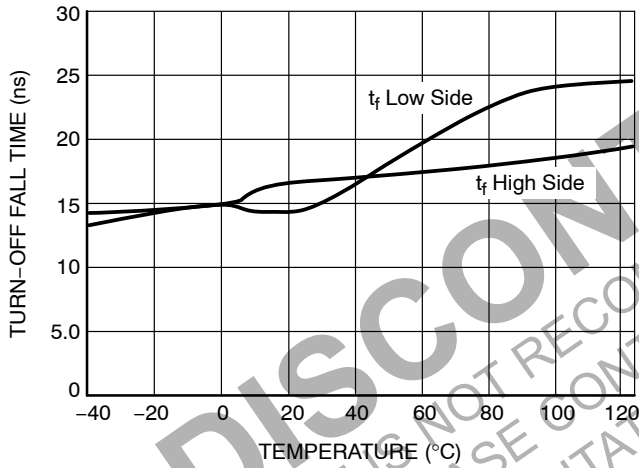


Figure 15. Turn-off Fall Time vs. Temperature

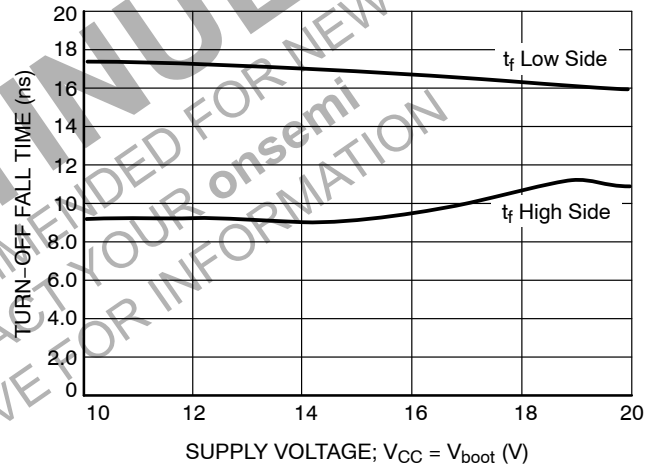


Figure 16. Turn-off Fall Time vs. V_{CC} Voltage ($V_{CC} = V_{boot}$)

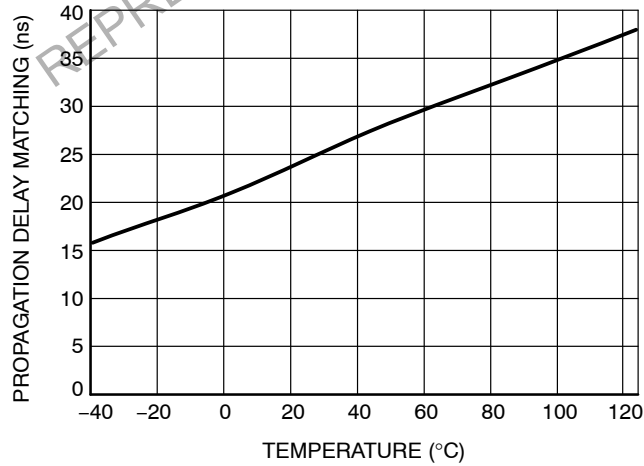


Figure 17. Propagation Delay Matching Between High Side and Low Side Driver

TYPICAL CHARACTERISTICS

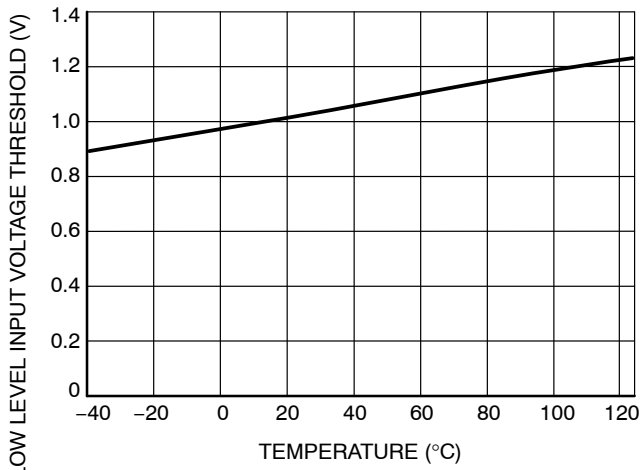


Figure 18. Low Level Input Voltage Threshold vs. Temperature

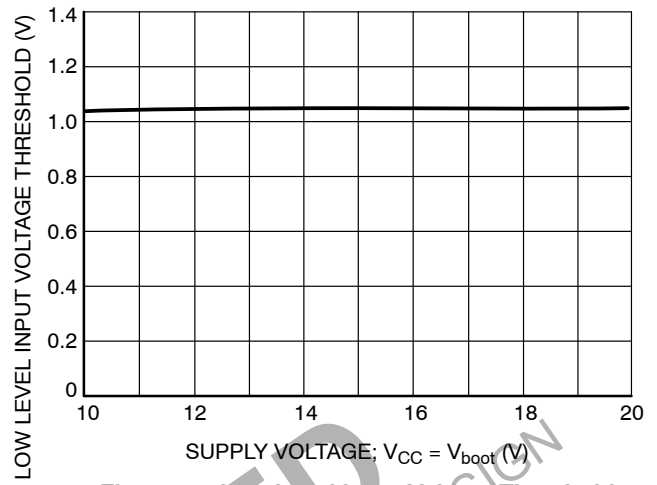


Figure 19. Low Level Input Voltage Threshold vs. V_{CC} Voltage

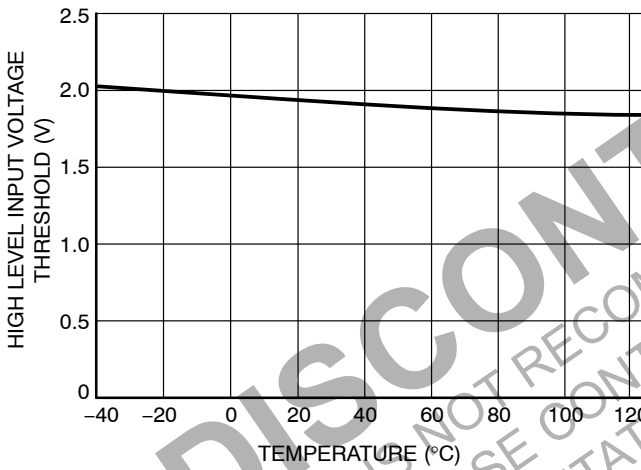


Figure 20. High Level Input Voltage Threshold vs. Temperature

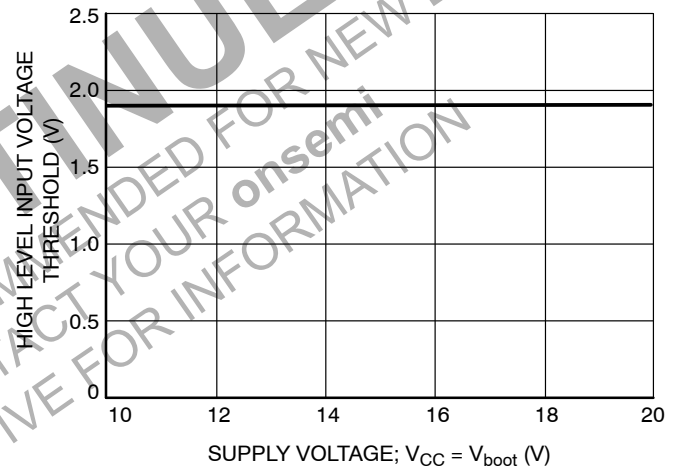


Figure 21. High Level Input Voltage Threshold vs. V_{CC} Voltage

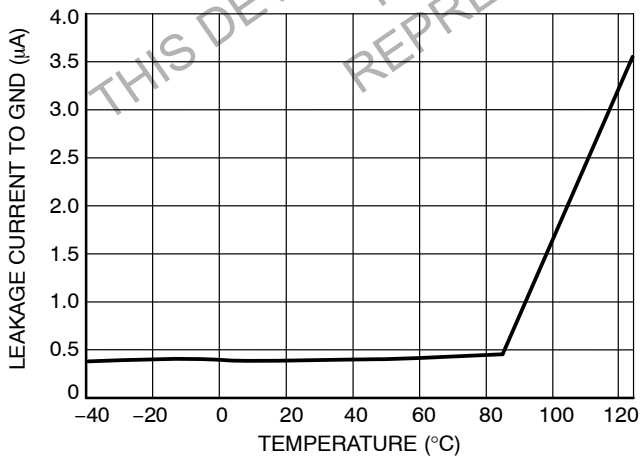


Figure 22. Leakage Current on High Voltage Pins (600 V) to Ground vs. Temperature

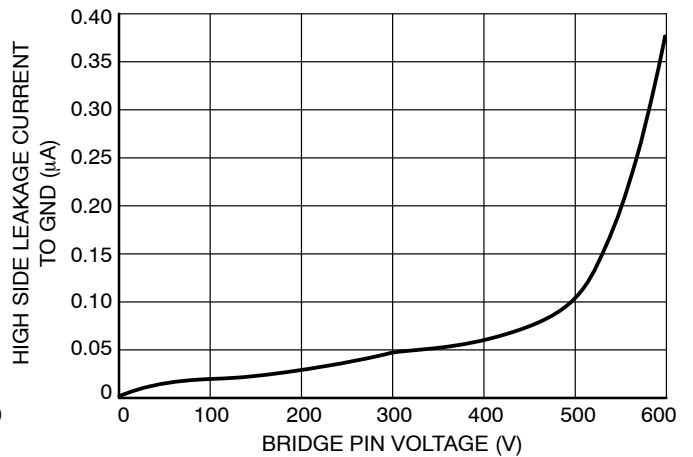


Figure 23. Leakage Current on High Voltage Pins to Ground vs. V_{bridge} Voltage
(V_{bridge} = V_{boot} = V_{DRV_HI})

TYPICAL CHARACTERISTICS

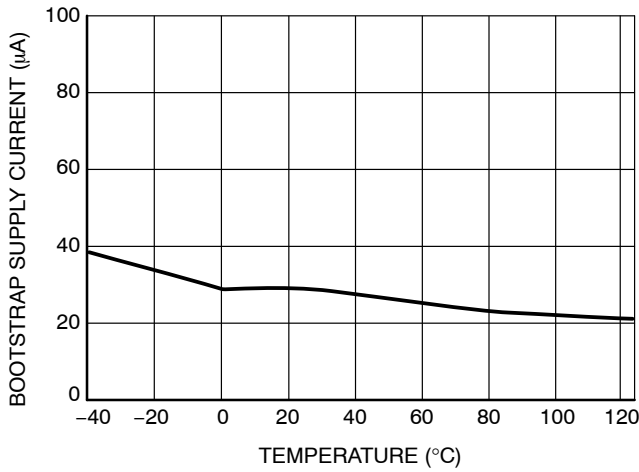


Figure 24. High Side Supply Current vs. Temperature

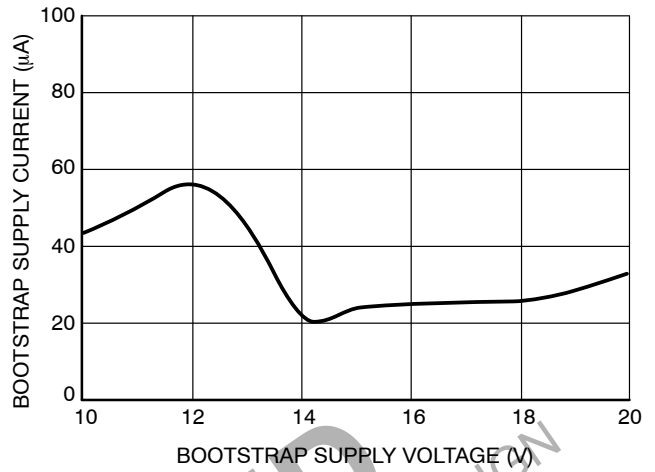


Figure 25. High Side Supply Current vs. Bootstrap Supply Voltage

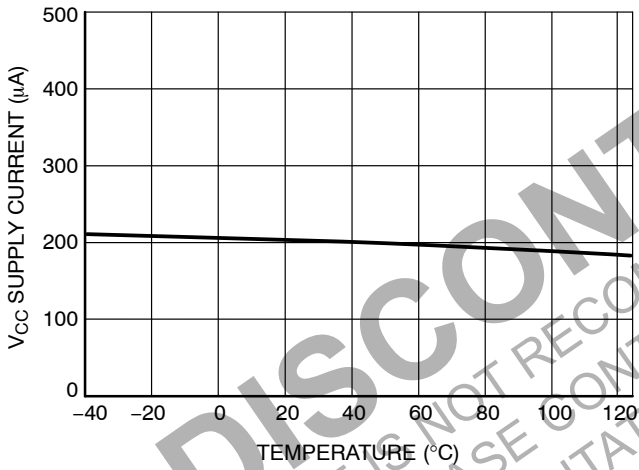


Figure 26. V_{CC} Supply Current vs. Temperature

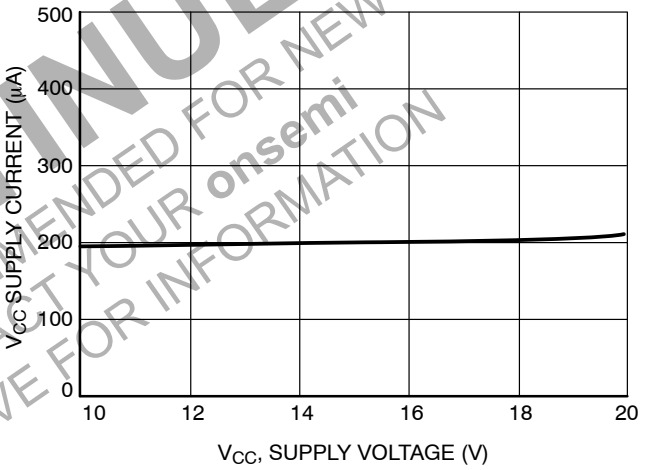


Figure 27. V_{CC} Supply Current vs. V_{CC} Supply Voltage

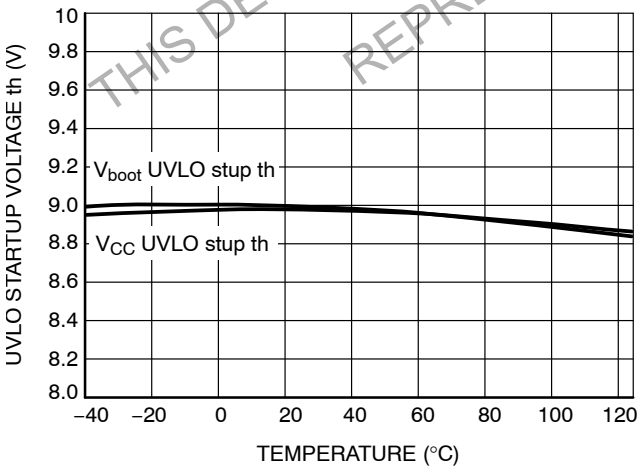


Figure 28. UVLO Start Up Voltage vs. Temperature

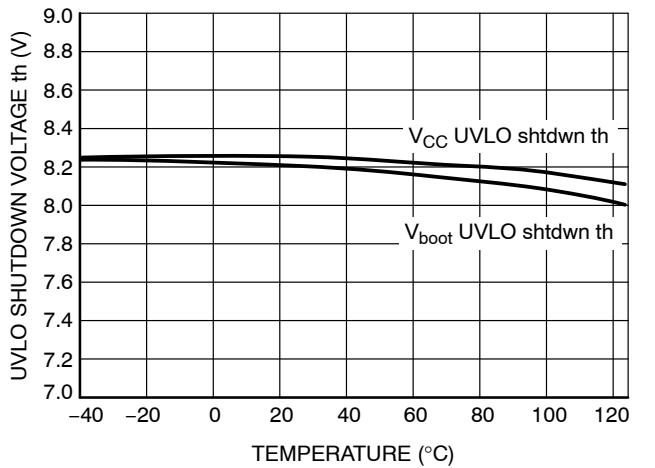


Figure 29. UVLO Shut Down Voltage vs. Bootstrap Supply Voltage

TYPICAL CHARACTERISTICS

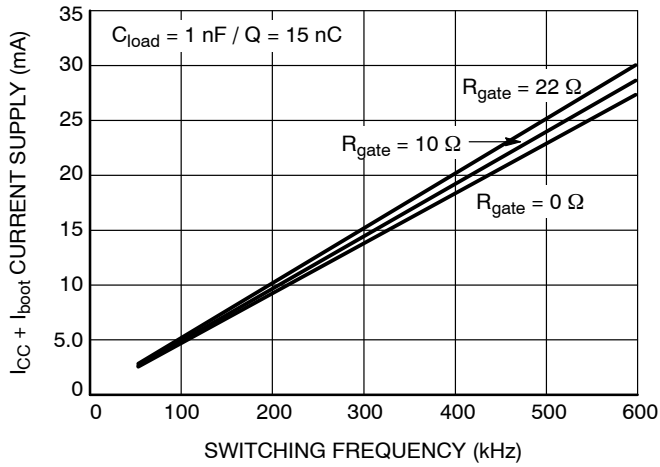


Figure 30. ICC1 Consumption vs. Switching Frequency with 15 nC Load on Each Driver

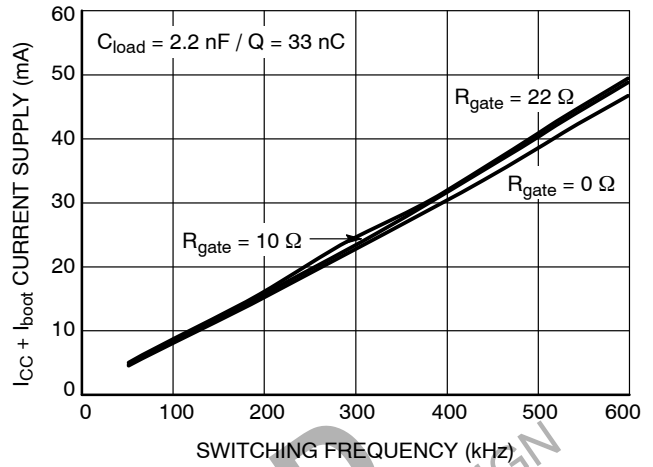


Figure 31. ICC1 Consumption vs. Switching Frequency with 33 nC Load on Each Driver

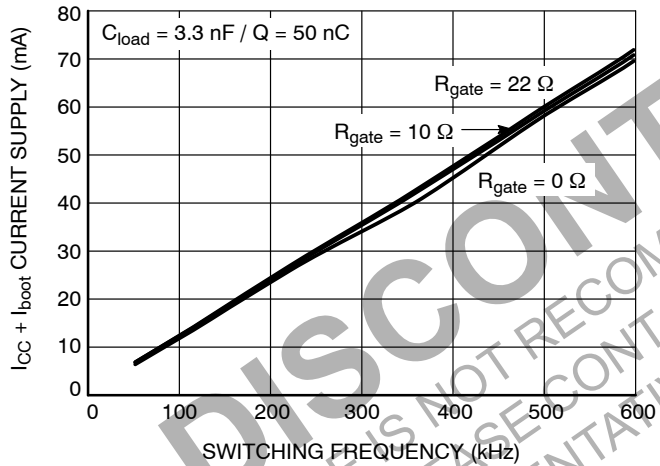


Figure 32. ICC1 Consumption vs. Switching Frequency with 50 nC Load on Each Driver

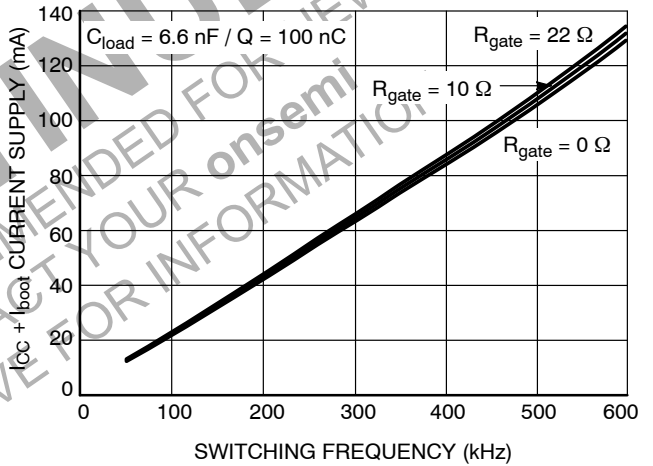


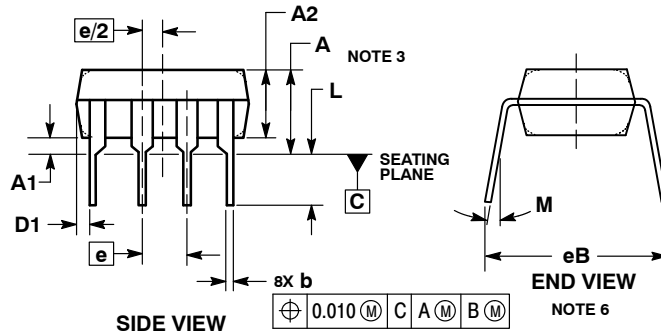
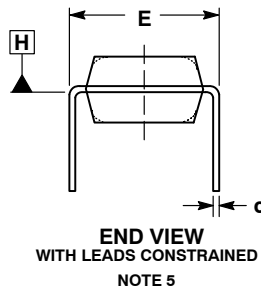
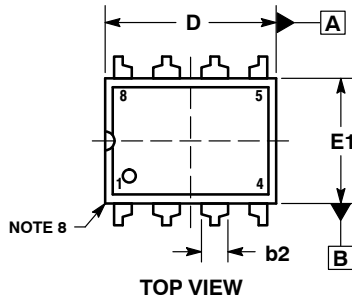
Figure 33. ICC1 Consumption vs. Switching Frequency with 100 nC Load on Each Driver



SCALE 1:1

PDIP-8
CASE 626-05
ISSUE P

DATE 22 APR 2015

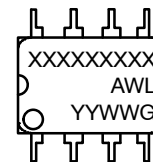


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	0.210	---	5.33
A1	0.015	---	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP	---	1.52 TYP	---
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	---	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC	---	2.54 BSC	---
eB	---	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	---	10°	---	10°

GENERIC
MARKING DIAGRAM*



- XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

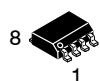
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

- PIN 1. AC IN
2. DC + IN
3. DC - IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

DOCUMENT NUMBER:	98ASB42420B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP-8	PAGE 1 OF 1

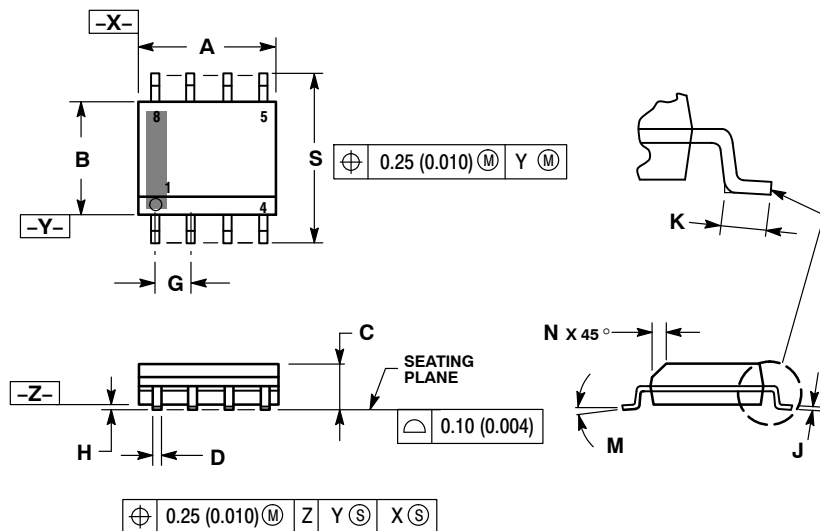
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

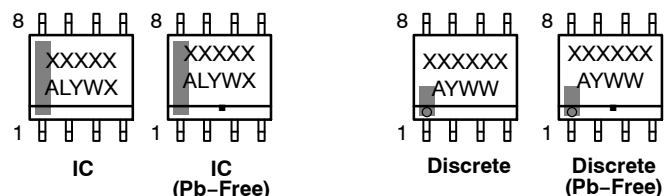
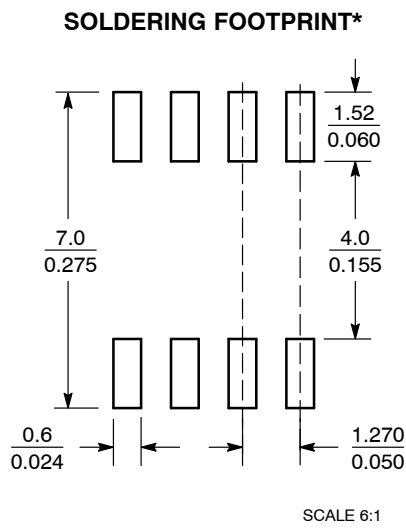
DATE 16 FEB 2011



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*


XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales