

3.3 V/5 V ECL JK Flip-Flop

MC100EP35

Description

The MC100EP35 is a higher speed/low voltage version of the EL35 JK flip-flop. The J/K data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The reset pin is asynchronous and is activated with a logic HIGH.

The 100 Series contains temperature compensation.

Features

- 410 ps Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:
 - ♦ $V_{CC} = 3.0\text{ V}$ to 5.5 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:
 - ♦ $V_{CC} = 0\text{ V}$ with $V_{EE} = -3.0\text{ V}$ to -5.5 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



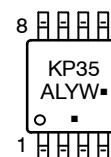
ON Semiconductor®

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**TSSOP-8
DT SUFFIX
CASE 948R-02**

MARKING DIAGRAM*



K = MC100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100EP35DTG	TSSOP-8 (Pb-Free)	100 Units / Tube
MC100EP35DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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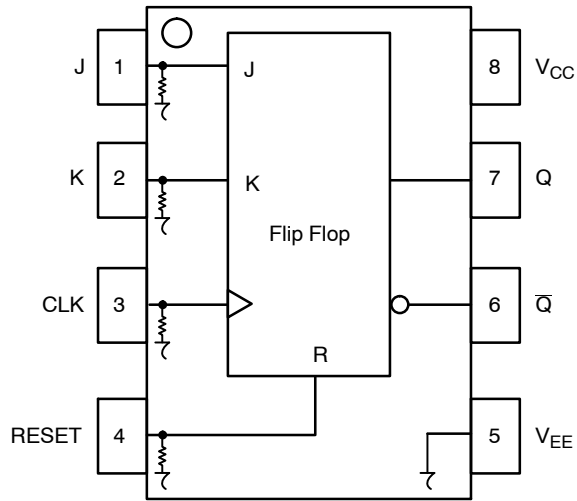


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK*	ECL Clock Inputs
J*, K*	ECL Signal Inputs
RESET*	ECL Asynchronous Reset
Q, $\bar{Q}$	ECL Data Outputs
V _{CC}	Positive Supply
V _{EE}	Negative Supply

* Pins will default LOW when left open.

Table 2. TRUTH TABLE

J	K	RESET	CLK	Q _{n+1}
L	L	L	Z	Q _n
L	H	L	Z	L
H	L	L	Z	H
H	H	L	Z	$\bar{Q}_n$
X	X	H	X	L

Z = LOW to HIGH Transition

Table 3. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) TSSOP-8	Pb-Free Pkg Level 3
Flammability Rating Oxygen Index: 28 to 34	UL-94 V-0 @ 0.125 in
Transistor Count	77 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

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Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		–6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 –6	V
I _{out}	Output Current	Continuous Surge		50 100	mA
T _A	Operating Temperature Range			–40 to +85	°C
T _{stg}	Storage Temperature Range			–65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP–8	185 140	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP–8	41 to 44	°C/W
T _{sol}	Wave Solder (Pb-Free)	<2 to 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 5. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 3.3 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
V _{OH}	Output HIGH Voltage (Note 2)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V _{OL}	Output LOW Voltage (Note 2)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V _{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to –2.2 V.
2. All loading with 50 Ω to V_{CC} – 2.0 V.

Table 6. 100EP DC CHARACTERISTICS, PECL (V_{CC} = 5.0 V, V_{EE} = 0 V (Note 1))

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
V _{OH}	Output HIGH Voltage (Note 2)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V _{OL}	Output LOW Voltage (Note 2)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V _{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to –0.5 V.
2. All loading with 50 Ω to V_{CC} – 2.0 V.

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Table 7. 100EP DC CHARACTERISTICS, NECL ($V_{CC} = 0\text{ V}$; $V_{EE} = -5.5\text{ V}$ to -3.0 V (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	30	40	50	30	40	50	30	40	50	mA
V_{OH}	Output HIGH Voltage (Note 2)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 2)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Input and output parameters vary 1:1 with V_{CC} .
2. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

Table 8. AC CHARACTERISTICS ($V_{CC} = 0\text{ V}$; $V_{EE} = -3.0\text{ V}$ to -5.5 V or $V_{CC} = 3.0\text{ V}$ to 5.5 V ; $V_{EE} = 0\text{ V}$ (Note 1))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (See Figure 2. $F_{\max}/\text{JITTER}$)		> 3			> 3			> 3		GHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential R, CLK to Q, $\bar{Q}$	200	400	480	200	410	490	200	420	575	ps
t_{RR}	Reset Recovery	150	80		150	90		150	100		ps
t_S t_H	Setup Time Hold Time	150 150	50 50		150 150	50 50		150 150	80 80		ps
t_{PW}	Minimum Pulse width RESET	550	400		550	400		550	400		ps
t_{JITTER}	Cycle-to-Cycle Jitter (See Figure 2. $F_{\max}/\text{JITTER}$)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t_r t_f	Output Rise/Fall Times Q, $\bar{Q}$ (20% – 80%)	70	120	170	80	130	180	100	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.

MC100EP35

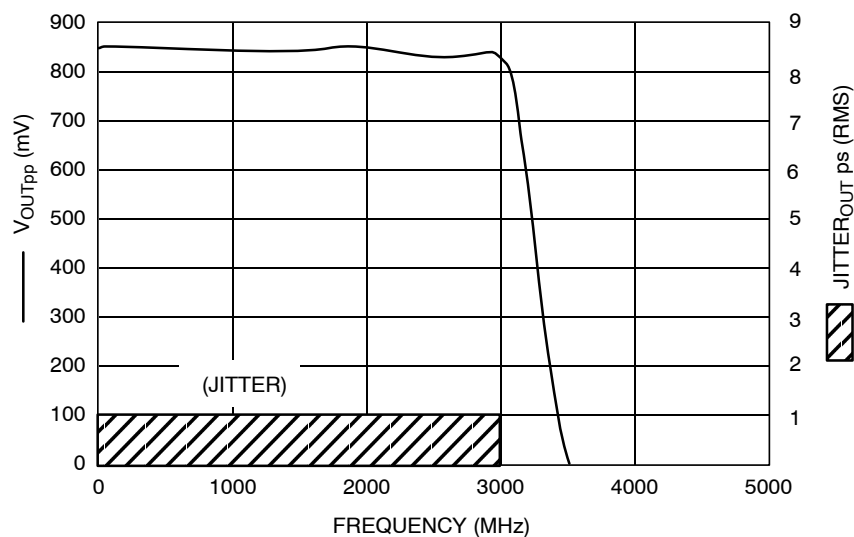


Figure 2. $F_{max}/Jitter$

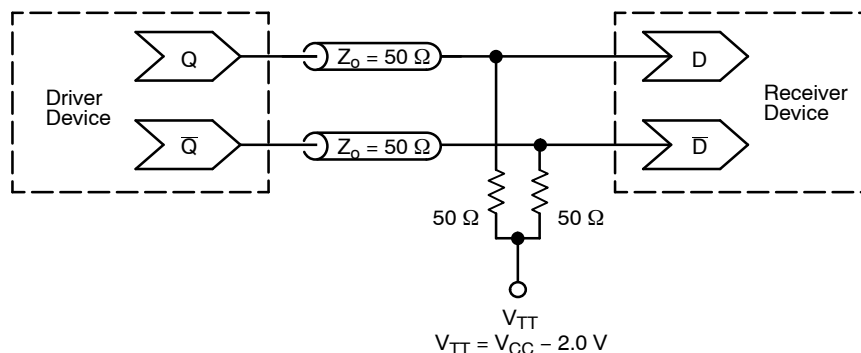


Figure 3. Typical Termination for Output Driver and Device Evaluation
(See Application Note [AND8020/D](#) – Termination of ECL Logic Devices.)

Resource Reference of Application Notes

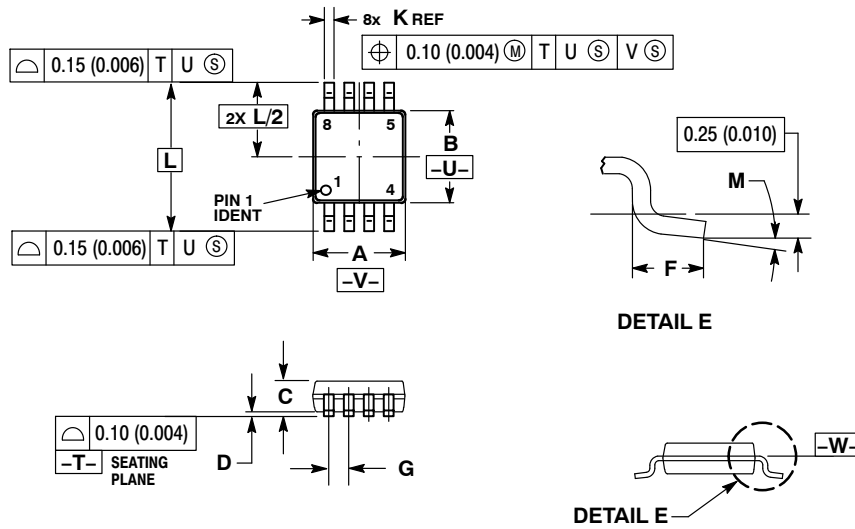
- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices



SCALE 2:1

TSSOP-8 3.00x3.00x0.95
CASE 948R-02
ISSUE A

DATE 07 APR 2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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