

NCP1650

Power Factor Controller

The NCP1650 is an active, power factor correction controller that can operate over a wide range of input voltages, and output power levels. It is designed to operate on 50/60 Hz power systems. This controller offers several different protection methods to assure safe, reliable operation under any conditions.

The PWM is a fixed frequency, average current mode controller with a wide complement of features. These features allow for both flexibility as well as precision in its application to a circuit. Critical components of the internal circuitry are designed for high accuracy, which allows for precise power and current limiting, therefore minimizing the amount of overdesign necessary for the power stage components.

The NCP1650 is designed with a true power limiting circuit that will maintain excellent power factor even in constant power mode. It also contains features that allow for fast transient response to changing load currents and line voltages.

Features

- Fixed Frequency Operation
- Average Current Mode PWM
- Continuous or Discontinuous Mode Operation
- Fast Line/Load Transient Compensation
- True Power Limiting Circuit
- High Accuracy Multipliers
- Undervoltage Lockout
- Overvoltage Limiting Comparator
- Brown Out Protection
- Ramp Compensation Does Not Affect Oscillator Accuracy
- Operation from 25 to 250 kHz
- This is a Pb-Free Device

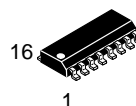
Typical Applications

- Server Power Converters
- Front End for Distributed Power Systems



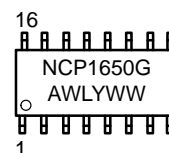
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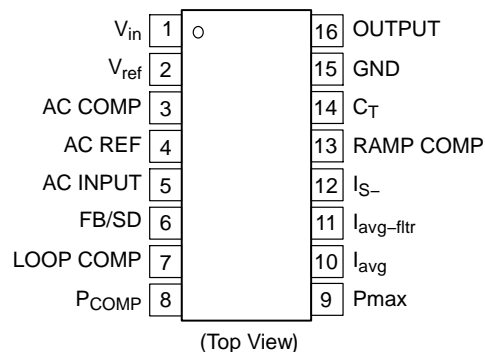
**SO-16
D SUFFIX
CASE 751B**

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1650DR2G	SOIC-16 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PIN FUNCTION DESCRIPTION

Pin #	Function	Description
1	V_{CC}	Provides power to the device. This pin is monitored for undervoltage and the unit will not operate if the V_{CC} voltage is not within the UVLO range.
2	V_{ref}	6.5 V regulated reference output. This reference voltage is disabled when the chip is in the shutdown mode.
3	AC Compensation	Provides pole for the AC Reference Amplifier. This amplifier compares the sum of the AC input voltage and the low frequency component of the input current to the reference signal. The response must be slow enough to filter out most of the high frequency content of the current signal that is injected from the current sense amplifier, but fast enough to cause minimal distortion to the line frequency information.
4	AC REF	This pin accommodates a capacitor to ground for filtering and stability of the AC error amplifier. The AC error amplifier is a transconductance amplifier and is terminated with an internal high impedance load.
5	AC Input	The rectified input AC rectified sinewave is connected to this pin. This information is used for the reference comparator, maximum power circuit, and the average current compensation circuit.
6	Feedback/ Shutdown	The DC output of the converter is reduced through a resistive voltage divider, to a level of 4.0 V, and connected to this pin to provide feedback for the voltage regulation loop. This pin also provides an input undervoltage lockout feature by disabling the chip until the divided output voltage exceeds 0.75 V. It can also be used as a shutdown pin by shorting it to ground with an open collector comparator, or a small signal transistor.
7	Loop Compensation	A compensation network for the voltage regulation loop, is connected to the output of the voltage error amplifier at this pin.
8	P_{COMP}	A compensation network for the maximum power loop, is connected to the output of the power error amplifier at this pin.
9	P_{MAX}	This pin allows the output of the power multiplier to be scaled for the desired maximum power limit level. This multiplier is a proprietary switching design and requires both a resistor and capacitor to ground. The value of this resistor is determined in conjunction with R10.
10	I_{avg}	An external resistor with a low temperature coefficient is connected from this terminal to ground, to set and stabilize the gain of the Current Sense Amplifier output that drives the Power Multiplier and the AC error amplifier. This resistor should be of the same type as that used on pin 9. The value of this resistor will determine the maximum average current that the unit will allow before limiting will occur.
11	I_{avgftr}	A capacitor connected to this pin filters the high frequency component from the instantaneous current waveform, to create a waveform that resembles the average line current.
12	I_{S-}	Negative current sense input. Designed to connect to the negative side of the current shunt.
13	Ramp Compensation	This pin biases the ramp compensation circuit, to adjust the amount of compensation that is added to the instantaneous current and AC error amp outputs.
14	C_T	Timing capacitor for the internal oscillator. This capacitor adjusts the oscillator frequency.
15	Ground	Ground reference for the circuit.
16	Output	Drive output for power FET or IGBT. Capable of driving small devices, or can be connected to an external driver for larger transistors.

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MAXIMUM RATINGS (Maximum ratings are those that, if exceeded, may cause damage to the device. Electrical Characteristics are not guaranteed over this range.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Operating) Output (Pin 16)	V_{CC}	-0.3 to 20	V
Current Sense Inverting Input (Pin 12)	$V(I_{S-})$	-0.5 to 1.0	V
Reference Voltage (Pin 2)	V_{ref}	-0.3 to 7.5	V
Reference Filter (Pin 4)	Ref fltr	-0.3 to 5.0	V
All Other Inputs		-0.3 to 6.5	V
Thermal Resistance, Junction-to-Air 0.1 in ² Copper 0.5 in ² Copper	θ_{JA}	130 110	°C/W
Thermal Resistance, Junction-to-Lead (Pin 1) (Note 1)	θ_{JL}	50	°C/W
Maximum Power Dissipation @ $T_A = 25^\circ\text{C}$	P_{max}	0.77	W
Operating Temperature Range	T_J	-40 to 125	°C
Non-operating Temperature Range	T_J	-55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. θ_{JL} is equivalent to Ψ_{jL}

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: $V_{CC} = 14$ volts, $C_T = 470$ pF, $C_2 = 0.1$ μF , $T_J = 25^\circ\text{C}$ for typical values. For min/max values T_J is the applicable junction temperature.)

Characteristic	Symbol	Min	Typ	Max	Unit
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OSCILLATOR

Frequency	F_{osc}	90	100	110	kHz
Max Duty Cycle	dmax	0.95	0.97	-	-
Min Duty Cycle (Note 2)	dmin	-	0	5.0	%
Ramp Peak (Note 2)	V_{Rpeak}	-	4.0	-	V
Ramp Valley (Note 2)	$V_{Rvalley}$	-	0.100	-	V
Ramp Compensation Peak Voltage (Pin 13) (Note 2)	-	-	4.0	-	V
Ramp Compensation Current (Pin 13) (Note 2)	-	-	400	-	μA

VOLTAGE ERROR AMPLIFIER

Input Bias Current (Note 2)	I_{bias}	-	0.2	0.6	μA
Input Offset Voltage (Note 2)	V_{IO}	-	10	-	mV
Transconductance ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$)	g_m	90	120	150	umho
Output Source ($V_{ref} + 0.2$ V)	$I_{Osource}$	10	20	-	μA
Output Sink ($V_{ref} - 0.2$ V)	I_{Osink}	-10	-20	-	μA
Boost Current ($V_{ref} = 4.0$ volts nominal)					
Source Boost Current Threshold (V_{pin6}/V_{ref})	$V_{fb(boost+)}$	-	1.06	-	V/V
Sink Boost Current Threshold (V_{pin6}/V_{ref})	$V_{fb(boost-)}$	-	0.920	-	V/V
Source Boost Current ($V_{ref} + 0.4$ V)	$I_{(boost+)}$	150	230	-	μA
Sink Boost Current ($V_{ref} - 0.4$ V)	$I_{(boost-)}$	-150	-260	-	μA

2. Verified by design.

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ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise noted: $V_{CC} = 14$ volts, $C_T = 470$ pF, $C_2 = 0.1$ μ F, $T_J = 25^\circ\text{C}$ for typical values. For min/max values T_J is the applicable junction temperature.)

Characteristic	Symbol	Min	Typ	Max	Unit
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POWER ERROR AMPLIFIER ($V_{comp} = 2.0$ V, $V_{ref} = 2.5$ V)

Input Offset Voltage (Note 3)	V_{IO}	–	20	–	mV
Transconductance	g_m	60	100	150	umho
Output Source ($V_{ref} + 0.2$ V)	$I_{Osource}$	10	20	–	μ A
Output Sink ($V_{ref} - 0.2$ V)	I_{Osink}	–10	–20	–	μ A
Boost Current ($V_{ref} = 2.5$ V nominal)					
Source Boost Current Threshold	$V_{fb(boost+)}$	–	1.175	–	V/V
Sink Boost Current Threshold	$V_{fb(boost-)}$	–	0.825	–	V/V
Source Boost Current ($1.3 \times V_{ref}$)	$I_{(boost+)}$	150	250	–	μ A
Sink Boost Current	$I_{(boost-)}$	–150	–285	–	μ A

AC ERROR AMPLIFIER

Input Offset Voltage (Note 3)	V_{IO}	–	20	–	mV
Transconductance	g_m	60	100	150	umho
Output Source (Pin 4 = 4 V, Pin 5 = 0 V)	$I_{Osource}$	25	70	–	μ A
Output Sink (Pin 4 = 0 V, Pin 5 = 4 V)	I_{Osink}	–25	–70	–	μ A
AC Inverting Input Clamp Voltage (250 μ A) ($T_J = 25^\circ\text{C}$)	V_{clamp}	4.30	4.45	4.60	V
AC Inverting Input Clamp Voltage (250 μ A) ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$)	V_{clamp}	3.70	–	4.60	V
Gain from AC_{comp} to PWM+ ($A_v = V_{PWM+} / (V_{ACcomp} - V_{offset})$) (Note 3)	A_v	–	2.0	–	V/V

CURRENT SENSE AMPLIFIER

Input Bias Current (Pin 11)	I_{bias}	–40	–50	–80	μ A
Differential Input Voltage Range (Note 3)	V_{Idiff}	–	–0.20	–	V
Input Offset Voltage	V_{IO}	0	2.5	5.0	mV
Output Gain (150 μ A/0.150 V) (Voltage Loop Outputs) (Note 3)	A_v	–	1000	–	umho
Output Gain (150 μ A/0.150 V) (Max Pwr Output) ($R_{10} = 15$ k Ω) (Note 3)	A_v	–	1000	–	umho
Bandwidth (Note 3)	f_{unity}	–	1.5	–	MHz
PWM Output Voltage Gain ($k = V_{PWM+} / V_{sense-}$) (Pin 13 = Open) ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$)	A_v	12.9	15	17	V/V
Current Limit Voltage Gain ($k = V_{ac/ea} / V_{sense-}$) ($V_{pin5} = 0$, $R_{10} = 15$ k)	A_v	13	15	17	V/V
Power Output Voltage Gain ($k = V_{pin10} / V_{sense-}$) ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$)	k	13.4	15	17	V/V
Current Limit Threshold ($V_{pin5} = 0$, Pin 13 = Open)	I_{LIMthr}	225	270	315	mV
Current Limit Delay (0 to –450 mV Step) (Note 3)	$I_{LIMdelay}$	–	300	–	nS

REFERENCE MULTIPLIER

Dynamic Input Voltage Range Ac Input (p–input) (Note 3) Compensation Input (a–input) (Note 3) Offset Voltage (a–input)	V_{max}	–	3.75	–	V
Multiplier Gain $k = \frac{V_{mult\ out}}{(V_{AC}/V_{ramp\ pk}) \times (V_{LOOPcomp} - V_{offset})}$ (Note 3)	k	–	8.0	–	1.0/V

3. Verified by design.

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ELECTRICAL CHARACTERISTICS (continued) (Unless otherwise noted: $V_{CC} = 14$ volts, $C_T = 470$ pF, $C_2 = 0.1$ μ F, $T_J = 25^\circ\text{C}$ for typical values. For min/max values T_J is the applicable junction temperature.)

Characteristic	Symbol	Min	Typ	Max	Unit
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MAXIMUM POWER MULTIPLIER

Multiplier Gain $K = \frac{V_{\text{pin9}}}{(-V_{\text{pin12}}) \times V_{\text{pin5}}} \approx \frac{4.0 \times R_9}{R_{10}} \quad \begin{matrix} (T_J = 25^\circ\text{C}) \\ (T_J = -40^\circ\text{C to } +125^\circ\text{C}) \end{matrix}$ $R_9 = 47 \text{ k}, R_{10} = 15 \text{ k}$	k	12.1 11.8	12.8 12.8	13.3 13.3	1.0/V
Dynamic Input Voltage Range Ac Input (p-input) (Note 4)	V_{max}	–	3.75	–	V

AC INPUT (Pin 5)

Input Bias Current (Total bias current for both multipliers and current compensation amplifier)	I_{Nbias}	–	0.01	–	μ A
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DRIVE OUTPUT

Source Resistance (80 mA Load)	R_{source}	4.0	8.0	15	Ω
Sink Resistance (–80 mA Load)	R_{sink}	3.0	8.0	15	Ω
Rise Time ($C_L = 1.0$ nF, 20% to 80%)	t_r	–	50	–	ns
Fall Time ($C_L = 1.0$ nF, 20% to 80%)	t_f	–	50	–	ns
Output Voltage in UVLO Condition	$V_{\text{O(UV)}}$	–	1.0	10	mV

VOLTAGE REFERENCE

4.0 Volt Reference (Pin 6) ($T_J = 25^\circ\text{C}$)	V_{ref}	3.94	4.00	4.06	V
4.0 Volt Regulation ($T_J = -55^\circ\text{C}$ to 125°C)	V_{ref}	3.92	4.00	4.08	V
2.5 Volt Reference (P_{max} , Pin 9)	$V_{\text{ref}2.5}$	2.40	2.50	2.60	V
Buffered Output ($I_{\text{load}} = 0$ mA)	V_{refOUT}	6.24	6.50	6.76	V
Load Regulation (Buffered Output, $I_o = 0$ to 10 mA, $V_{CC} \geq 10$ V)	DV_{refOUT}	0	4.0	40	mV

UNDERVOLTAGE LOCKOUT/SHUTDOWN

UVLO Startup Threshold (V_{CC} Increasing)	V_{SU}	10	10.5	11	V
UVLO Hysteresis (Shutdown Voltage = $V_{\text{SU}} - V_{\text{H}}$)	V_{H}	0.3	0.5	0.7	V
Shutdown Startup Threshold (Pin 6) (V_{out} Increasing)	V_{SD}	0.50	0.85	1.00	V
Shutdown Hysteresis (Pin 6)	V_{H}	0.10	0.18	0.3	V

OVERVOLTAGE PROTECTION

Overvoltage Voltage Trip Point ($V_{\text{pin6}}/V_{\text{ref}}$)	V_{OV}	106.5	108	109.5	V/V
Overvoltage Voltage Differential ($V_{\text{OV}} - V_{\text{boost+}}$)	V_{OVdiff}	–	50	–	mV

TOTAL DEVICE

Operational Bias Current ($C_{L(\text{Driver})} = 1.0$ nF, 100 kHz)	I_{BIAS}	–	4.0	5.0	mA
Bias Current in Undervoltage Mode	$I_{\text{Bshutdown}}$	–	0.6	1.0	mA

4. Verified by design.

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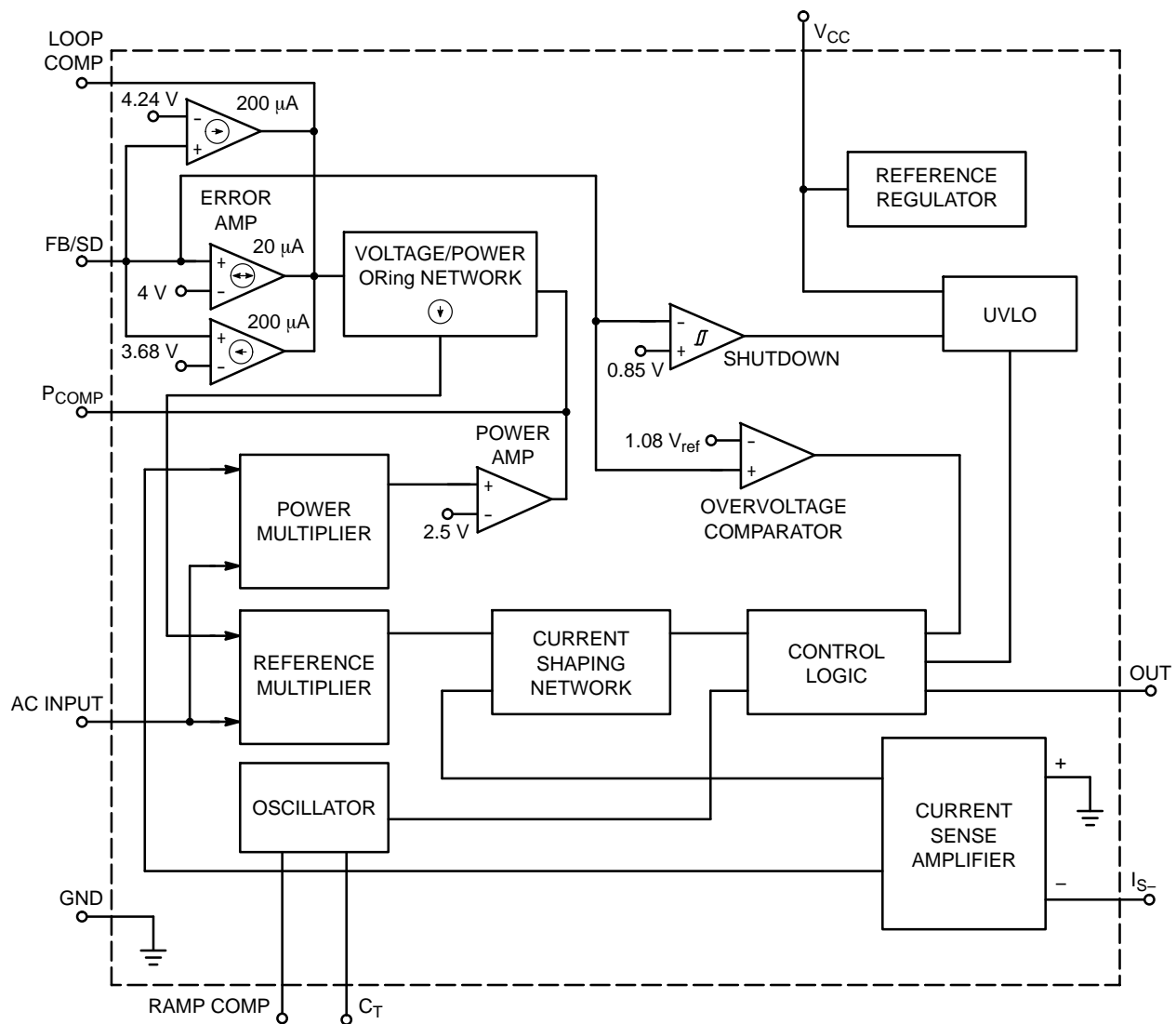


Figure 1. Simplified Block Diagram

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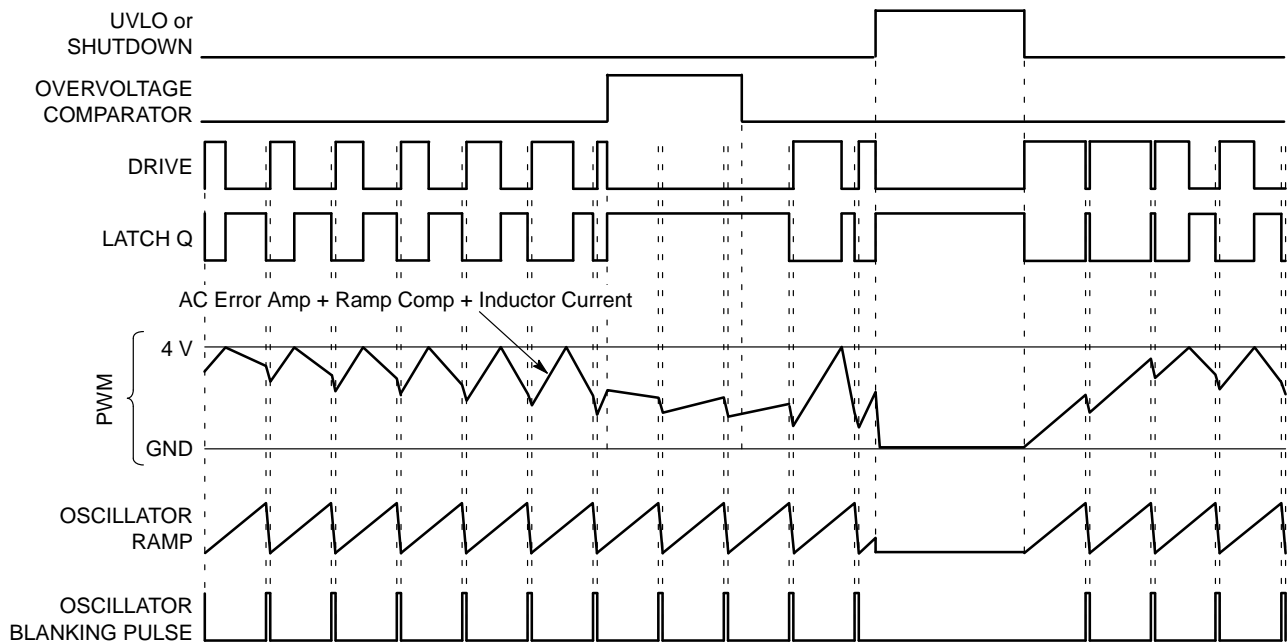


Figure 2. Timing Diagram

Typical Performance Characteristics

(Test circuits are located in the document TND307/D)

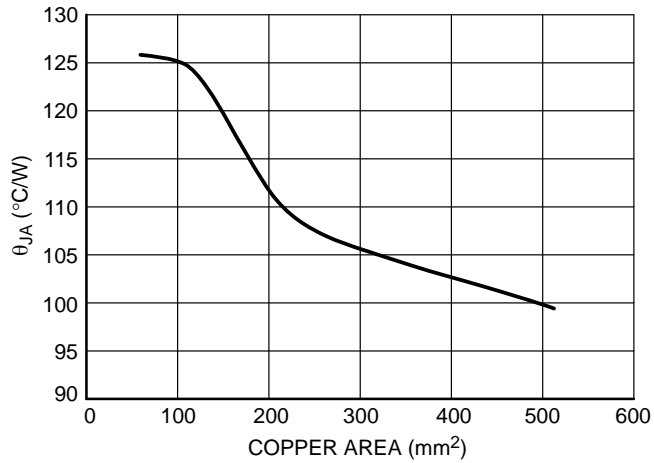


Figure 3. θ_{JA} as a Function of the Pad Copper Area (1 oz. Cu Thickness) for a JEDEC Test PCB

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Typical Performance Characteristics (Test circuits are located in the document TND307/D)

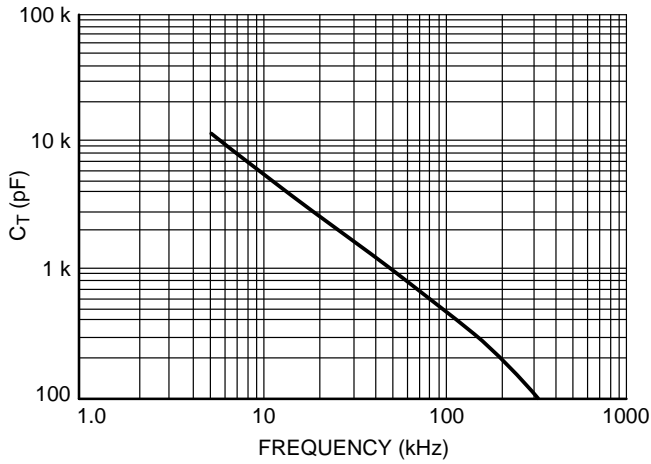


Figure 4. C_T versus Frequency

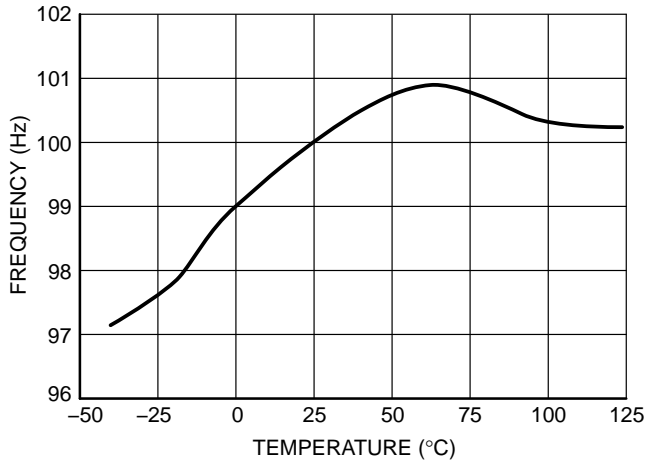


Figure 5. Frequency versus Temperature

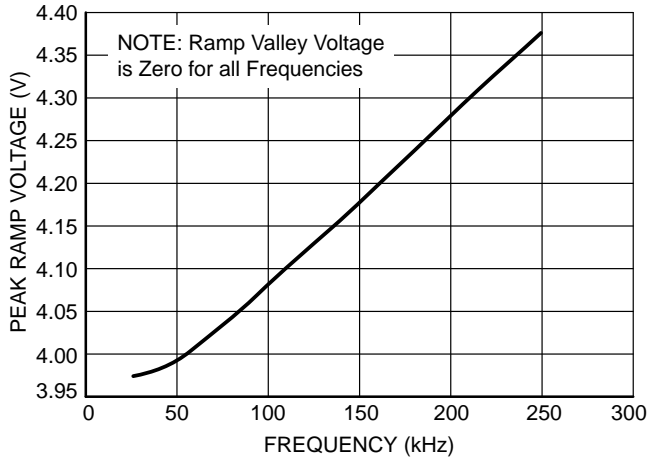


Figure 6. Ramp Peak versus Frequency

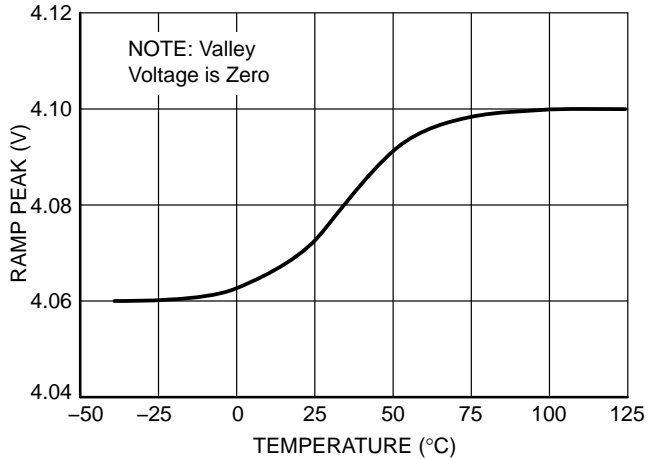


Figure 7. Peak Ramp Voltage versus Temperature

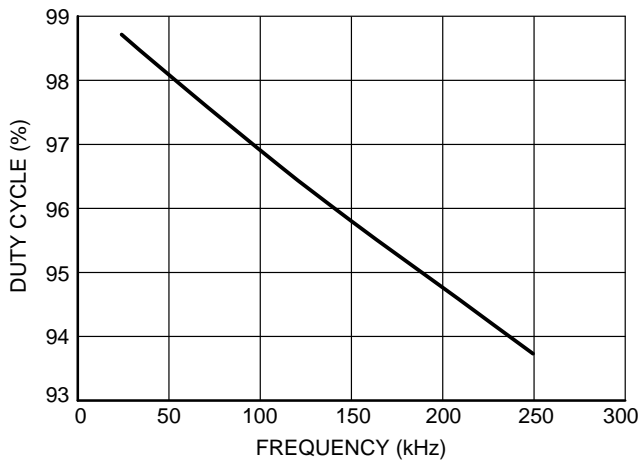


Figure 8. Max Duty Cycle versus Frequency

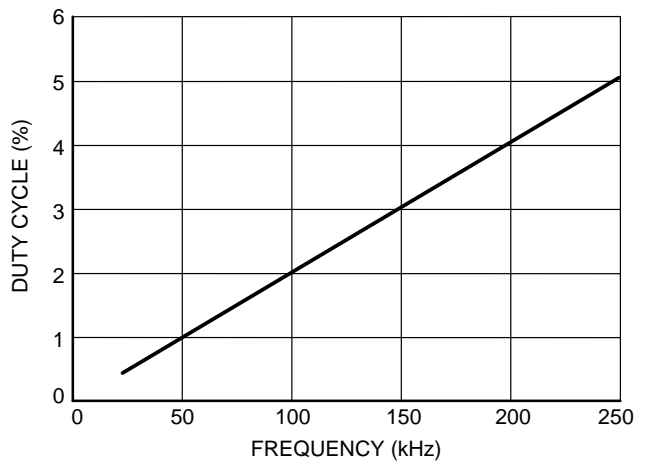


Figure 9. Minimum Duty Cycle versus Frequency

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Typical Performance Characteristics (Test circuits are located in the document TND307/D)

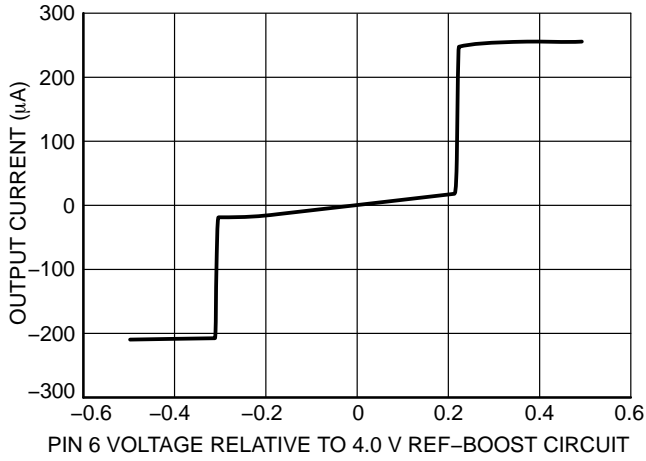


Figure 10. Voltage Amplifier Gain

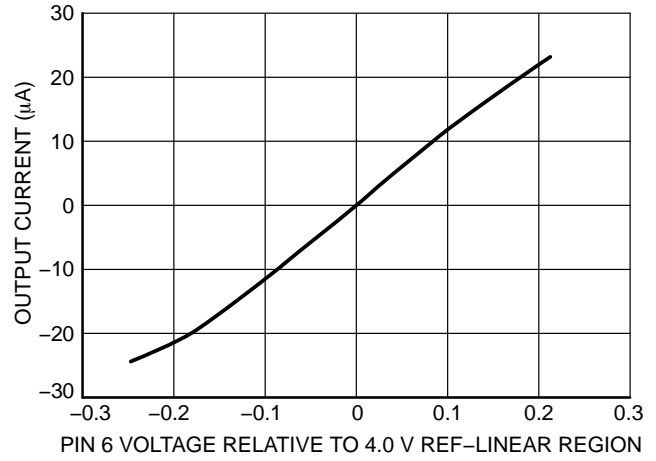


Figure 11. Voltage Amplifier Gain

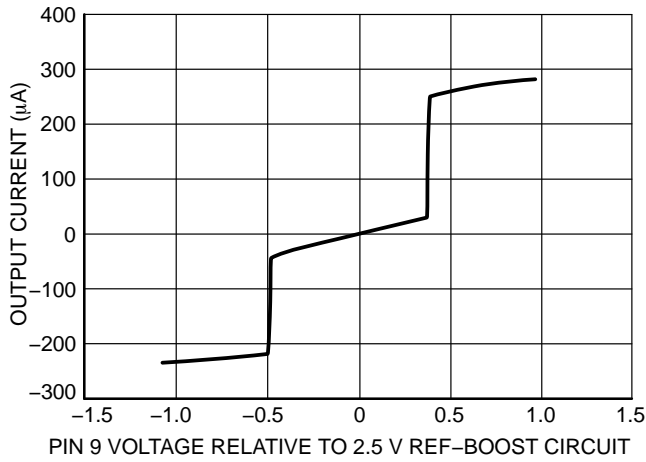


Figure 12. Power Amplifier Gain

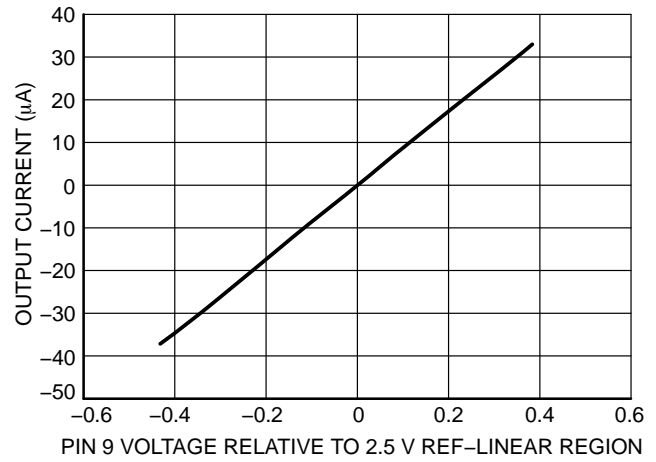


Figure 13. Power Amplifier Gain

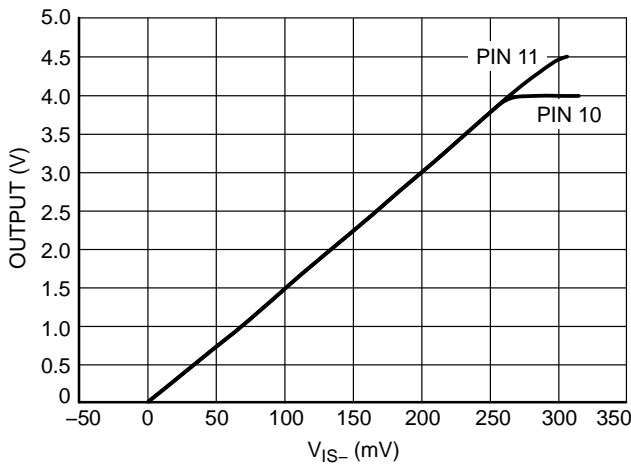


Figure 14. Current Sense Amplifier Gain

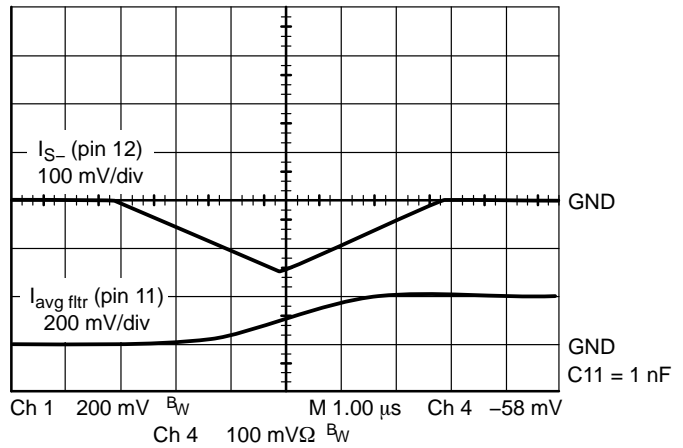


Figure 15. Current Sense Amplifier High Frequency Response

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Typical Performance Characteristics (Test circuits are located in the document TND307/D)

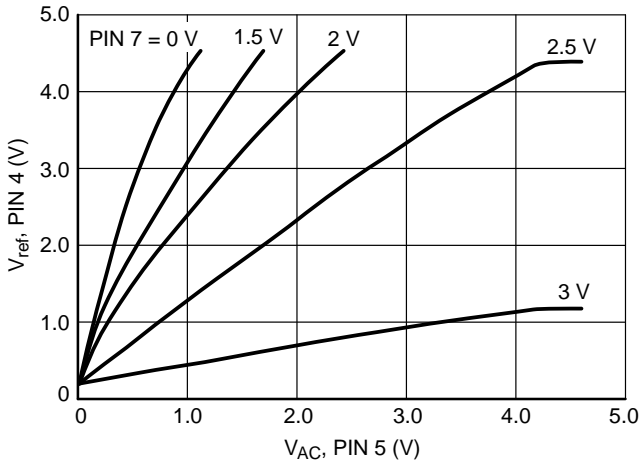


Figure 16. Reference Multiplier Transfer Function

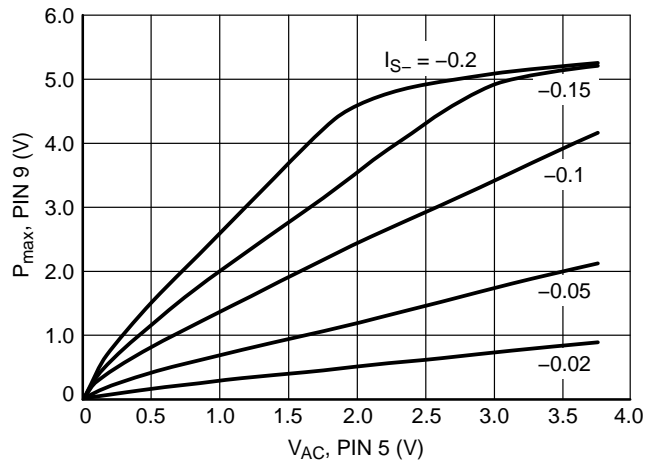


Figure 17. Power Multiplier Transfer Function

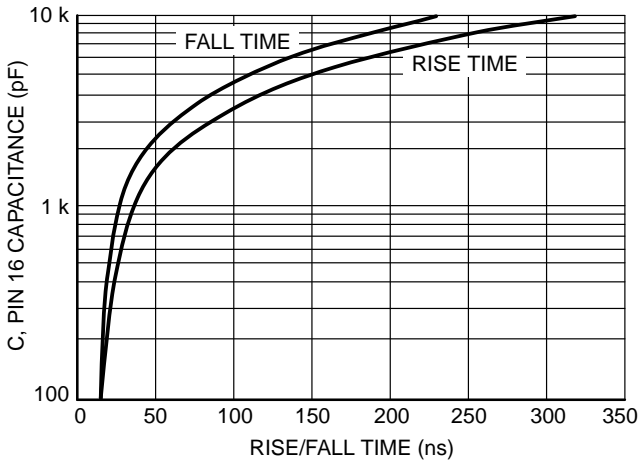


Figure 18. Capacitance versus 10-90% Drive Rise and Fall Times

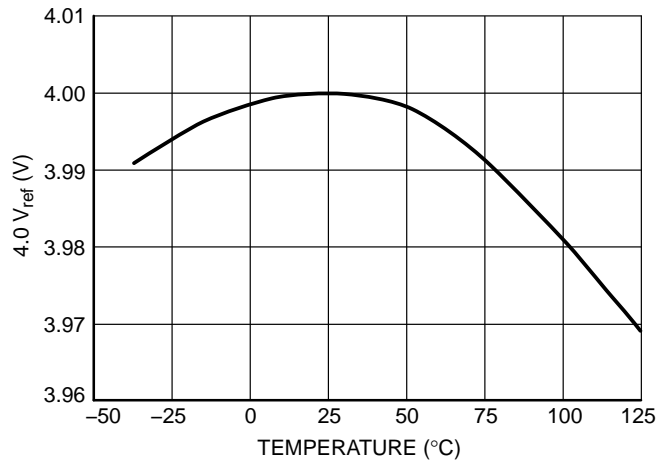


Figure 19. 4.0 Volt Reference versus Temperature

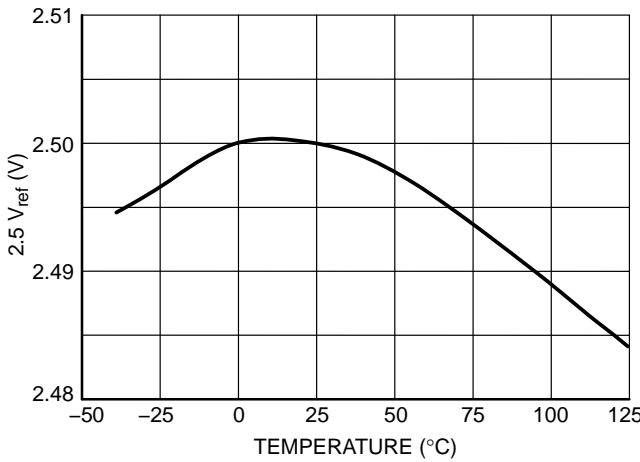


Figure 20. 2.5 Volt Reference versus Temperature

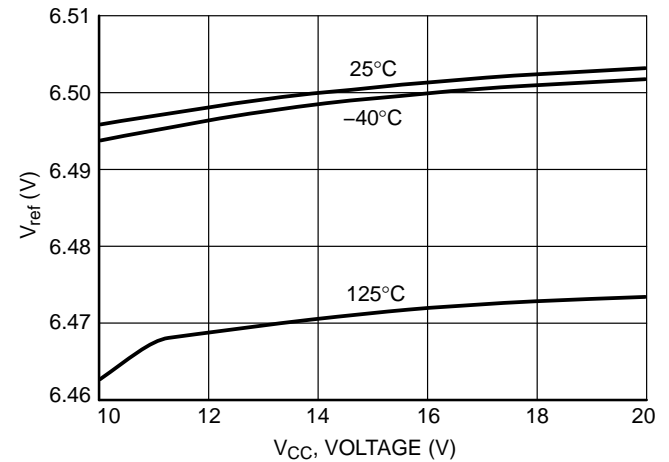


Figure 21. V_ref Line Regulation

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Typical Performance Characteristics (Test circuits are located in the document TND307/D)

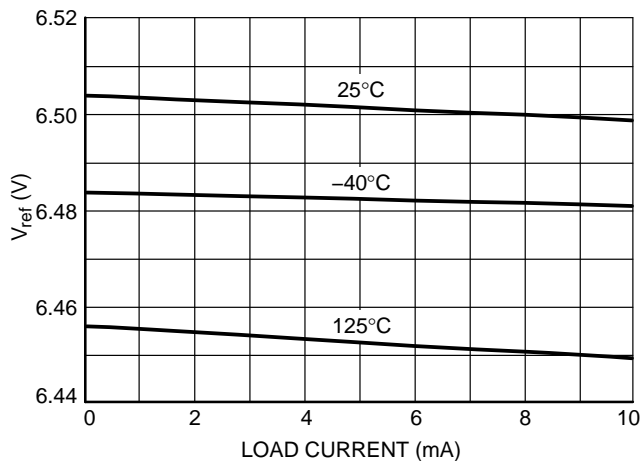


Figure 22. V_{ref} Load Regulation

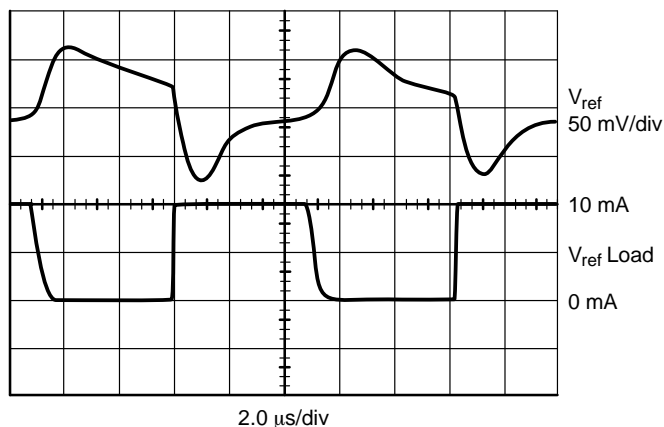


Figure 23. V_{ref} Transient Response

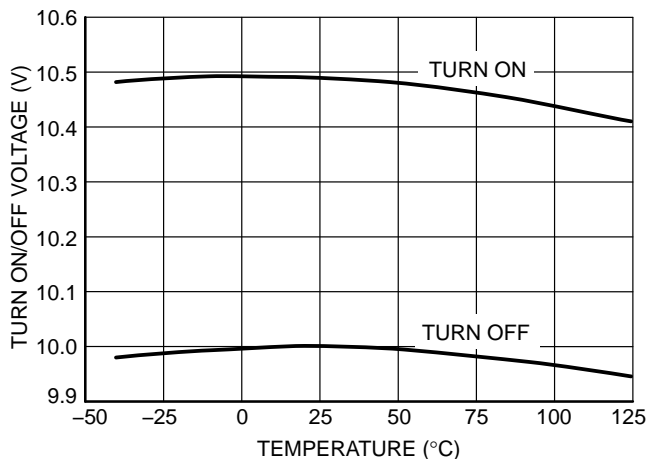


Figure 24. UVLO versus Temperature

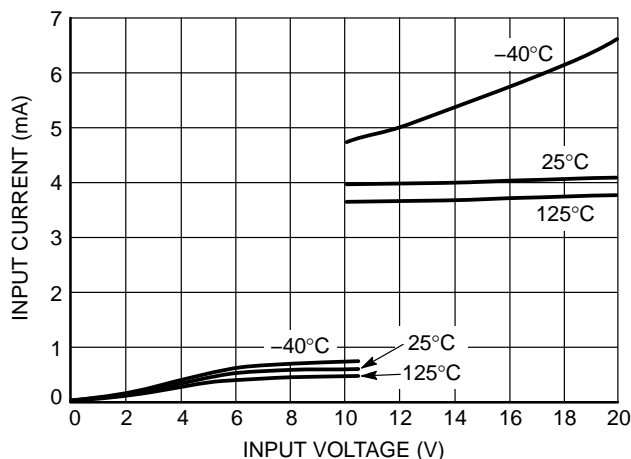


Figure 25. Input Current versus Input Voltage

NCP1650

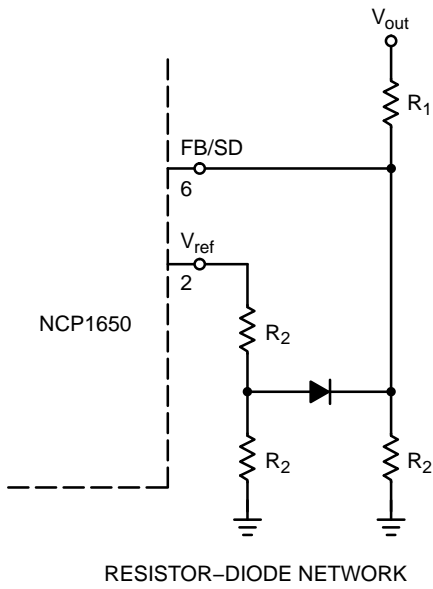


Figure 26. Shutdown Override Circuit

(This circuit will not override the shutdown until the chip has achieved its initial enable state)

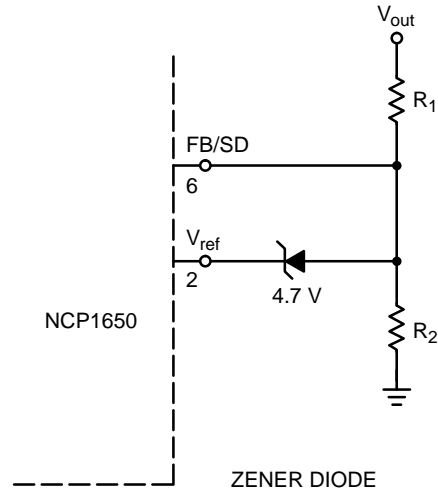


Figure 27. Shutdown Override Circuit

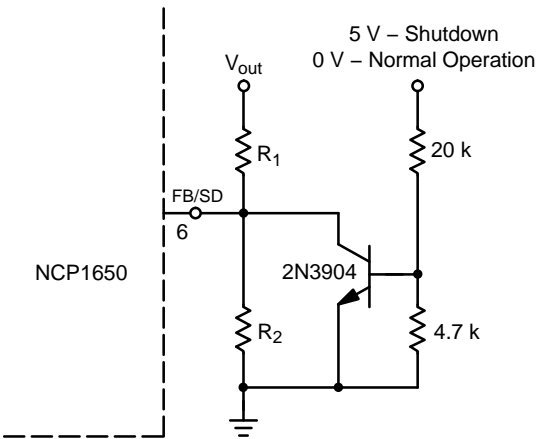


Figure 28. External Shutdown Circuit

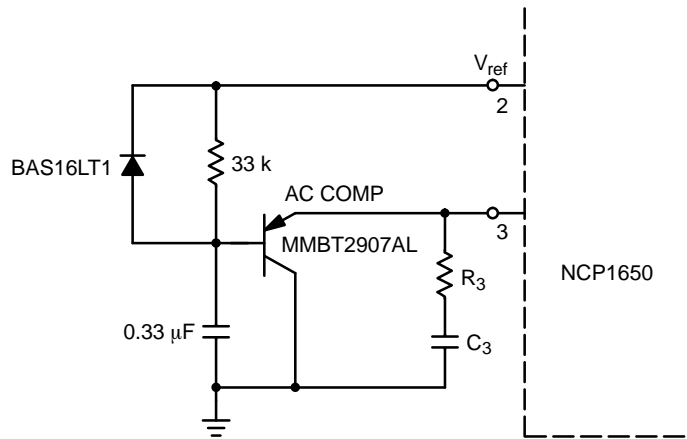


Figure 29. Soft-Start Circuit

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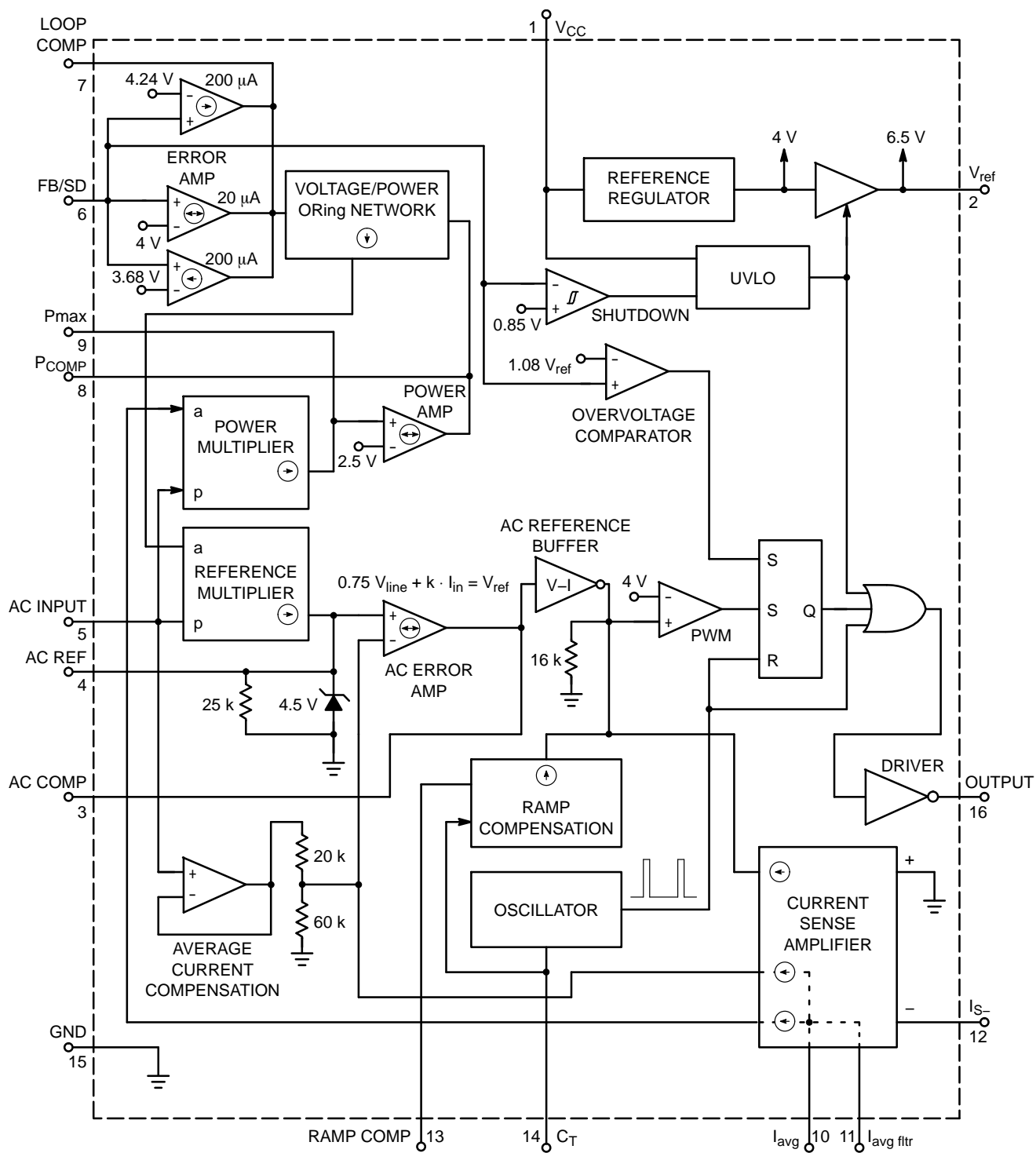


Figure 30. Detailed Block Diagram

THEORY OF OPERATION

Introduction

Optimizing the power factor of units operating off of AC lines is becoming more and more important. There are a number of reasons for this.

There are a growing number of government regulations requiring Power Factor Correction (PFC). Many of these are originating in Europe. Regulations such as IEC1000-3-2 are forcing equipment to utilize input stages with topologies other than a simple off-line front end which contains a bridge rectifier and capacitor.

There are also system requirements that dictate the use of PFC. In order to obtain the maximum power from an existing circuit in a building, the power factor is very critical. The real power available from such a circuit is:

$$P_{real} = V_{rms} \times I_{rms} \times PF$$

A typical off-line converter will have a power factor of 0.5 to 0.6, which means that for a given circuit breaker rating only 50% to 60% of the maximum power is available. If the power factor is increased to unity, the maximum available power can be obtained.

There is a similar situation in aircraft systems, where a limited supply of power is available from the on-board generators. Increasing the power factor will increase the load on the aircraft without the need for a larger generator.

Unity power factor is defined as the current waveform being in phase with the voltage, and undistorted. Therefore, there are two causes of power factor degradation – phase shift and distortion. Phase shift is normally caused by reactive loads such as motors which are inductive, or electroluminescent lighting which is highly capacitive. In such a case the power factor is relatively simple to analyze, and is determined by the phase shift.

$$PF = \cos \theta$$

Where θ is the phase angle between the voltage and the current.

Reduced power factor due to distortion is more complicated to analyze and is normally measured with AC analyzers, although most circuit simulation programs can also calculate power factor. One of the major causes of distortion is rectification of the line into a capacitive filter. This causes current spikes that do not follow the input voltage waveform. An example of this type of waveform is shown in the upper diagram in Figure 2.

A power converter with PFC forces the current to follow the input waveform. This reduces the peak current, the rms current and eliminates any phase shift.

The NCP1650 accomplishes this for both continuous and discontinuous mode power converters.

PFC Operation

The basic PWM function of the NCP1650 is controlled by a small block of circuitry, which comprises the DC regulation loop and the PFC circuit. These components are shown in Figure 26.

There are three inputs to this loop. They are the fullwave rectified input sinewave, the instantaneous input current and the DC output voltage.

The input current is forced to maintain a near unity power factor due to the control of the AC error amplifier. This amplifier uses information from the AC input voltage and the AC input current to control the power switch in a manner that provides good DC regulation as well as an excellent power factor.

The reference multiplier sets a reference level for the input fullwave rectified sinewave waveform. One of its inputs is connected to the scaled down fullwave rectified sinewave, and the other is connected to the output of the DC error amplifier. The signal from the DC error amplifier adjusts the level of the fullwave rectified sinewave on its output without distorting it. To accomplish this, it is necessary for the bandwidth of the DC error amp to be less than twice the lowest line frequency. Typically it is set at a factor of ten less than the rectified frequency (e.g. for a 60 Hz input, the bandwidth would be 12 Hz).

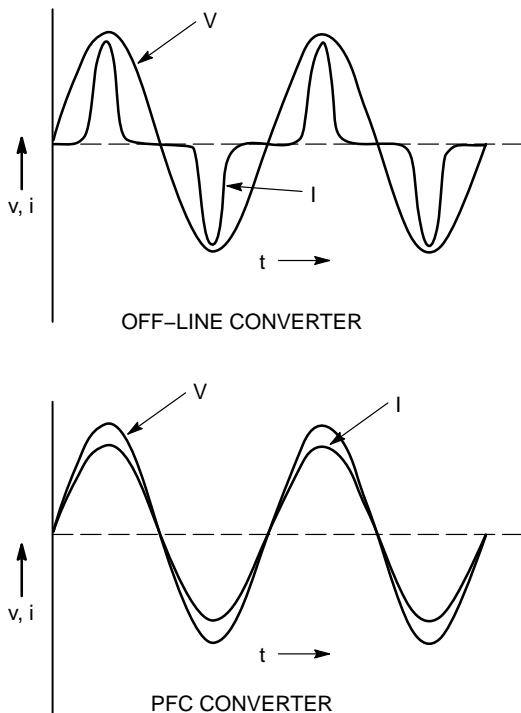


Figure 31. Voltage and Current Waveforms

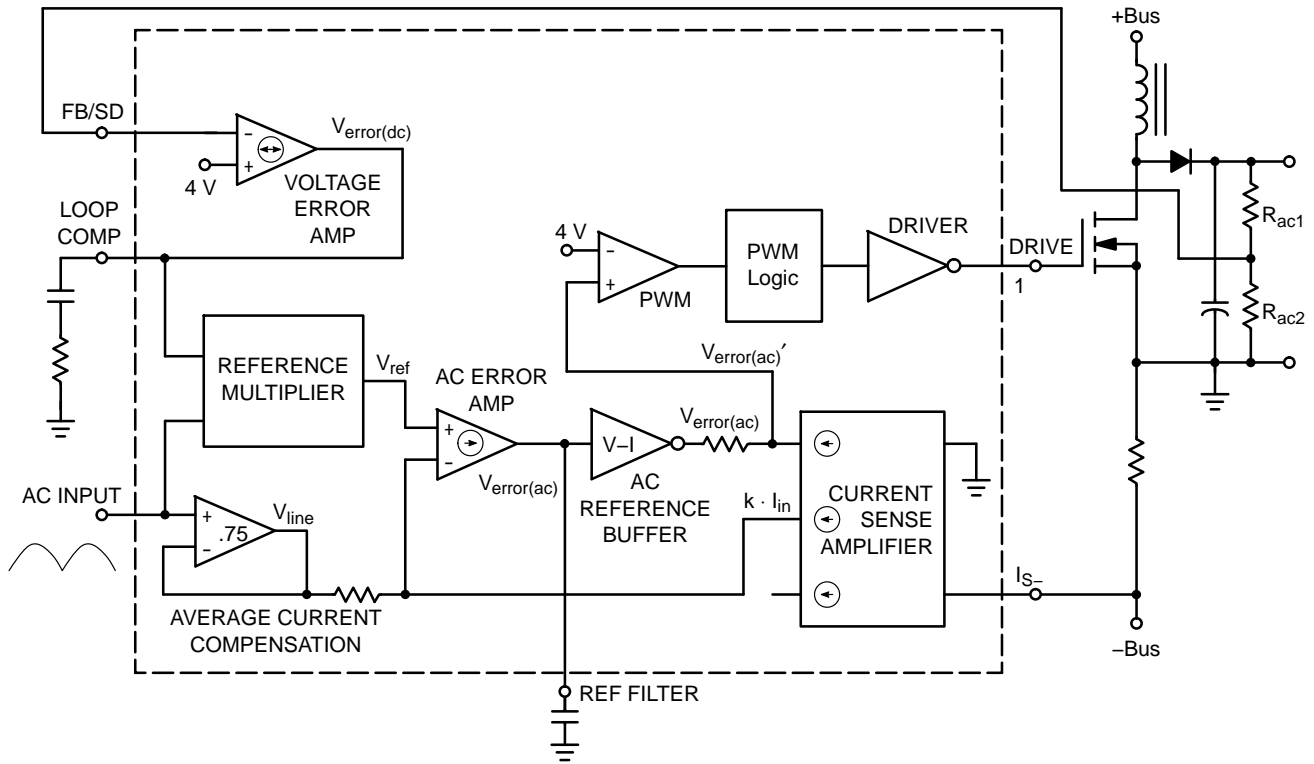


Figure 32. Simplified Block Diagram of Basic PFC Control Circuit

The key to understanding how the input current is shaped into a high quality sine wave is the operation of the AC error amplifier. The inputs of an operational amplifier operating in its linear range, must be equal.

There are several secondary effects, that create small differences between the inverting and non-inverting inputs, but for the purpose of this analysis they can be considered to be equal.

The fullwave rectified sinewave output of the reference multiplier is fed into the non-inverting input of the AC error amplifier. The inverting input to the AC error amplifier receives a signal that is comprised of the input fullwave rectified sinewave (which is not modified by the reference multiplier), and summed with the filtered input current. Since the two inputs to this amplifier will be at the same potential, the complex signal at the inverting input will have the same wave shape as the AC reference signal. The AC reference signal (V_{ref}) is a fullwave rectified sinewave, and the AC input signal (V_{line}) is also a fullwave rectified sinewave, therefore, the AC current signal (I_{in}), must also be a fullwave rectified sinewave. This relationship gives the formula:

$$V_{ref} = .75 \cdot V_{line} + (k \cdot I_{in})$$

The I_{in} signal has a wide bandwidth, and its instantaneous value will not follow the low frequency fullwave rectified sinewave exactly, however, the output of the AC error amplifier has a low frequency pole that allows the average value of the $.75 V_{line} + (k \times I_{in})$ to follow V_{ref} . Since the AC error amplifier is a transconductance amplifier, it is followed by an inverting unity gain buffer stage with a low impedance

output so that the signal can be summed with the instantaneous input switching current (I_{in}). The output of the buffer is still V_{error}^{ac} .

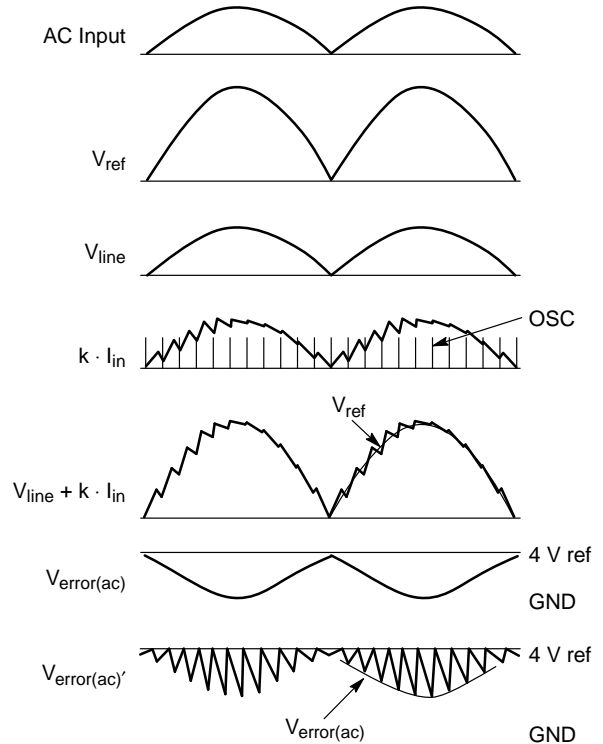


Figure 33. Typical Signals for PFC Circuit

The difference between $V_{\text{error(ac)}}$ and the 4.0 volt reference, sets the window that the instantaneous current will modulate in, to determine when to turn the power switch off.

The switch is turned on by the oscillator, which makes this a fixed frequency controller. Under normal operation, the switch will remain on until the instantaneous value of $V_{\text{error(ac)}}$ reaches the 4.0 volt reference level, at which time the switch will turn off.

Since the input current has a fundamental frequency that is twice that of the line, the output filter must have poles lower than the input current to create a reasonable DC waveform. The output DC voltage is divided down via an external divider and fed back to the DC error amplifier.

Protection Features

The NCP1650 contains a number of features to protect the device and circuit from overload and stressful conditions. These include:

- Output voltage overshoot protection
- Low line input protection
- Instantaneous current limit
- Line frequency current limit
- Maximum power limit

Output Voltage Overshoot Protection

An overshoot comparator has been provided to monitor the output voltage. Due to the slow transient response of a PFC controller, a fast load dump can cause a large output voltage transient to occur.

The overshoot comparator uses the same input as the feedback and shutdown signals. Its reference is set 8% higher than the reference used by the error amplifier. This comparator will shutdown the output stage if the output voltage exceeds the set level by 8%. The circuit will resume operation once the voltage is reduced to within 8% of the set level.

Low Line Input Protection

This feature uses the shutdown circuitry to assure that the unit does not start under low line condition. PFC converters typically are designed with an output voltage of 400 VDC. To reduce this to the level of the 4.0 volt reference, a 100:1 ratio is required for the voltage divider to the FB/SD pin. When the converter is energized, the output voltage will be the peak line voltage. If the peak line voltage does not exceed 75 volts (0.75 volts at the FB/SD pin) the unit will not start. This corresponds to a line voltage of 53 volts rms. Application circuits have been provided in Figures 33 and 34 to override this feature if desired.

Instantaneous Current Limit

The fastest protection available is a cycle-by-cycle current limit feature.

The current sense amplifier has three outputs. One is the instantaneous current in the inductor, and the other two are average current waveforms. The instantaneous current signal goes directly to the PWM and is terminated by an internal 16 k Ω resistor. This current signal is added to the output of the AC error amplifier and the ramp compensation signal. The switch will conduct current until the sum of these three signals reaches the 4.0 V reference of the inverting input to the PWM comparator. The peak current is determined by the value of the ramp compensation resistor (R_{13}) and the current shunt.

Line Frequency Current Limit

The output of the reference multiplier determines the current that will be required for the unit to regulate. The sum of the input voltage from the Average Current Compensation amplifier and the averaged current signal from the current sense amplifier must add to the level of the reference multiplier. The output of this multiplier is clamped to a 4.5 maximum level. The maximum average current is set by R_{10} .

This form of protection is slower than the cycle-by-cycle current limiting, but faster than the maximum power limit circuit.

Maximum Power Limit

The NCP1650 can limit the output power to protect against nuisance tripping of circuit breakers or other input power restrictions. It should be understood that boost regulators by design, can not be short circuit limited. Operation of the power limiting circuit will reduce the output voltage only to the level where it is equal to the peak of the input line voltage. At this point, the rectified line voltage will continue to provide output voltage through line frequency rectification by means of the series rectifier diode.

The input power of the converter is calculated by the power multiplier. By multiplying the instantaneous input voltage (AC input signal, pin 5) and the instantaneous input current (averaged current sense amplifier output), the actual input power is accurately calculated.

The power multiplier has a very low frequency pole which converts the power to a filtered DC level. The power error amplifier has a reference set at 2.5 volts. If the output of the power multiplier reaches 2.5 volts, the power error amplifier takes control of the loop via the ORing network and will regulate a constant power output within the limits of the power stage. It should be understood that once the output voltage is reduced to a level equal to the peak of the input voltage, the converter can no longer control the output power.

The output power level is set by combination of the I_{avg} resistor at pin 10 and the P_{max} resistor at pin 9.

OPERATING DESCRIPTION

DC Reference and Buffer

The internal DC reference is a precision bandgap design with a nominal output voltage of 4.0 volts. It is temperature compensated, and trimmed for a $\pm 1\%$ tolerance of its nominal voltage, with an overall tolerance over line and temperature of $\pm 2\%$. To assure maximum stability, this is only used as a reference so there is minimal loading on this source.

The DC reference is fed into a buffer with a gain of 1.625 which creates a 6.5 volt supply. This is used as an internal voltage to power many of the blocks inside of the NCP1650 and is also available for external use. The 6.5 volt reference is designed to be terminated with at 0.1 μF capacitor for stability reasons.

There is no buffer between the internal and external 6.5 V supply, so care should be used when connecting external loads. A short or overload on this voltage output will inhibit the operation of the chip.

There is also a 2.5 volt reference on the power amplifier. This is derived by a resistive voltage divider off of the 4.0 V reference.

Undervoltage Lockout

An Undervoltage Lockout circuit (UVLO) is provided to assure that the unit does not exhibit undesirable behavior at low V_{cc} levels. It also reduces power consumption to a level that allows rapid charging of the V_{cc} cap.

When the V_{cc} cap is originally charging, the UVLO will hold the unit off, and in a low bias current mode until the V_{cc} voltage reaches a nominal 10.5 volt level. At this point the unit will begin operation, and the UVLO will no longer be active. If the V_{cc} voltage falls to a level that is 0.5 volts below the turn-on point, the UVLO circuit will again become active.

When in the shutdown state, the UVLO circuit removes power from all internal circuitry by shutting off the 6.5 volt supply. The 4.0 volt reference remains active, and the UVLO and Shutdown comparators are also active.

Multipliers

The NCP1650 uses a new proprietary concept for the Power and Reference multipliers. This innovative design allows greatly improved accuracy compared to a conventional linear analog multiplier. The multipliers use a PWM switching circuit to create a scalable output signal, with a very well defined gain.

One input (A) to the multiplier is a voltage-to-current (V-I) converter. By converting the input voltage into a current, an overall multiplier gain can be accomplished. In addition, there will be no error in the output signal due to the series rectifier.

The other signal (Input P) is inputted into the PWM comparator. This selects a pulse width for the comparator output. The current signal from the V-I converter is factored by the duty cycle of the PWM comparator, and then filtered

by the RC network on the output. This network creates a low pass filter, and removes the high frequency content from the original waveform.

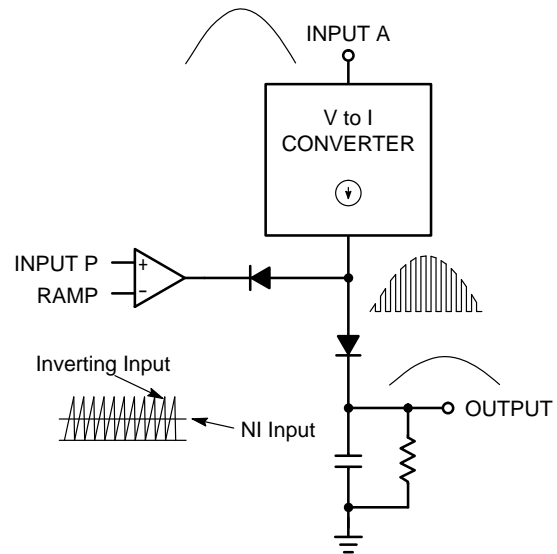


Figure 34. Simplified Multiplier Schematic

The multiplier ramp is generated by the internal oscillator, and is the same signal as is used in the PWM. It will therefore have the same frequency as the power stage.

It is not necessary for Input P (into the PWM comparator) to be a DC signal, low frequency AC signals (relative to the ramp frequency) work well also.

The gain of the multiplier is determined by the current-to-voltage ratio of the V-I converter, the load resistor of the output filter and the peak and valley points of the sawtooth ramp. When the P input signal is at the peak of the ramp waveform, the comparator will allow the A input signal to pass without chopping it at all. This gives an output voltage of the A current multiplied by the output filter resistance. When the P input signal is at the ramp valley voltage, the comparator is held low and no current is passed into the output filter. Between these two extremes, the duty cycle (and therefore, the output signal) is proportional to the level of the P input signal.

The output filter is a parallel RC network. The pole for this network needs to be greater than twice the highest line frequency (120 Hz for a 60 Hz line), and less than the switching frequency.

Reference Multiplier The two multipliers have different rules for designing their filters. The reference multiplier contains an internal loading resistor, with a nominal value of 25 k Ω . This is because the resistor that converts the A input voltage into a current is internal. Making both of these resistors internal, allows for good accuracy and good temperature performance. Only a capacitor needs to be added externally to properly compensate this multiplier. It is not

recommended that an external resistor be used at the “Ref Gain” pin, due to tolerance variations of the internal resistances.

The voltage-to-current conversion is performed in the Voltage/Power ORing network. This circuit also limits the maximum input signal (from the error amplifier) to 3 volts.

Power Multiplier/Current Sense Amplifier There is no voltage-to-current converter on the power multiplier. The current output of the current sense amplifier is used for the analog input with no scaling.

The power multiplier requires an external resistor as well as an external capacitor. The value of the resistor at pin 9 (max power) will depend on the value of the resistor used at pin 10 for the current gain and the maximum desired output power of the converter. These resistors should be the same style of resistor and have the same temperature coefficients for best performance.

The gain of the power multiplier is based on the values of external components on this multiplier as well as the current sense amplifier. The current sense amplifier output that drives the power multiplier has its gain controlled by R_9 and R_{10} , and is filtered by a capacitor on pin 11 which removes the high frequency content from the inductor current signal.

The gain for the power multiplier can be calculated as follows:

$$(1.) V_9 = I_{CS} \times R_9 \times (V_{ac}/V_{ramp})$$

Where:

I_{CS} is the rms value of the average current out of the current sense amplifier

R_9 is the resistor value at pin 9 (Ohms)

V_{ac} is the rms voltage at pin 5

V_{ramp} is the sawtooth p-p ramp voltage (4.0 volts)

and,

$$(2.) I_{CS} = V_{CS} \times 15/R_{10}$$

Since the pole at pin 12 is much greater than twice the line frequency we can ignore the effects of the capacitor on this pin. V_{CS} is the differential current sense rms input voltage.

Equations 1 and 2 can be rearranged to give the gain of the multiplier:

$$(3.) V_9 = \frac{3.75 \cdot R_9 \cdot V_{CS} \cdot V_{ac}}{R_{10}}$$

This gain equation gives the output voltage of the multiplier, where the inputs are the AC fullwave rectified sinewave and the current sense input signal.

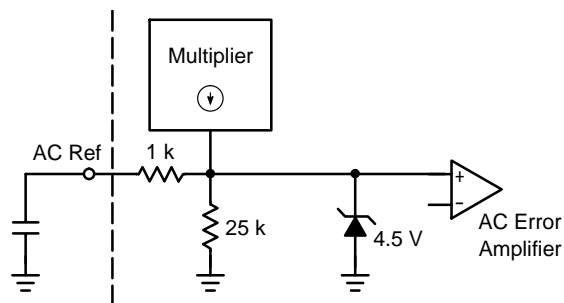


Figure 35. Reference Multiplier Clamp Circuit

There is a 1 k resistor between the AC Ref pin and the AC Error Amplifier for ESD protection. Due to this resistor, the voltage on pin 4 will exceed 4.5 volts under some conditions, but the maximum voltage at the non-inverting AC Error Amplifier input will be clamped at 4.5 volts.

Feedback/Shutdown

The FB/SD pin is a multiple function pin. Its primary function is to provide an input to the error amplifier for sensing of the output voltage. The signal at this pin is also sensed by an internal comparator that will shutdown the unit if the voltage falls below 0.75 volts.

The feedback circuit applies the signal to the non-inverting input of the voltage loop error amp. The other input of the error amp is connected to the internal 4.0 volt reference. The output of a voltage divider from the high voltage DC output to ground, feeds this pin.

The shutdown function can be used for multiple purposes including overvoltage, undervoltage or hot-swap control. An external transistor, open collector or open drain gate, connected to this pin can be used to pull it low, which will inhibit the operation of the chip, and change the operating state to a low power standby mode. An example of a shutdown circuit is shown in Figure 36.

The shutdown circuit is designed such that under normal line conditions the unit will be on. At startup, the AC line is rectified and charges up the output capacitor. Under normal line conditions, the output voltage will be great enough to apply more than 1.0 volt to this pin and the circuit will commence switching. If the unit is turned on into a low line condition, the voltage at this pin will not allow the unit to start.

Figures 33 and 34 shown circuits that can be used to disable the shutdown function. Both of these circuits limit the minimum voltage that can appear at the FB/SD input when the chip is properly biased, while not interfering with the 4.0 volt level that pin 6 sees when the unit is operating properly.

Ramp Compensation

The Ramp Compensation pin allows the amount of ramp compensation to be adjusted for optimum performance. Ramp compensation is necessary in a current mode

converter to stabilize the units operation when the duty cycle is greater than 50%.

The amount of compensation required is dependent on several variables, including the boost inductor value, and the desires of the designer. The value should be based on the falling di/dt of the inductor current. For a boost inductor with a variable input voltage, this will vary over the AC input cycle, and with changes in the input line. A di/dt chart is included in the design spreadsheet that is available for the NCP1650.

This pin is a buffered output of the oscillator, which provides a voltage equal to the ramp on the oscillator C_T pin. A resistor from this pin to ground, programs a current that is transformed via a current mirror to the non-inverting input of the PWM comparator.

The ramp voltage due to the inductor di/dt at the input to the PWM comparator is the current shunt voltage at pin 11 multiplied by 15, which is the gain of the current amplifier output that feeds the PWM.

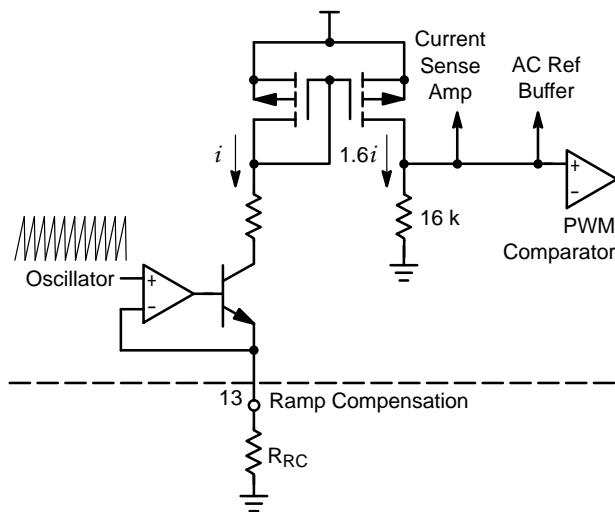


Figure 36. Ramp Compensation Circuit

The current mirror is designed with a 1:1.6 current ratio. The ramp signal injected can be calculated by the following formula:

$$V_{Rcomp} = \frac{1.6 V_{oscpk} 16 k}{R_{RC}} = \frac{102}{R_{RC}}$$

Where:

V_{Rcomp} = Peak injected ramp signal (v)

R_{RC} = Ramp compensation resistor (kΩ)

Oscillator

The oscillator generates the sawtooth ramp signal that sets the switching frequency, as well as sets the gain for the multipliers. Both the frequency and the peak-to-peak amplitude are important parameters.

The oscillator uses a current source for charging the capacitor on the C_T pin. The charge rate is approximately 200 μA and is trimmed to maintain an accurate, repeatable frequency. Discharge is accomplished by grounding the C_T

pin with a saturated transistor. A hysteretic comparator monitors that ramp signal and is used to switch between the current source and discharge transistor. While the cap is charging, the comparator has a reference voltage of 4.0 volts. When the ramp reaches that voltage, the comparator switches from the charging circuit to the discharge circuit, and its reference changes from 4.0 to ~0.5 volts (overshoot and delays will allow the valley voltage to reach 0 volts).

The relationship between the frequency and timing capacitor is:

$$C_T = 47,000/f$$

Where C_T is in pF and f is in kHz.

It is important not to load the capacitor on this pin, since this could affect the accuracy of the frequency as well as that of the multipliers which use the ramp signal. Any use of this signal should incorporate a high impedance buffer.

Due to the required accuracy of the peak and valley ramp voltages, the NCP1650 is not designed to be synchronized to the frequency of another oscillator.

Average Current Compensation

The Peak Current Compensation circuit adjusts the maximum current that can occur before the controller limits the current. This allows for higher levels of current under low line conditions than at high line.

The input signal to this amplifier is the input fullwave rectified sinewave. The amplifier is a unity gain amplifier, with a voltage divider on the output that attenuates the signal by a factor of 0.75. This scaled down fullwave rectified sinewave is summed with the low frequency current signal out of the current sense amplifier.

The sum of these signals must equal the signal at the inverting input to the AC error amplifier, which is the output of the reference multiplier. Since there is a hard limit of 4.5 volts at the inverting input, the sum of the line voltage plus the current cannot exceed this level.

A typical universal input design operates from 85 to 265 vac, which is a range of 3.1:1. The output of the Average Current Compensation amplifier will change by this amount to allow the maximum current to vary inversely to the line voltage.

Driver

The output driver can be used to directly drive a FET, for low and medium power applications, or a larger driver for high power applications.

It is a complementary MOS, totem pole design, and is capable of sourcing and sinking over 1.5 amps, with typical rise and fall times of 30 ns with a 1.0 nF load. The totem pole output has been optimized to minimize cross conduction current during high speed operation.

Additional internal circuitry has been added to keep the Driver in its low state whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pulldown resistor.

Error Amplifiers

The NCP1650 has three error amplifiers. These amplifiers regulate the DC output voltage, the maximum output power, and shape the AC reference fullwave rectified sinewave signal.

All three of these are transconductance amplifiers. Transconductance amplifiers differ from voltage amplifiers in that the output is a high impedance with a controlled voltage-to-current gain (i.e. the output current is proportional to the differential input voltage). The gain of a transconductance amplifier is determined by the equation:

$$A_v = g_m R_L$$

Voltage Error Amplifier The voltage loop has a low bandwidth amplifier, which is referred to simply as “Error Amp” on the block diagram. This amplifier compares the output DC voltage to the 4.0 volt reference and generates an error signal which is used to adjust the AC reference voltage from the reference multiplier.

The voltage error amplifier has a nominal gain of 100 umhos (or 0.0001 amps/volt). This means that an input voltage differential of 10 mv would cause the output current to change by 1.0 μA. The maximum output current for this amplifier in its normal operating range is 50 μA.

This amplifier is a switched gain transconductance amplifier, that increases the output current (or gain) when the differential input voltage exceeds the reference voltage by +6% or -8% the output current is increased to 250 or -300 μA respectively. This boost circuit allows for rapid changes to line or load transients by increasing the dv/dt of the output capacitance of the amplifier.

Power Error Amplifier The power loop has a low bandwidth error amplifier which is referred to as the “Power Amp”. This amplifier performs a similar function to the Error Amp, only it generates an error signal that holds the power to a constant level.

The power error amplifier has a nominal gain of 100 umhos (or 0.0001 amps/volts). The maximum output current for this amplifier in its normal operating range is 20 μA. It is also a switched gain transconductance amplifier similar to the voltage error amplifier, however, the thresholds are different.

AC Error Amplifier The third error amplifier, is the “AC error amp”. It requires a higher bandwidth than the voltage or power error amplifiers. This amplifier forces a signal which is the sum of the current and input voltage to equal the AC reference signal from the reference multiplier.

The AC error amplifier has a nominal gain of 100 umhos (or 0.0001 amps/volt). The maximum output current for this amplifier in its normal operating range is 20 μA. This

amplifier does not contain a boost circuit, and has a constant transconductance across its operating range.

Voltage and Power ORing Network

The ORing network for the voltage and power amplifiers are inverting transconductance amplifiers. The network uses an internal reference of approximately 3.0 volts. Its gain is:

$$I_{out} = (V_{ref} - V_{in}) \cdot \frac{4}{12.5\text{ k}} = \frac{3\text{ V} - V_{in}}{3,125}$$

Where the 12.5 k is the internal resistor, and 4 is the gain of the current mirror.

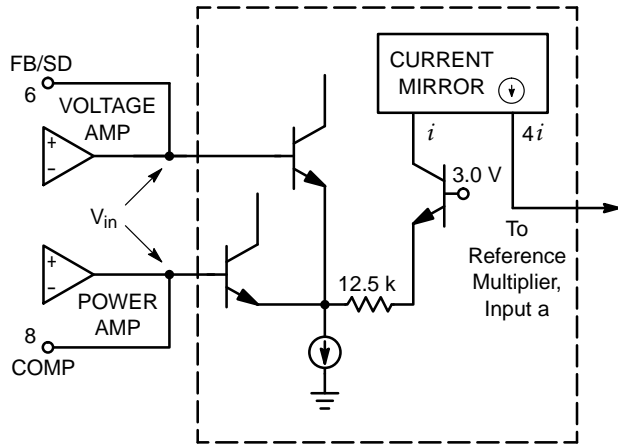


Figure 37. Voltage/Power ORing Network

The amplifier (voltage or power) with the highest output voltage will control the loop, as the buffer transistor from the other amplifier will be in cutoff. As the output voltage of an amplifier increases, its contribution to the current sink will increase, and the current driving the current mirror will decrease, thus the output of the current mirror will decrease.

The current mirror output feeds the analog (a) input to the reference multiplier.

Overvoltage Comparator

For a load transient, in which the current is suddenly reduced, the output voltage will overshoot. This circuit, will minimize the overshoot, and effectively decrease the response time of the loop.

A comparator is provided to monitor the feedback voltage and shut down the PWM in the event that the output exceeds 8% of the designed output voltage. The feedback voltage is supplied to this comparator from pin 6, which is the same signal that the voltage error amplifier uses to regulate the DC voltage loop.

Current Sense Amplifier

The current sense amplifier is a wide bandwidth amplifier with a differential input. It consists of a differential input stage, a high frequency current mirror and a low frequency current mirror, for a total of three current outputs. Two of them (AC Error Amplifier and Power Multiplier) are generated from the i_2 mirror, and their waveforms have been filtered to resemble the average value of the input current. The third output is the instantaneous inductor current and is generated from the i_1 mirror which directly feeds the input of the PWM.

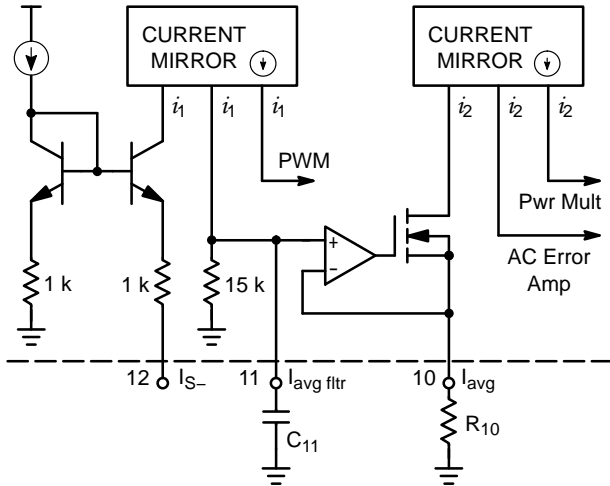


Figure 38. Current Sense Amplifier

The input to the current sense amplifier is a common base configuration. The voltage developed across the current shunt is sensed at the I_{S-} input. The amplifier input is designed for negative going voltages only; the power stage should resemble the configuration of the circuit in Figure 39.

Caution should be exercised when designing a filter between the shunt resistor and this input, due to the low impedance of this amplifier. Any series resistance due to a filter, will create an offset of:

$$V_{OS} = 50 \mu A \times R_{external}$$

which will add a negative offset to the current signal. The effect of this is that current information will be lost when the current signal is below the offset level. This will be a problem mainly at light loads and near the zero crossings.

The voltage across the current shunt resistor is converted into a current (i_1), which drives a current mirror. The output of the i_1 current mirror is a high frequency signal that is a replica of the instantaneous current in the inductor. The conversion of the current sense signal to current i_1 is:

$$i_1 = V_{I_{S-}} / 1 k$$

The PWM output sends that information directly to the PWM input where it is added to the AC error amp signal and the ramp compensation signal.

The other output of the i_1 mirror provides a voltage signal to a buffer amplifier. This signal is the result of i_1 dropped

across an internal 15 kW resistor, and filtered by a capacitor at pin 11. This signal, when properly filtered, will be the 2x line frequency fullwave rectified sinewave. The filter pole on pin 11 should be far enough below the switching frequency to remove most of the high frequency component, but high enough above the line frequency so as not to cause significant distortion to the input fullwave rectified sinewave waveform.

For a 100 kHz switching frequency and a 60 Hz line frequency, a 10 kHz pole will normally work well. The capacitor at pin 11 can be calculated knowing the desired pole frequency by the equation:

$$C_{11} = \frac{10.5}{f}$$

Where:

C_{11} = Pin 11 capacitance (nF)

f = pole frequency (kHz)

or, for a 10 kHz pole, C_{11} would be 1.0 nF.

The gain of the low frequency current buffer is set by the value of the resistor at pin 10. The value of R_{10} affects the operation of the AC error amplifier as well as the maximum power level. Power multiplier gain calculations are included in the description of that circuit.

PWM and Logic

The PWM and logic circuits are comprised of a PWM comparator, an RS flip-flop (latch) and an OR gate. The latch has two Set inputs and one Reset input. The Reset input is dominant over the PWM Set input, but the Overshoot Comparator Set input is dominant over the Reset input. The two Set Inputs are effectively OR'ed together although their dominance varies.

The NCP1650 uses a standard Pulse Width Modulation scheme based on a fixed frequency oscillator. The oscillator outputs a ramp waveform as well as a pulse which is coincident with the falling edge of the ramp. The pulse is fed into the PWM latch and AND gate that follows. During the pulse, the latch is reset, and the output drive is in it's low state.

On the falling edge of the pulse, the output drive goes high and the power switch begins conduction. The instantaneous inductor current is summed with the AC error amplifier voltage and the ramp compensation signal to create a complex waveform that is compared to the 4.0 volt reference signal on the inverting input to the PWM comparator. When the signal at the non-inverting input to the PWM comparator exceeds 4.0 volts, the output of the PWM comparator changes to a high state which drives one of the Set inputs to the latch and turns the power switch off until the next oscillator cycle. Figure 40 shows the relationships of the oscillator and logic signals.

There are two override signals to the normal cycle-by-cycle PWM operation. The UVLO circuit feeds directly into the AND gate and will inhibit operation until the input voltage is in a valid range. The Overshoot

Comparator monitors the output voltage and will shutdown operation of the PWM circuit if the output voltage exceeds 8% above the normal regulation level. The Overshoot Comparator signal is fed into the second Set input to the latch.

AC Reference Buffer

The AC reference buffer converts the voltage generated by the AC error amplifier to be converted into a current to be summed with the ramp compensation signal and the instantaneous current signal.

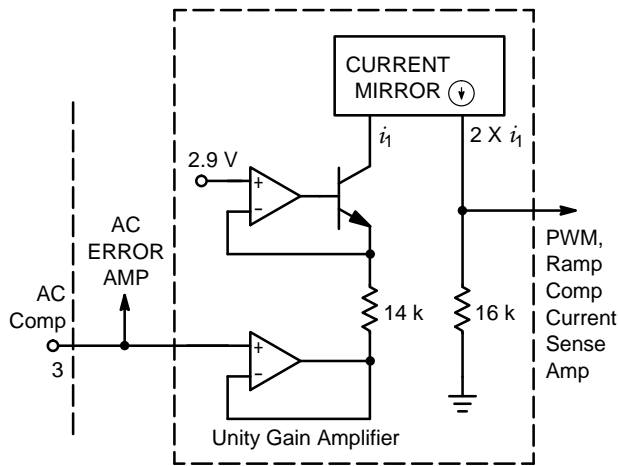


Figure 39. AC Reference Buffer Schematic

The buffer’s transfer function is:

$$i_{out} = (2.9\text{ V} - V_{ac})/7\text{ k}$$

The buffer amplifier, converts the input voltage to a current by creating a current equal to the voltage difference between the AC error amplifier output and the 2.9 volt reference dropped across the 14 kΩ resistor. The bipolar transistor level shifts the voltage and maintains the proper current into the current mirror. The current mirror has a 1:2 ratio and delivers the output current to the PWM input. This current is summed with the currents of the ramp compensation signal and the instantaneous current signal to determine the turn-off point in the switching cycle.

Soft-Start Circuit

The AC error amplifier has been configured such that a low output level will cause the output duty cycle to go to zero. This will have the effect of soft-starting the unit at turn-on, since the output is coupled to ground through a capacitor.

There will be an initial offset of the output voltage due to the output current and the resistor at pin 3. For example, if the output is saturated in the high state at turn on, it will source 50 μA. If pin 3 is terminated with a 2.2 kΩ resistor and a 0.01 F capacitor, the initial step will be:

$$50\ \mu\text{A} \times 2.2\ \text{k} = 0.11\ \text{volts}$$

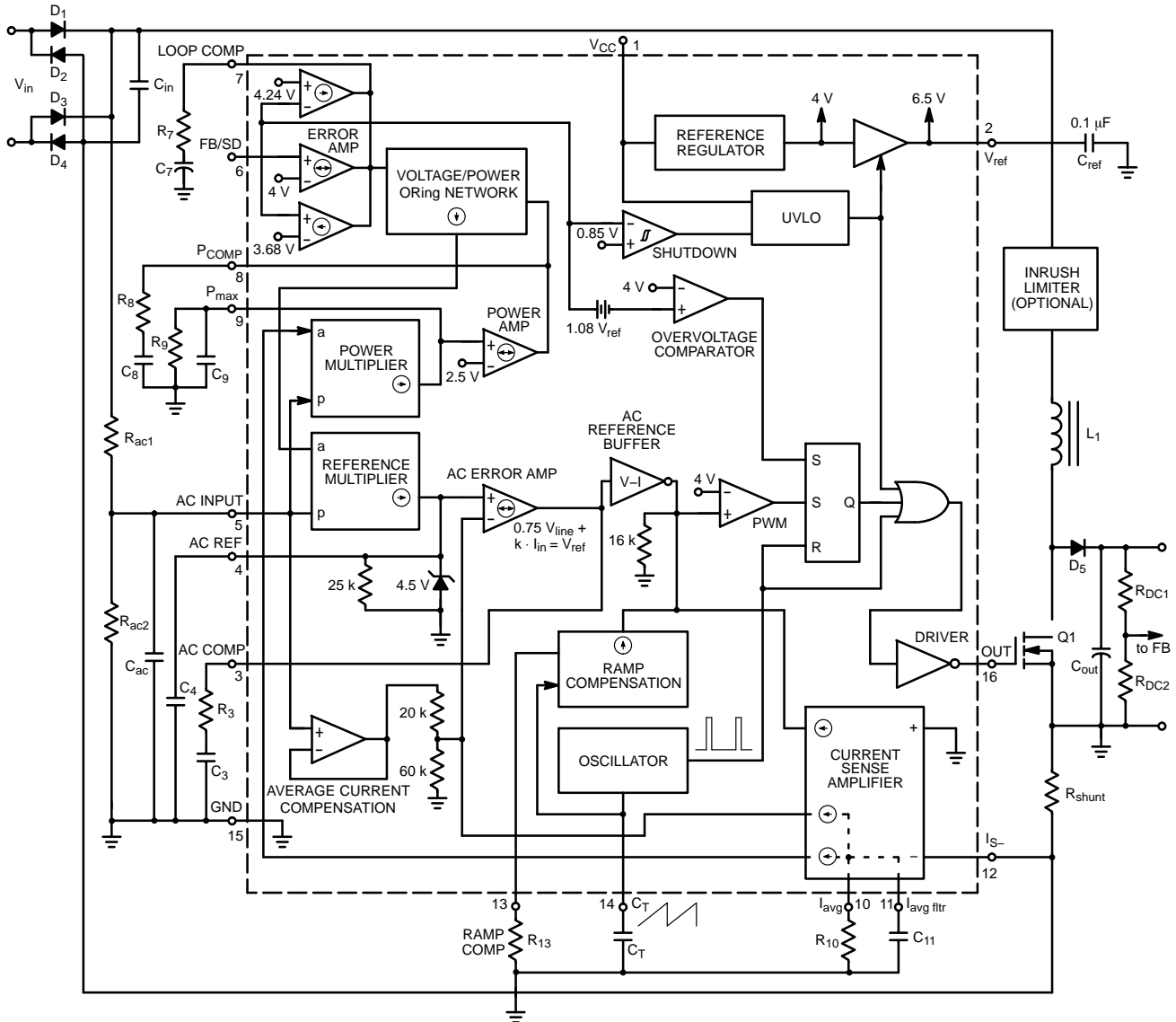
and the rate of rise will be:

$$50\ \mu\text{A}/0.01\ \mu\text{F} = 5\ \text{mv}/\mu\text{s}$$

or, 560 μs until the output is at 2.9 volts, which corresponds to full duty cycle.

An external soft-start circuit can be added, as shown in Figure 29, if additional time is desired.

DESIGN GUIDELINES



Note: This is a theoretical design, and it is not implied that a circuit designed by this procedure will operate properly without normal troubleshooting and adjustments as are common with any power conversion circuit. ON Semiconductor provides a spread sheet that incorporates the following equations, and will calculate the bias components for a circuit using the above schematic.

Figure 40. Typical Application Schematic

Basic Specifications

The design of any power converter begins with a basic set of specifications. As a minimum, the following parameters should be known before beginning:

- P_{Omax} (Maximum rated output power)
- V_{rmsmin} (Minimum operational line voltage)
- V_{rmsmax} (Maximum operational line voltage)
- f_{switch} (Nominal switching frequency)
- V_{out} (Nominal regulated output voltage)

Most of these parameters will be dictated by system requirements. The output voltage may not be defined. In general, it should be slightly greater than the peak of the line waveform at high line. For a 265 v_{rms} input, the peak line

voltage would be 375 volts, and 400 volts is a standard output voltage. In no case should it be less than the peak input line voltage.

Inductor

For an average current mode, fixed frequency PFC converter, there is no magic formula to determine the optimum value of the inductor. There are several trade-off's that should be considered. These include peak current vs. average current, and switching losses vs. core losses. All of these are a function of inductance, line and load. These parameters determine when the converter is operating in the continuous conduction mode and when it is operating in the discontinuous conduction mode.

For a first approach, the following formula will give the inductance value that will cause the peak current to be a fraction of the peak line frequency current.

$$L = \frac{T \cdot V_{in}^2}{2 \cdot I\% \cdot P_{out}} \left(1 - \frac{\sqrt{2} \cdot V_{in}}{V_{out}} \right)$$

Where:

L is the inductance (μ H)

T is the switching period (μ s)

V_{in} is the minimum rms line voltage (v)

I% is the percent switching current ripple relative to the line current (.xx)

P_{out} is the maximum output power (w)

V_{out} is the output voltage (v)

So for the following unit:

$V_{in} = 85$ vrms

$V_{out} = 400$ VDC

$P_{max} = 1000$ watts

$T = 10$ μ s (100 kHz)

I% = .30

the inductance would be 84 μ H.

$$I_{max} = \frac{\sqrt{2} \cdot P_{out}}{V_{in}}$$

The maximum low frequency line current would be determined at full load and low line, or:

where the definitions of P_{out} and V_{in} are as in the above equation. For the above conditions, I_{max} would be 16.6 amps. The peak current in the inductor at full load and low line would be 30% greater than this, or 21.6 amps.

For thermal calculations the transformer will have to pass 11.8 amps rms, and not saturate with a peak current of 21.6 amps.

There are several options available for the design of inductors. You can contact a magnetics manufacturer, such as Coiltronics (cooperet.com) or inductor designs can be made simply with the use of programs such as the DC inductor design program from Magnetics Inc. This software is free at their website, www.mag-inc.com.

Using the equation provided, and the following variables:

$T = 10$ μ s ($f = 100$ kHz)

$V_{rms} = 265$ v

$V_o = 400$ VDC

$P_{max} = 1000$ watts

I% = 30

the inductance would be 74 μ H.

Using the ON Semiconductor spreadsheet, a value of 250 μ H allows for continuous mode operation at full load and most input voltages. At the high line value of 265 vac, the unit will operate in the continuous mode from 30° to 150°, and discontinuous when the input voltage is near zero.

Using information from the ON Semiconductor spreadsheet the inductor can either be specified to a magnetics company to design, or can be designed by the Magnetics Inc. software. In either case, the critical information for the inductor design, (inductance, maximum average current, peak-to-peak ripple current, and switching frequency) can be obtained from the spreadsheet.

If a secondary winding is desired to provide a bias supply, it should provide a minimum of 11.8 volts (to exceed the UVLO spec) and a maximum of 18 volts. The secondary should be connected such that it conducts when the power switch is off. This will create an output voltage that varies with the input voltage, and near the zero crossings of the line frequency will have a peak voltage equal to the regulated output voltage divided by the turns ratio. The filter cap on the Vcc pin needs to be of sufficient size to hold the voltage up over between the zero crossings.

Oscillator

The relationship between the frequency and timing capacitor is:

$$C_T = 47,000/f$$

Where C_T is in pF and f is in kHz.

AC Voltage Divider

The voltage divider from the input rectifiers to ground is a simple but important calculation. For this calculation it is necessary to know the maximum line that the unit can operate at. The peak input voltage will be:

$$V_{inpeak} = 1.414 \times V_{rms\ max}$$

The maximum voltage at the AC input (pin 5) is 3.75 volts (this is true for both multipliers).

If the maximum line voltage is 265 vac, the peak input voltage is:

$$V_{inpeak} = 1.414 \times 265\ V_{rms} = 375\ V_{pk}$$

To keep the power dissipation reasonable for a 1/2 watt resistor (R_{ac1}), it should dissipate no more than 1/4 watt. Depending on environmental conditions, further derating may be required. The power in this resistor is:

$$P_{Rac1} = (375\ v - 3.75\ v)^2 / R_{ac1} = .25\ watts$$

$$\text{so : } R_{ac1} = 551\ kOhms$$

To minimize dissipation, use the next largest standard value, or 560 kOhms.

$$\text{Then, } R_{ac2} = 3.75\ v / ((375\ v - 3.75\ v) / 560\ k) = 5.6\ kOhms$$

Current Sense Resistor/Ramp Compensation

The combination of the voltage developed across the current sense resistor and ramp compensation signal, will determine the peak instantaneous current that the power switch will be allowed to conduct before it is turned off.

The vector sum of the three signals that combine to create the signal at the non-inverting input to the PWM comparator must add up to 4.0 volts in order to terminate the switch cycle. These signals are the error signal from the AC error amp, the ramp compensation signal, and the instantaneous current. For a worst case condition, the output of the AC error amp could be zero (current), which would require that the sum of the ramp compensation signal and current signal be 4.0 volts. This must be evaluated under full load and low line conditions.

Equation 1)

$$V_{R_{COMP}} = \frac{1.6 * V_{osc_{pk}} * 16 \text{ k}}{R_{RC}}$$

Where: $V_{osc_{pk}} = 4.0 \text{ V}$

$$V_{R_{COMP}} = \frac{1.6 * 4 * 16 \text{ k}}{R_{RC}} = \frac{102,400}{R_{RC}}$$

For proper ramp compensation, the ramp signal should match the falling di/dt (which has been converted to a dv/dt) of the inductor at 50% duty cycle. 50% duty cycle will occur when the input voltage is 50% of the output voltage. Thus the following equations must be satisfied:

Equation 2)

$$\frac{di}{dt} * T * R_S * \text{High Frequency Current Gain}$$

$$\frac{V_o * T * R_S * 16}{L * 2} = \frac{102,400}{R_{RC}}$$

$$R_S = \frac{12800 * L}{V_o * T * R_{RC}}$$

R_S = Shunt resistance (Ω)

P_O = Output power (W)

L = Inductance (H)

$$t_{on} = T \left(1 - \frac{\sqrt{2} \cdot V_{inLL}}{V_{out}} \right)$$

Where: t_{on} = Switch on time (s)

T = Period (s)

V_{inLL} = Low line input voltage (Vrms)

V_{out} = DC output voltage (V)

$$i_{pk} = \frac{\sqrt{2} \cdot P_{in}}{V_{inLL}} + \frac{V_{inLL} \cdot t_{on}}{\sqrt{2} \cdot L}$$

Ramp Compensation:

Equation 3)

$$V_{ref_{pwm}} = V_{inst} + V_{R_{COMP}}$$

Where: $V_{ref_{pwm}} = 3.8 \text{ V}$

$$3.8 = (i_{pk} * R_S * 16 + \frac{102,400}{R_{RC}}) * \frac{t_{on}}{T}$$

$$R_{RC} = \frac{102,400}{(3.8 - (16 * i_{pk} * R_S)) * \frac{t_{on}}{T}}$$

Where:

R_S = Shunt resistance (Ω)

L = Inductance (H)

V_{out} = Output voltage (V)

R_{RC} = Ramp comp resistor (k Ω)

Current Shunt:

Equation 4)

Combining equations 2 and 3:

$$R_S = \frac{12800 * L}{V_o * T * R_{RC}} * \frac{T}{t_{on}} * \frac{(3.8 - 16 * i_{pk} * R_S)}{102,400}$$

$$R_S = \frac{3.8}{\left(\frac{8 * V_o * t_{on}}{L} \right) + (16 * i_{pk})}$$

Solve for R_S and then R_{RC} , using the above equations. It should be understood that these equations do not take into account tolerances of the inductor, switching frequency, etc...

The shunt should be a non-wirewound (low inductance) type of resistor. There are several types of metal film resistors available for shunt applications.

Current Scaling Resistor and Filter Capacitor

R_{10} sets the gain of the averaged current signal out of the current sense amplifier. This signal is fed into the AC error amplifier and is also used in the power multiplier. R_{10} is used to scale the current to the appropriate level for protection purposes in the AC error amplifier circuit. The power multiplier has an external resistor, R_9 that will adjust the gain of that circuit.

R_{10} should be calculated to limit the maximum current signal at the input to the AC error amplifier to less than 4.5 volts at low line and full load. 4.5 volts is the clamp voltage at the output of the reference amplifier and limits the maximum averaged current that the unit can process. The equation for R_{10} is:

$$R_{10} = \frac{318,200 \cdot P_{in} \cdot R_S / V_{inLL}}{4.5 - (1.06 \cdot V_{inLL} \cdot AC_{ratio})}$$

Where:

P_{in} = rated input power (w)

R_S = Shunt resistance (W)

V_{inLL} = min. operating rms input voltage (v)

AC_{ratio} = AC attenuation factor at pin 5

This equation does not allow for tolerances, and it would be advisable to increase the input power to assure operation at maximum power over production tolerance variations.

The current sense filter capacitor should be selected to set its pole about a factor of 10 below the switching frequency.

$$C_{11} = \frac{10.6}{f}$$

Where:

C_{11} = Pin 11 capacitance (nF)

f = pole frequency (kHz)

so, for a 100 kHz switching frequency, a 10 kHz pole is desirable, and C_{11} would be 1.0 nF.

Maximum Power Circuit

The power multiplier multiplies the input voltage, current and a scale factor, to output a value that is proportional to the input power. This voltage is filtered to remove the line frequency components. The resulting output is compared to the 2.5 volt reference on the power error amplifier. When the output of the multiplier reaches 2.5 volts the power loop takes control and will reduce the output voltage as necessary, but can not reduce it to less than the peak of the line voltage.

For proper operation, resistor R_9 should be chosen such that the unit will power limit at a value slightly greater than the maximum power desired. R_9 can be calculated by the formula:

$$R_9 = \frac{V_9 R_{10}}{AC_{ratio} Pin RS 3.75}$$

Where:

V_9 = Power reference voltage (2.5 v nom)

R_{10} = Current scaling resistor (Ω)

AC_{ratio} = AC attenuation factor at pin 5

Pin = rated input power (w)

RS = Shunt resistance (W)

The NCP1650 has been designed such that with a 2% current shunt and a 1% AC divider, the RSS error will be 7% maximum, or a worst case error of 14%. In order to assure maximum power output the reference voltage (V_9) should be reduced by the error factor.

The output signal from the power multiplier should be close to a DC level, so a filter cap needs to be added with a high frequency pole relative to the line frequency. For a 60 Hz line, a 0.6 Hz pole would allow 40 dB of attenuation, or .01 which would reduce a 5.0 volt p-p signal to a DC level of 2.5 volts, with 50 mv of ripple. The chosen frequency will be a tradeoff of response time vs. ripple. For a pole of 0.6 Hz:

$$C_9 = \frac{1}{2 \cdot \pi \cdot R_9 \cdot 0.6} = \frac{0.265}{R_9}$$

Where:

C_9 = Pin 9 capacitance (F)

R_9 = Pin 9 resistance (Ω)

Reference Multiplier

The output of the reference multiplier is a pulse width modulated representation of the analog input. The multiplier is internally loaded with a resistor to ground which will set the DC gain. An external capacitor is required to filter the signal back into one that resembles the input fullwave rectified sinewave. The pole for this circuit should be greater than the line frequency and lower than the switching frequency.

1/15th of the switching frequency is a recommended starting value for a 60 Hz line frequency. The filter capacitor for pin 4 can be determined by the following equation:

$$C_4 = \frac{1}{2 \cdot \pi \cdot 25 k \cdot f_{pole}} = \frac{6.366E - 6}{f_{pole}}$$

C_4 = Pin 4 capacitance (F)

f_{pole} = Ref gain pole freq (Hz)

AC Error Amplifier

The AC error amplifier is a transconductance amplifier that is terminated with a series RC impedance. This creates a pole-zero pair.

To determine the values of R_3 and C_3 , it is necessary to look at the two signals that reach the PWM inputs. The non-inverting input is a slow loop using the averaged current signal. Its gain is:

$$A_{if} = \frac{15 k}{1 k} \cdot \frac{15 k}{R_{10}} \cdot (g_m \cdot R_3) \cdot 2.3$$

Where the first two terms are the gains in the current sense amplifier averaging circuit. The next term is the gain of the transconductance amplifier and the constant is the gain of the AC Reference Buffer.

The high frequency path is that of the instantaneous current signal to the PWM non-inverting input. This gain is simply 16, since the input signal is converted to a current through a 1 k resistor, and then terminated by the 16 k resistor at the PWM input.

For stability, the gain of the low frequency path must be less than the gain of the high frequency path. This can be written as:

$$\frac{517,500 \cdot g_m \cdot R_3}{R_{10}} < 16$$

The suggested resistor and capacitor values are:

$$R_3 = \frac{R_{10}}{56,000 g_m}$$

and for a zero at 1/10th of the switching frequency

$$C_3 = \frac{1.59}{f_{sw} R_3}$$

Where:

R_3 and R_{10} are in units of Ω

g_m is in units of mhos

C_3 is in Farads

f_{sw} is in Hz

Loop Compensation

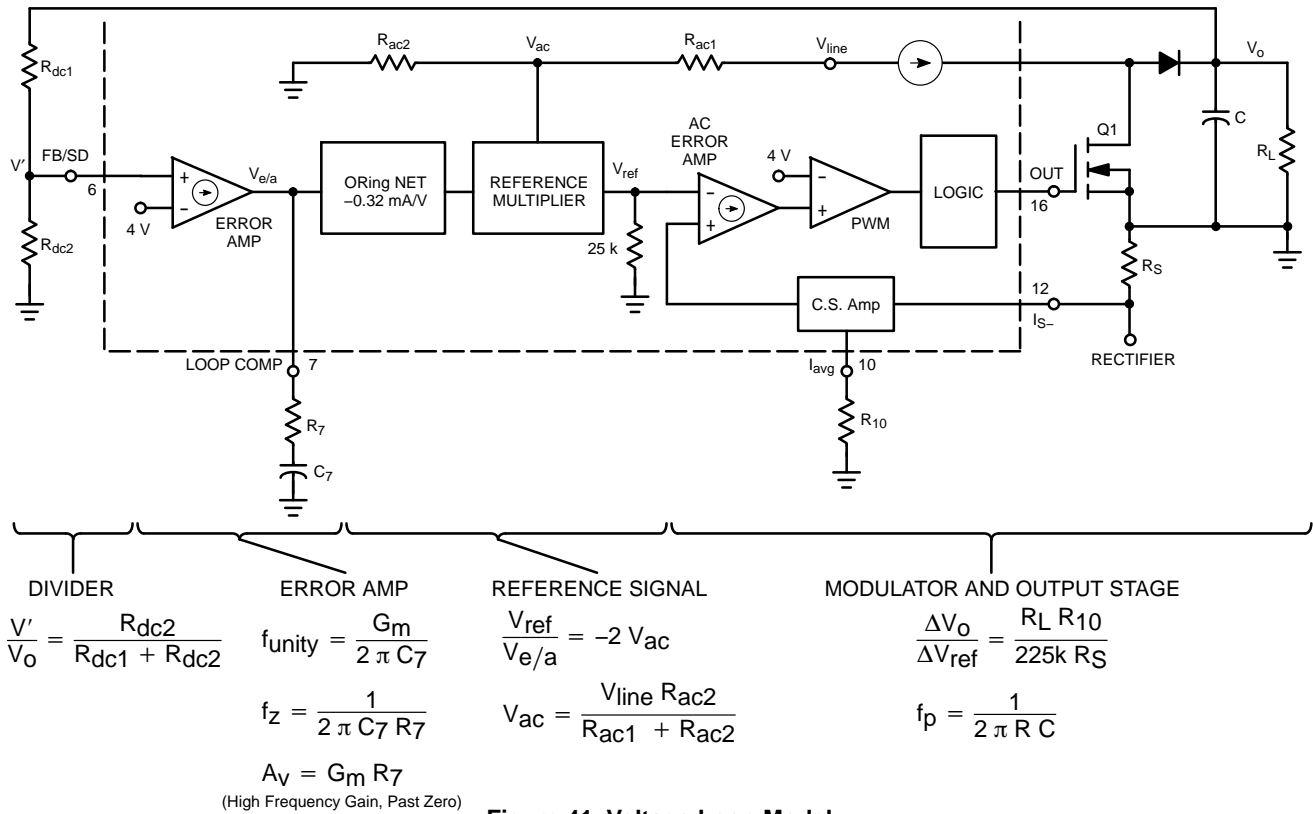


Figure 41. Voltage Loop Model

Voltage Loop

Block Diagram

The block diagram for the voltage loop has been broken down into four sections. These are the voltage divider, voltage error amplifier, reference signal and modulator and output stage.

The modulator and output stage circuitry is greatly simplified based on the assumption that that poles and zeros in the current feedback loop are considerably greater than the bandwidth of the overall loop. This should be a good assumption, because a bandwidth in the kilohertz is necessary for a good current waveform, and the voltage error amplifier needs to have a bandwidth of less than the lowest line frequency that will be used.

There are two poles in this circuit. The output filter has a pole that varies with the load. The pole on the voltage error amplifier will be determined by this analysis.

Voltage Divider

The voltage divider is a simple resistive divider that reduces the output voltage to the 4.0 volt level required by the internal reference on the voltage error amplifier.

Voltage Error Amplifier

The voltage error amplifier is constrained by the three equations. When this amplifier is compensated with a pole-zero pair, there will be a unity gain pole which will be cancelled by the zero at frequency f_z. The corresponding bode plot would be:

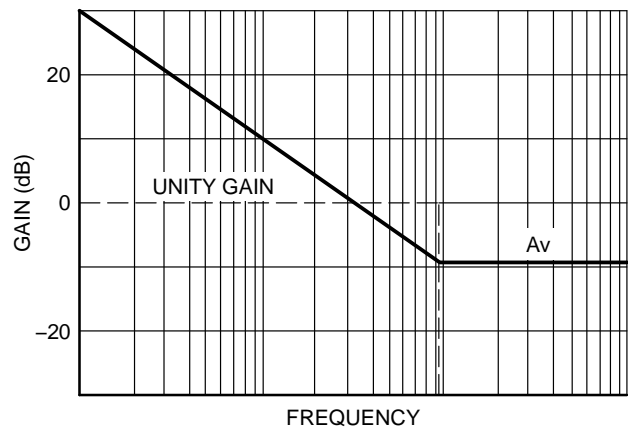


Figure 42. Pole-Zero Bode Plot

Reference Signal

The output of the error amplifier is modified by the ORing network, which has a negative gain, and is then used as an input to the reference multiplier. The gain of this block is dependent on the AC input voltage, because of the multiplier which requires two inputs for one output.

Modulator and Output Stage

The AC error amplifier receives an input from the reference multiplier and forces the current to follow the shape and amplitude of the reference signal. The current shaping circuit is an internal loop within this section due to the current sense amplifier. Based on the assumptions listed

in the introduction to this analysis, this is not analyzed separately.

The equation for the gain is good for frequencies below the pole. There is a single pole due to the output filter. Since the NCP1650 is a current mode converter, the inductor is not part of the output pole as can be seen in that equation.

Calculating the Loop Gain

At this point in the design process, all of the parameters involved in this calculation have been determined with the exception of the pole-zero pair on the output of the voltage error amplifier.

All equations give gains in absolute numbers. It is necessary to convert these to the decibel format using the following formula:

$$A(\text{dB}) = 20 \text{ Log}_{10} (A)$$

For example, the voltage divider would be:

$$A = \frac{5.6 \text{ k}}{560 \text{ k} + 5.6 \text{ k}} = .0099$$

$$A(\text{dB}) = 20 \text{ Log}_{10} .0099 = -40 \text{ dB}$$

The gain of the loop will vary as the input voltage changes. It is recommended that the compensation for the voltage error amplifier be calculated under high line, full load conditions. This should be the greatest bandwidth that the unit will see.

By necessity, the unity gain (0dB) loop bandwidth for a PFC unit, must be less than the line frequency. If the bandwidth approaches or exceeds the line frequency, the voltage error amplifier signal will have frequency components in its output that are greater than the line frequency. These components will cause distortion in the output of the reference amplifier, which is used to shape the current waveform. This in turn will cause distortion in the current and reduce the power factor.

Typically the maximum bandwidth for a 60 Hz PFC converter is 10 Hz, and slightly less for a 50 Hz system. This can be adjusted to meet the particular requirements of a system. The unity gain bandwidth is determined by the frequency at which the loop gain passes through the 0 dB level.

For stability purposes, the gain should pass through 0 dB with a slope of -20 dB/decade for approximately one decade on either side of the unity gain frequency. This assures a phase margin of greater than 45°.

The gain can be calculated graphically using the equations of Figure 43 as follows:

Divider: Calculate V'/V_o in dB, this value is constant so it will not change with frequency.

Reference Signal: Calculate $V_{\text{ref}}/V_{e/a}$ using the peak level of the AC input signal at high line that will be seen on pin 5. Convert this to dB. This is also a constant value.

Modulator and Output Stage: Calculate the gain in dB for DV_o/DV_{ref} . Calculate the pole frequency. The gain will be constant for all frequencies less than f_p . Starting at the pole frequency, this gain will drop off at a rate of 20 dB/decade.

Plot the sum of these three values. Figure 43 shows a gain of 35.5 dB until the pole of the output filter is reached at 0.3 Hz. After that, the gain is reduced at a rate of 20 dB/decade.

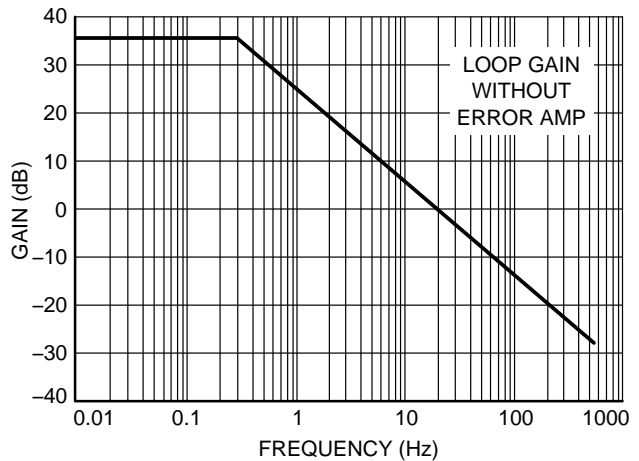


Figure 43. Open Loop Gain Less Error Amp

A typical error amplifier bode plot is shown in Figure 44. The zero is used to offset the pole of the output filter. The output filter pole will typically be lower than the unity gain loop bandwidth, so the zero will be necessary.

This plot shows a forward gain of 7.0 dB at 10 Hz. To compensate for this the error amplifier should have a gain of -7.0 dB (0.45) at 10 Hz, and a zero at 0.4 Hz. The gain at 10 Hz is determined by the resistor since it is well past the zero. The resistor can be calculated by the equation:

$$R_7 = A_v/G_m = .45/.0001 = 4.5 \text{ k}\Omega$$

4.7 kW is the closest standard value. Using this, the capacitor can be calculated based on the zero frequency of 0.4 Hz. This would give a value for C_7 of:

$$C = \frac{1}{2 \cdot \pi \cdot 4.7 \text{ k} \cdot 0.4 \text{ Hz}} = 85 \mu\text{F}$$

Using these values (4.7 kΩ and 86 μF), the open loop gain plot would be:

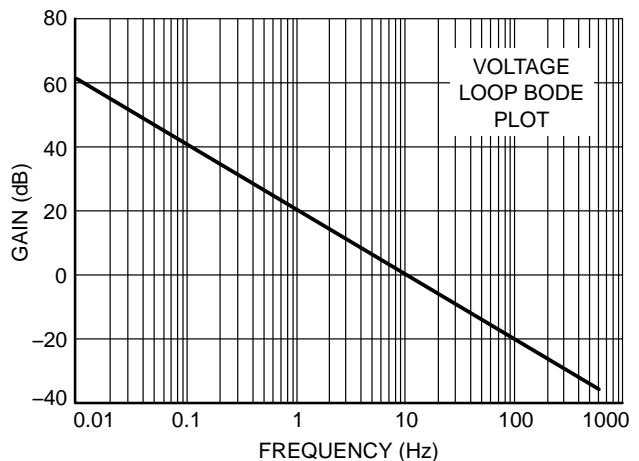
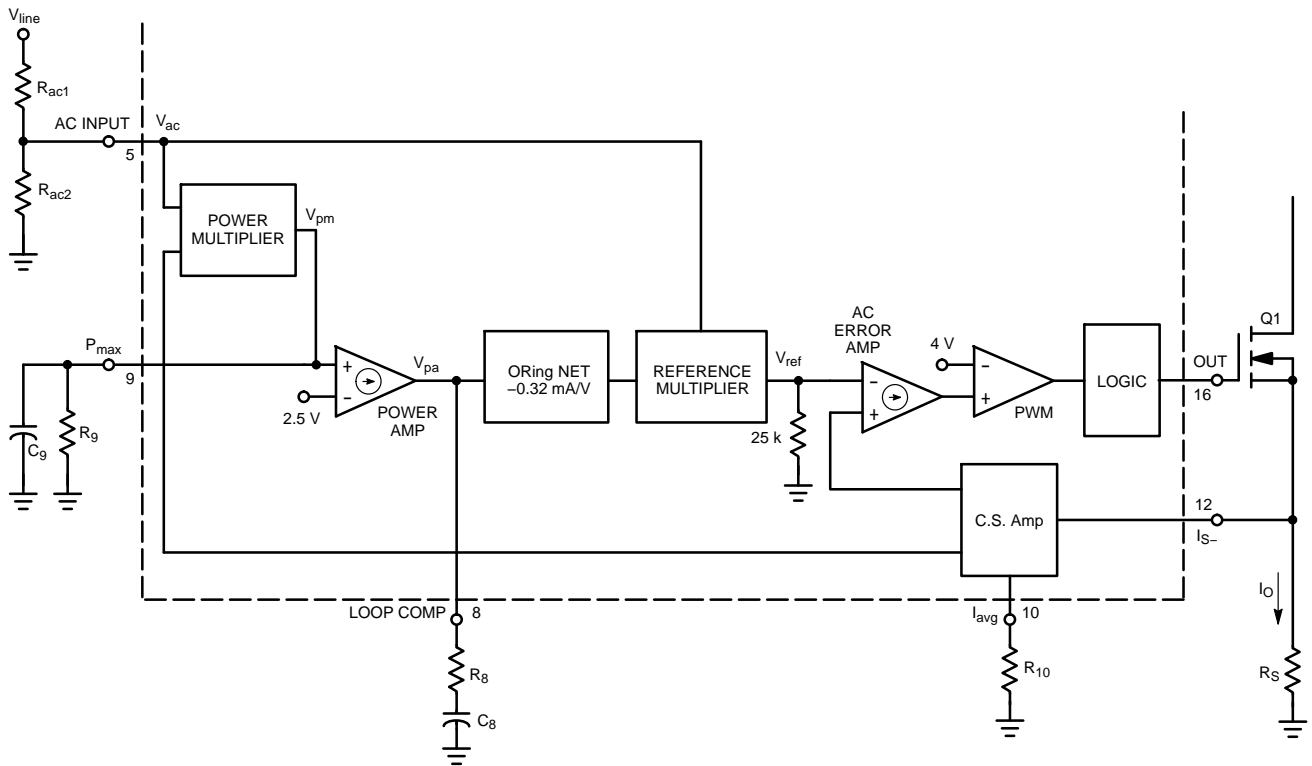


Figure 44. Open Loop Gain of Voltage Loop

NCP1650



POWER MULTIPLIER	POWER AMP	REFERENCE SIGNAL	MODULATOR AND OUTPUT STAGE
$\frac{V_{pm}}{i_o} = \frac{3.75 R_g V_{ac} R_S}{R_{10}}$	$A_V = \frac{G_m}{2 \pi f C_8}$	$\frac{V_{ref}}{V_{pa}} = -2 V_{ac}$	$\frac{i_o}{V_{ref}} = \frac{R_{10}}{225k R_S}$
$V_{ac} = \frac{V_{line} R_{ac2}}{R_{ac1} + R_{ac2}}$	$f_z = \frac{1}{2 \pi C_8 R_8}$	$V_{ac} = \frac{V_{line} R_{ac2}}{R_{ac1} + R_{ac2}}$	
$f_p = \frac{1}{2 \pi C_g R_g}$	$A_V = G_m R_8$ (High Frequency Gain, Past Zero)		

Figure 45. Power Loop Model

Power Loop

Block Diagram

The block diagram for the power loop has been broken down into four sections. These are the power multiplier, power amplifier, reference signal and modulator and output stage.

Similar to the voltage loop, the modulator and output stage circuitry has been greatly simplified due to the location of the associated poles and zeros.

There are two significant poles in this circuit. The first is on the power multiplier and the second is due to the power error amplifier. Because the pole on the power multiplier is very low, it will normally be necessary to include the resistor (R_g) for the zero on this amplifier.

Power Multiplier

The power multiplier's gain is a function of the input voltage. This multiplier has a very low frequency pole that must be considerably lower than the line frequency, so that the power signal is essentially a DC level.

Reference Signal

The reference signal block is unchanged from the voltage loop model.

Modulator and Output Stage

For the power circuit, the transfer function of the modulator and output circuitry follows the path from the AC reference voltage (V_{ref}) to the output current. Since this circuit regulates the power, and the input and output voltages are the two basic components of the power, the output current is the output variable for this block.

There is no pole associated with this function.

Power Amplifier

The compensation for this amplifier will be determined similar to the network for the voltage error amplifier. The series RC on pin 8 will create a pole-zero pair based on the equations given.

Calculating the Loop Gain

The power loop gain should be calculated using high line conditions. At lower lines the bandwidth will decrease.

Similar to the voltage loop, calculate the gains and power multiplier pole. Make sure that they are converted to dB's. Begin with all stages except the power amplifier, and determine what the gain of the power amplifier needs to be at the unity gain frequency. This loop is normally slower than the voltage loop and will generally be a factor of 5 to 10 lower in bandwidth.

The loop gain without the amplifier should resemble the following plot:

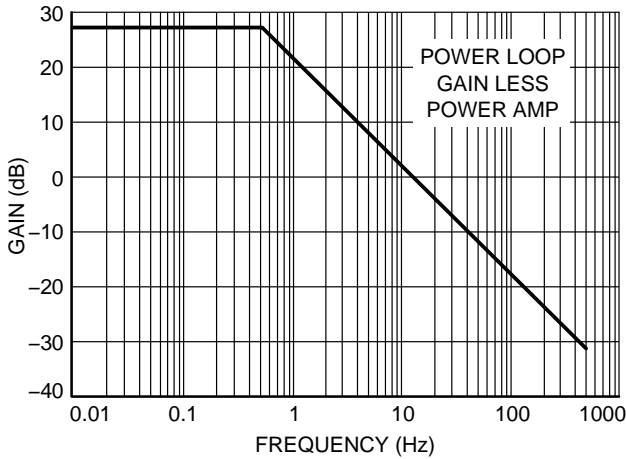


Figure 46. Power Loop without Power Amp

For this example it can be seen that for a bandwidth of 1.0 Hz, the power amplifier needs a gain of -27 dB (0.045 v/v) at 1.0 Hz, with a zero at 0.7 Hz. The zero frequency is chosen to match the pole frequency. Although it is not essential to do this, it is a safe method of assuring a stable system.

Since the frequency that we are interested in is greater than the zero frequency, the gain of the amplifier is:

$$A_v = G_m R_8$$

$$\text{or, } R_8 = A_v / G_m = 0.045 / .0001 = 446 \text{ Ohms}$$

a 470 Ohm resistor would be a good choice, and for a zero at 0.7 Hz:

$$C_8 = \frac{1}{2 \cdot \pi \cdot 470 \Omega \cdot 0.7 \text{ Hz}} = 483 \mu\text{F}$$

and a 470 μF cap would be a good choice. Using these two values, the resulting open loop plot would be:

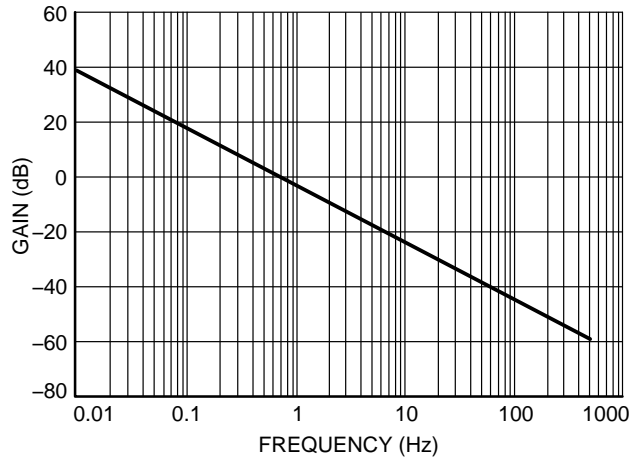


Figure 47. Power Circuit Open Loop Gain

As stated previously, these are calculated values, and may require adjustment in actual circuit conditions.



SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

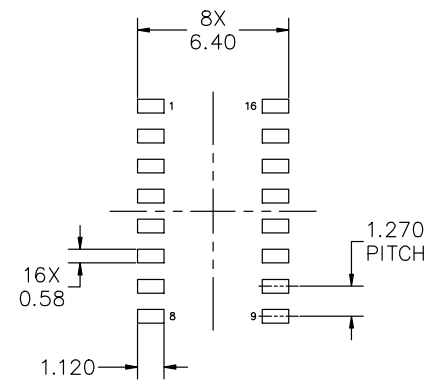
DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

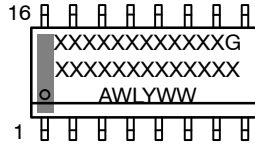
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DESCRIPTION:	SOIC-16 9.90X3.90X1.37 1.27P	PAGE 1 OF 2

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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

**GENERIC
MARKING DIAGRAM***



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH</p>	

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