

NDDL01N60Z, NDTL01N60Z

N-Channel Power MOSFET 600 V, 15 Ω

Features

- 100% Avalanche Tested
- Gate Charge Minimized
- Zener-protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	NDD	NDT	Unit
Drain-to-Source Voltage	V_{DSS}	600		V
Gate-to-Source Voltage	V_{GS}	± 30		V
Continuous Drain Current Steady State, $T_C = 25^\circ\text{C}$ (Note 1)	I_D	0.8	0.25	A
Continuous Drain Current Steady State, $T_C = 100^\circ\text{C}$ (Note 1)	I_D	0.5	0.15	A
Power Dissipation Steady State, $T_C = 25^\circ\text{C}$	P_D	26	2	W
Pulsed Drain Current, $t_p = 10 \mu\text{s}$	I_{DM}	3.4		A
Source Current (Body Diode)	I_S	2.5	1.7	A
Single Pulse Drain-to-Source Avalanche Energy ($I_D = 0.8 \text{ A}$)	EAS	12		mJ
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Lead Temperature for Soldering Leads	T_L	260		$^\circ\text{C}$
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by maximum junction temperature
2. $I_S = 1.5 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDDL1N60Z	$R_{\theta JC}$	4.8	$^\circ\text{C}/\text{W}$
Junction-to-Ambient (Note 4) NDDL1N60Z (Note 3) NDDL1N60Z-1 (Note 4) NDTL1N60Z (Note 5) NDTL1N60Z	$R_{\theta JA}$	42 96 62 151	$^\circ\text{C}/\text{W}$

3. Insertion mounted.
4. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces).
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

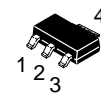
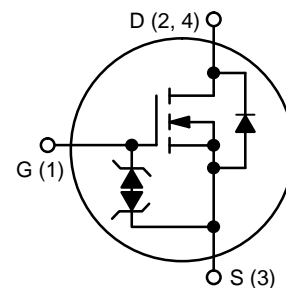


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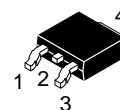
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$
600 V	15 Ω @ 10 V

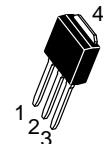
N-Channel MOSFET



SOT-223
CASE 318E
STYLE 3



DPAK
CASE 369C
STYLE 2



IPAK
CASE 369D
STYLE 2

MARKING & ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

NDDL01N60Z, NDTL01N60Z

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to $25^\circ\text{C}, I_D = 1\text{ mA}$		610		mV/ $^\circ\text{C}$
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		50	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 50\ \mu\text{A}$	3	4.0	4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			9.6		mV/ $^\circ\text{C}$
Static Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 0.4\text{ A}$		12.2	15	Ω
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 0.4\text{ A}$		0.7		S

CHARGES, CAPACITANCES & GATE RESISTANCES

Input Capacitance (Note 7)	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		92		pF
Output Capacitance (Note 7)	C_{oss}			13		
Reverse Transfer Capacitance (Note 7)	C_{rss}			3		
Effective output capacitance, energy related (Note 9)	$C_{o(er)}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }480\text{ V}$		5.5		pF
Effective output capacitance, time related (Note 10)	$C_{o(tr)}$	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }480\text{ V}$		8.1		
Total Gate Charge (Note 7)	Q_g	$V_{DS} = 300\text{ V}, I_D = 0.4\text{ A}, V_{GS} = 10\text{ V}$		4.9		nC
Gate-to-Source Charge (Note 7)	Q_{gs}			1.2		
Gate-to-Drain Charge (Note 7)	Q_{gd}			2.4		
Plateau Voltage	V_{GP}			5.8		V
Gate Resistance	R_g			6.6		Ω

SWITCHING CHARACTERISTICS (Note 8)

Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 0.4\text{ A}, V_{GS} = 10\text{ V}, R_G = 0\ \Omega$		10		ns
Rise Time	t_r			5		
Turn-off Delay Time	$t_{d(off)}$			13		
Fall Time	t_f			18		

DRAIN-SOURCE DIODE CHARACTERISTICS

Diode Forward Voltage	V_{SD}	$I_S = 0.4\text{ A}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 100^\circ\text{C}$		0.7		
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}, I_S = 1\text{ A}, d_i/d_t = 100\text{ A}/\mu\text{s}$		183		ns	
Charge Time	t_a			33			
Discharge Time	t_b			150			
Reverse Recovery Charge	Q_{rr}			255			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

7. Guaranteed by design.

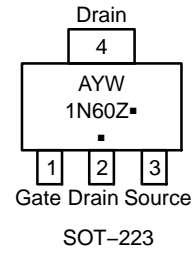
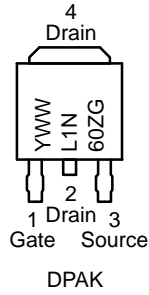
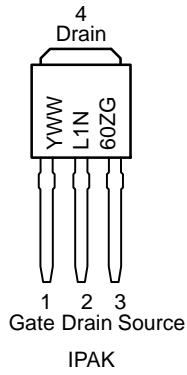
8. Switching characteristics are independent of operating junction temperatures.

9. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

10. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

NDDL01N60Z, NDTL01N60Z

MARKING DIAGRAMS



A = Assembly Location
 Y = Year
 W, WW = Work Week
 L1N60Z, 1N60Z = Specific Device Codes
 G or ■ = Pb-Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NDDL01N60Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDDL01N60ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel
NDTL01N60ZT1G	SOT-223 (Pb-Free, Halogen-Free)	1000 / Tape & Reel
NDTL01N60ZT3G	SOT-223 (Pb-Free, Halogen-Free)	4000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

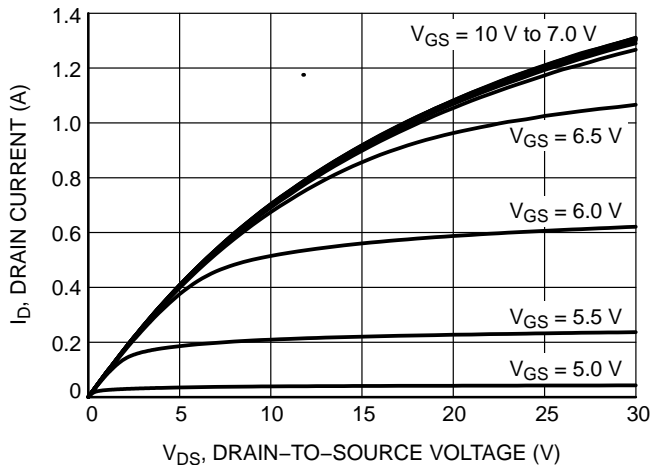


Figure 1. On-Region Characteristics

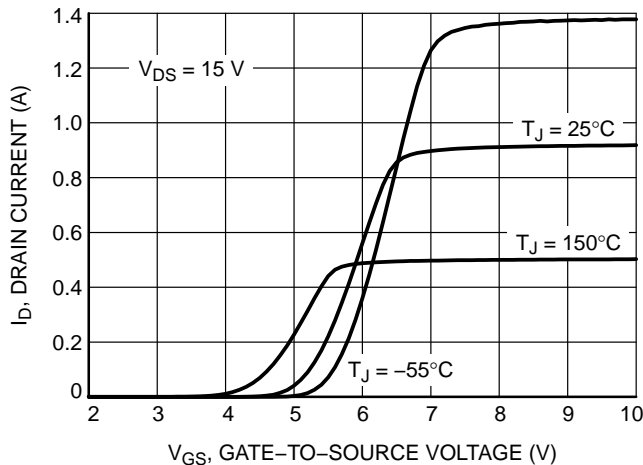


Figure 2. Transfer Characteristics

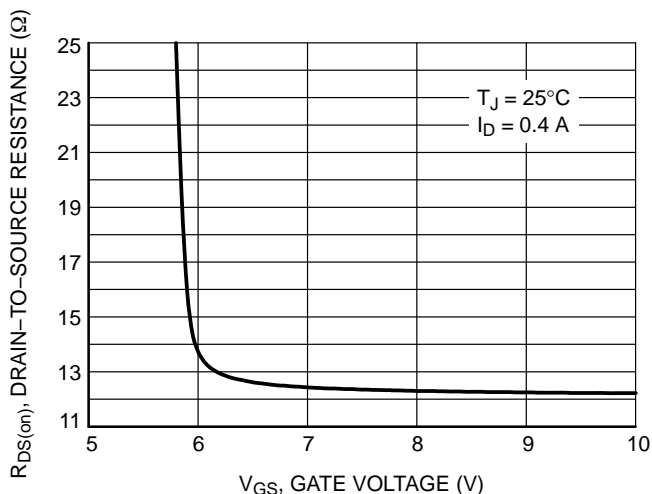


Figure 3. On-Resistance vs. Gate-to-Source Voltage

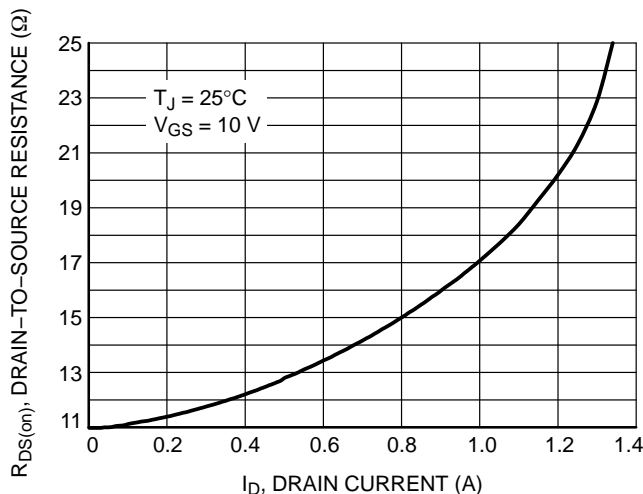


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

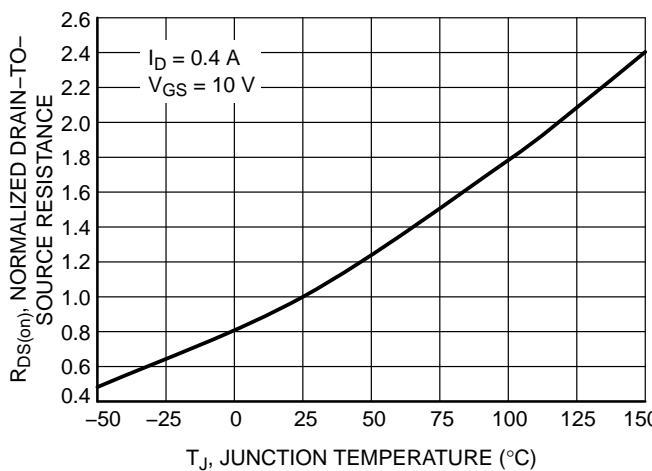


Figure 5. On-Resistance Variation with Temperature

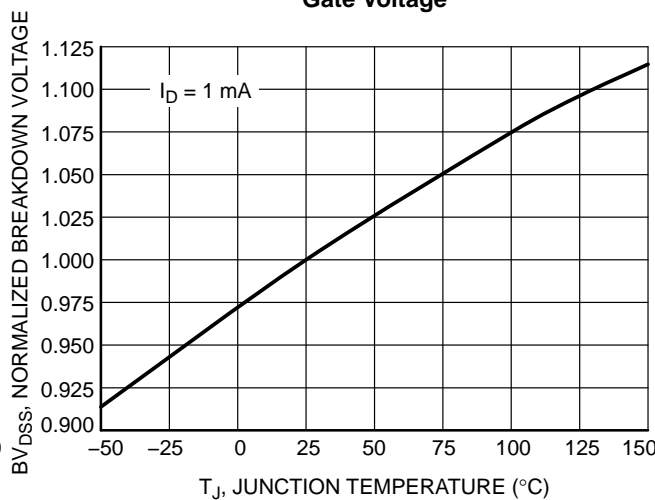


Figure 6. Breakdown Voltage Variation with Temperature

NDDL01N60Z, NDTL01N60Z

TYPICAL CHARACTERISTICS

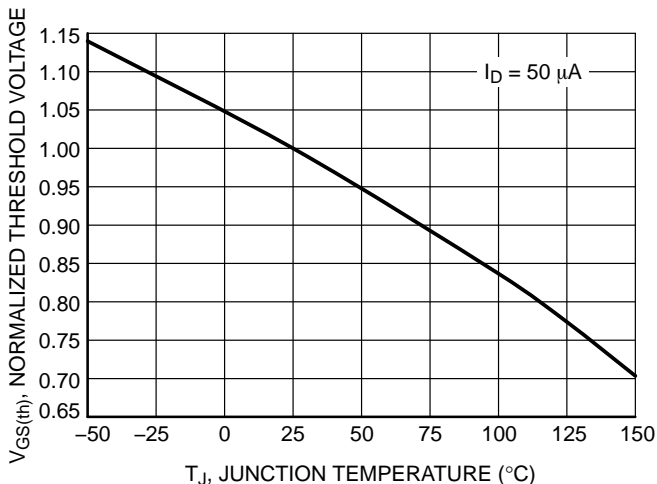


Figure 7. Threshold Voltage Variation with Temperature

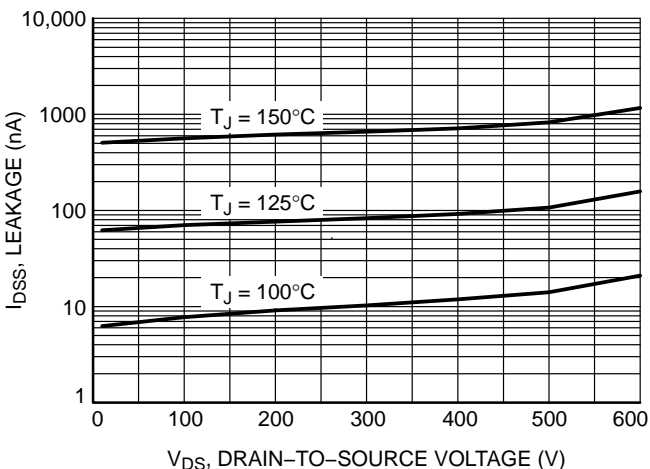


Figure 8. Drain-to-Source Leakage Current vs. Voltage

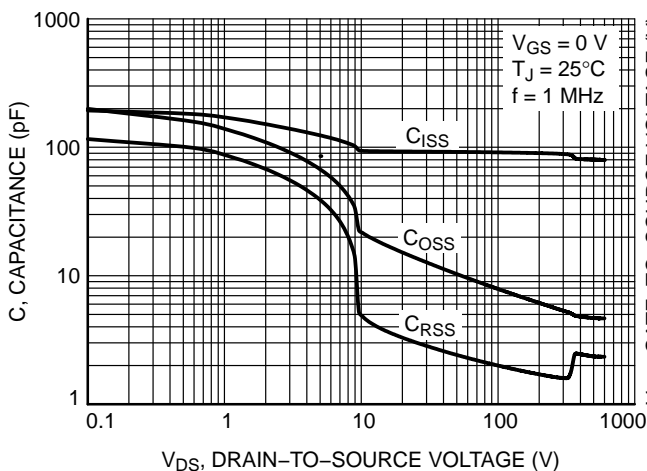


Figure 9. Capacitance Variation

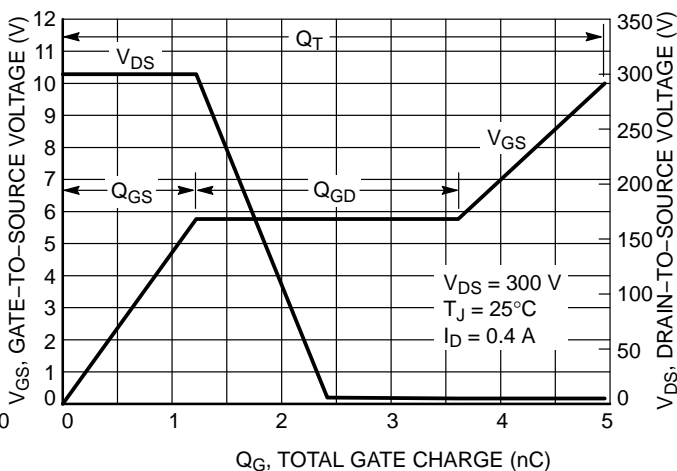


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

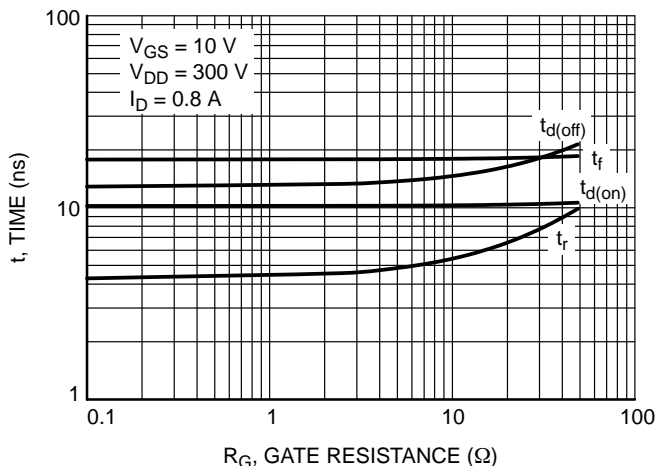


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

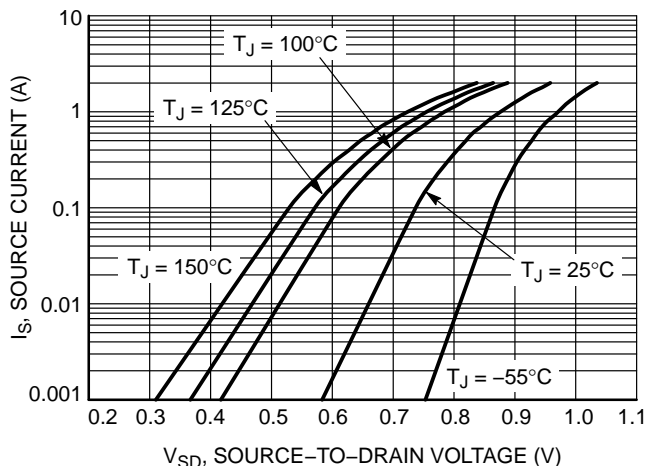


Figure 12. Diode Forward Voltage vs. Current

NDDL01N60Z, NDTL01N60Z

TYPICAL CHARACTERISTICS

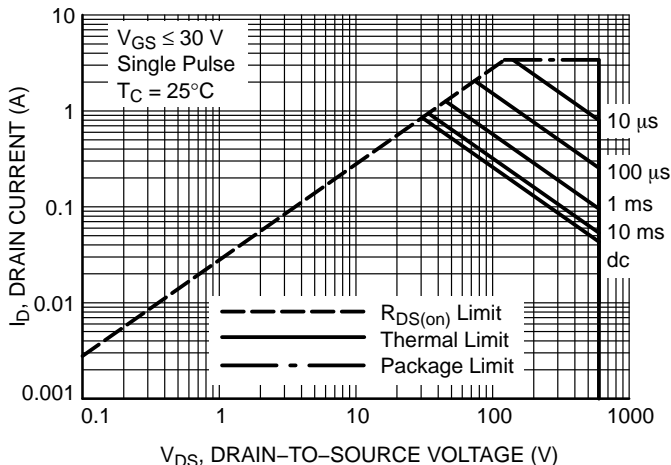


Figure 13. Maximum Rated Forward Biased Safe Operating Area for NDDL01N60Z

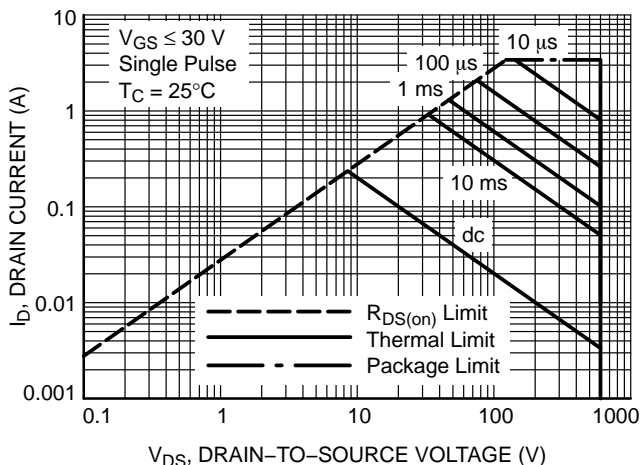


Figure 14. Maximum Rated Forward Biased Safe Operating Area for NDTL01N60Z

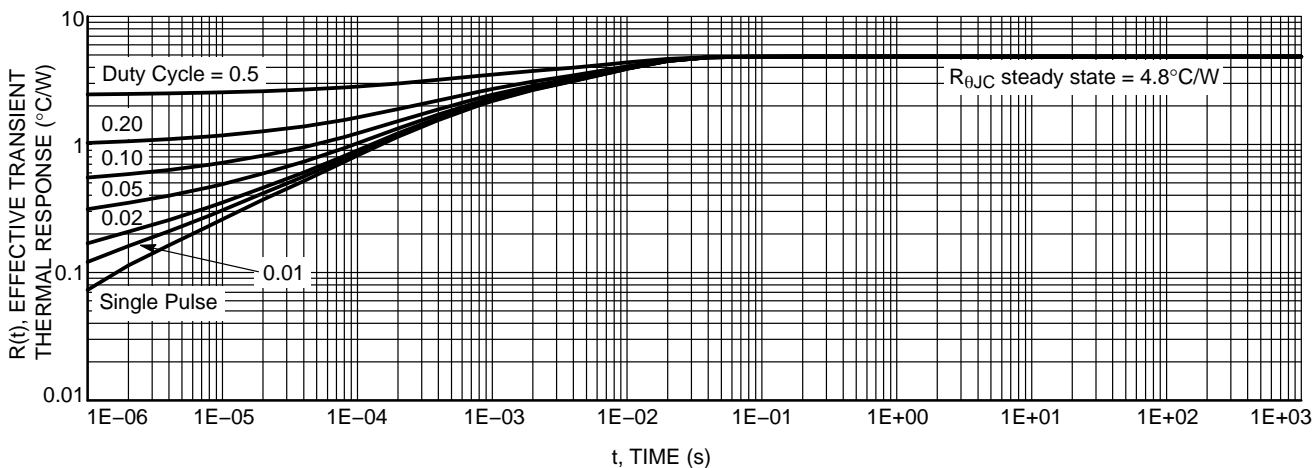


Figure 15. Thermal Impedance (Junction-to-Case) for NDDL01N60Z

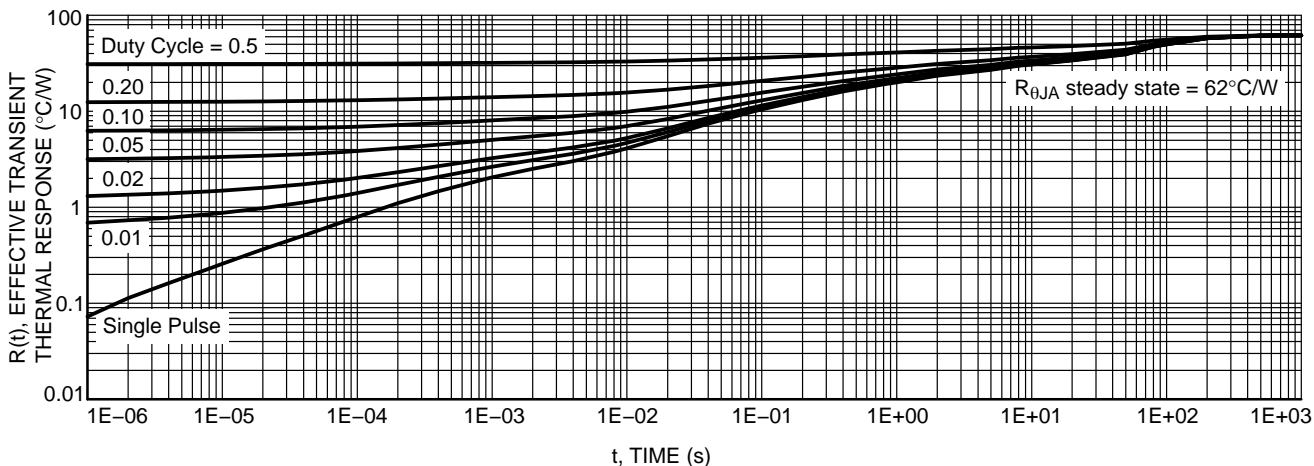


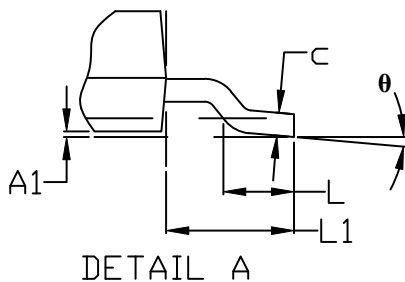
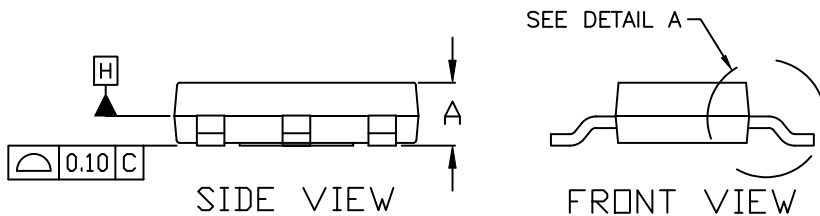
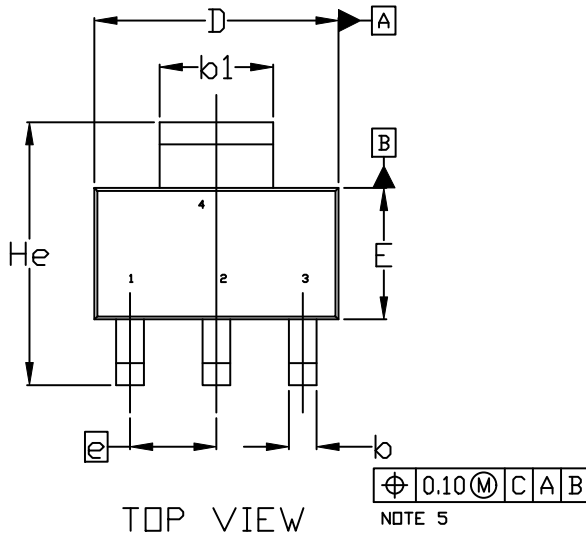
Figure 16. Thermal Impedance (Junction-to-Ambient) for NDTL01N60Z



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

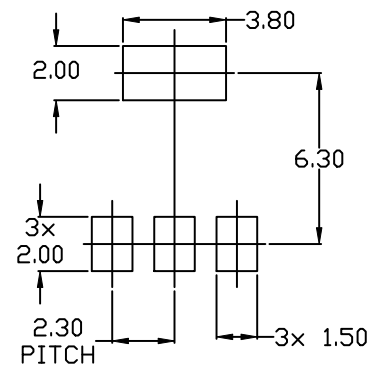
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

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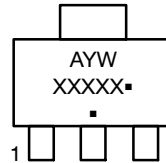
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|--|---|---|---|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***



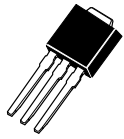
- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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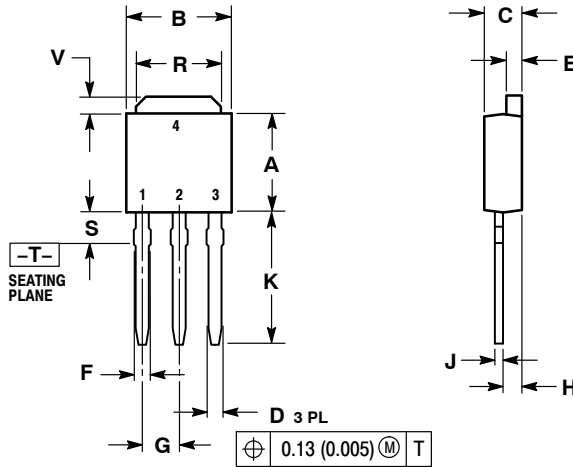
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DPAK INSERTION MOUNT
CASE 369
ISSUE O

DATE 02 JAN 2000

SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

- | | | | | | |
|---|--|--|---|---|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE | STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE | STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2 |
|---|--|--|---|---|---|

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DESCRIPTION:	DPAK INSERTION MOUNT	PAGE 1 OF 1

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