

# 12-Stage Binary Ripple Counter

## High-Performance Silicon-Gate CMOS

### MC74HC4040A

The MC74C4040A is identical in pinout to the standard CMOS MC14040. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half of that of the preceding one. The state counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the HC4040A for some designs.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With JEDEC Standard No. 7A Requirements
- Chip Complexity: 398 FETs or 99.5 Equivalent Gates
- -Q Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

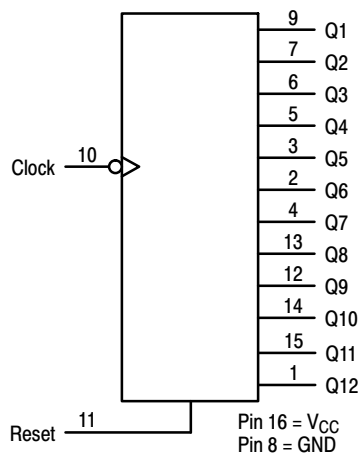
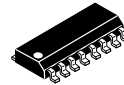
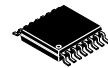


Figure 1. Logic Diagram

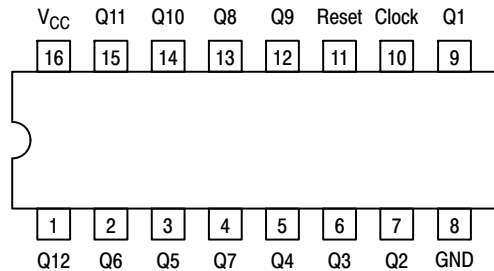


SOIC-16  
D SUFFIX  
CASE 751B



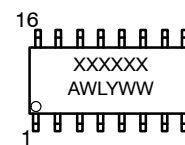
TSSOP-16  
DT SUFFIX  
CASE 948F

#### PIN ASSIGNMENT

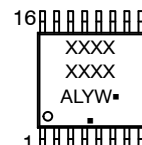


16-Lead Package (Top View)

#### MARKING DIAGRAMS



SOIC-16



TSSOP-16

A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

| Clock | Reset | Output State          |
|-------|-------|-----------------------|
|       | L     | No Charge             |
|       | L     | Advance to Next State |
| X     | H     | All Outputs Are Low   |

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8

# MC74HC4040A

## MAXIMUM RATINGS

| Symbol           | Parameter                                                                           | Value                        | Unit |
|------------------|-------------------------------------------------------------------------------------|------------------------------|------|
| V <sub>CC</sub>  | DC Supply Voltage                                                                   | −0.5 to +6.5                 | V    |
| V <sub>IN</sub>  | DC Input Voltage                                                                    | −0.5 to V <sub>CC</sub> +0.5 | V    |
| V <sub>OUT</sub> | DC Output Voltage                                                                   | −0.5 to V <sub>CC</sub> +0.5 | V    |
| I <sub>IN</sub>  | DC Input Diode Current, per Pin                                                     | ±20                          | mA   |
| I <sub>OUT</sub> | DC Input Diode Current, Per Pin                                                     | ±25                          | mA   |
| I <sub>CC</sub>  | DC Supply Current, V <sub>CC</sub> and GND Pins                                     | ±50                          | mA   |
| I <sub>IK</sub>  | Input Clamp Current (V <sub>IN</sub> < 0 or V <sub>IN</sub> > V <sub>CC</sub> )     | ±20                          | mA   |
| I <sub>OK</sub>  | Output Clamp Current (V <sub>OUT</sub> < 0 or V <sub>OUT</sub> > V <sub>CC</sub> )  | ±20                          | mA   |
| T <sub>STG</sub> | Storage Temperature Range                                                           | −65 to +150                  | °C   |
| T <sub>L</sub>   | Lead Temperature, 1 mm from Case for 10 secs                                        | 260                          | °C   |
| T <sub>J</sub>   | Junction Temperature Under Bias                                                     | +150                         | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Note 1) <div>SOIC-16<br/>TSSOP-16</div>                         | 126<br>159                   | °C/W |
| P <sub>D</sub>   | Power Dissipation in Still Air at 25 °C <div>SOIC-16<br/>TSSOP-16</div>             | 995<br>787                   | mW   |
| MSL              | Moisture Sensitivity                                                                | Level 1                      | –    |
| F <sub>R</sub>   | Flammability Rating <div>Oxygen Index: 28 to 34</div>                               | UL 94 V-0 @ 0.125 in         | –    |
| V <sub>ESD</sub> | ESD Withstand Voltage (Note 2) <div>Human Body Model<br/>Charged Device Model</div> | > 2000<br>N/A                | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter                         | Min                                                                                                      | Max                            | Unit |
|-------------------|-----------------------------------|----------------------------------------------------------------------------------------------------------|--------------------------------|------|
| $V_{CC}$          | DC Supply Voltage                 | 2.0                                                                                                      | 6.0                            | V    |
| $V_{IN}, V_{OUT}$ | DC Input, Output Voltage (Note 3) | 0                                                                                                        | $V_{CC}$                       | V    |
| $T_A$             | Operating Free-Air Temperature    | -55                                                                                                      | +125                           | °C   |
| $t_r, t_f$        | Input Rise or Fall Time           | $V_{CC} = 2.0\text{ V}$<br>$V_{CC} = 3.0\text{ V}$<br>$V_{CC} = 4.5\text{ V}$<br>$V_{CC} = 6.0\text{ V}$ | 0<br>1000<br>600<br>500<br>400 | ns   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

## DC CHARACTERISTICS

| Sym-<br>bol | Parameter                        | Condition                                                                                     | $V_{CC}$<br>V            | Guaranteed Limit             |                              |                              | Unit |
|-------------|----------------------------------|-----------------------------------------------------------------------------------------------|--------------------------|------------------------------|------------------------------|------------------------------|------|
|             |                                  |                                                                                               |                          | -55 to 25 °C                 | $\leq 85$ °C                 | $\leq 125$ °C                |      |
| $V_{IH}$    | Minimum High-Level Input Voltage | $V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$<br>$ I_{out}  \leq 20\text{ }\mu\text{A}$ | 2.0<br>3.0<br>4.5<br>6.0 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | 1.50<br>2.10<br>3.15<br>4.20 | V    |
| $V_{IL}$    | Maximum Low-Level Input Voltage  | $V_{out} = 0.1\text{ V}$ or $V_{CC} - 0.1\text{ V}$<br>$ I_{out}  \leq 20\text{ }\mu\text{A}$ | 2.0<br>3.0<br>4.5<br>6.0 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | 0.50<br>0.90<br>1.35<br>1.80 | V    |

# MC74HC4040A

## DC CHARACTERISTICS

| Sym-<br>bol     | Parameter                                      | Condition                                                                                                                                         | V <sub>CC</sub><br>V | Guaranteed Limit     |                      |                      | Unit |
|-----------------|------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|----------------------|----------------------|----------------------|------|
|                 |                                                |                                                                                                                                                   |                      | -55 to 25 °C         | ≤85 °C               | ≤125 °C              |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage              | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                               | 2.0<br>4.5<br>6.0    | 1.9<br>4.4<br>5.9    | 1.9<br>4.4<br>5.9    | 1.9<br>4.4<br>5.9    | V    |
|                 |                                                | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0<br>4.5<br>6.0    | 2.48<br>3.98<br>5.48 | 2.34<br>3.84<br>5.34 | 2.20<br>3.70<br>5.20 |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA                                                               | 2.0<br>4.5<br>6.0    | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1    | V    |
|                 |                                                | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4mA<br> I <sub>out</sub>   ≤ 4.0mA<br> I <sub>out</sub>   ≤ 5.2mA | 3.0<br>4.5<br>6.0    | 0.26<br>0.26<br>0.26 | 0.33<br>0.33<br>0.33 | 0.40<br>0.40<br>0.40 |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND                                                                                                          | 6.0                  | ±0.1                 | ±1.0                 | ±1.0                 | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA                                                                               | 6.0                  | 4                    | 40                   | 160                  | μA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## AC CHARACTERISTICS

| Symbol                                 | Parameter                                                                          | V <sub>CC</sub><br>V     | Guaranteed Limit     |                       |                       | Unit |
|----------------------------------------|------------------------------------------------------------------------------------|--------------------------|----------------------|-----------------------|-----------------------|------|
|                                        |                                                                                    |                          | -55 to 25 °C         | ≤85 °C                | ≤125 °C               |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 2 and 3)                      | 2.0<br>3.0<br>4.5<br>6.0 | 10<br>15<br>30<br>50 | 9.0<br>14<br>28<br>45 | 8.0<br>12<br>25<br>40 | MHz  |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Clock to Q1*<br>(Figures 2 and 3)                       | 2.0<br>3.0<br>4.5<br>6.0 | 96<br>63<br>31<br>25 | 106<br>71<br>36<br>30 | 115<br>88<br>40<br>35 | ns   |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to Any Q<br>(Figures 2 and 4)                     | 2.0<br>3.0<br>4.5<br>6.0 | 65<br>30<br>30<br>26 | 72<br>36<br>35<br>32  | 90<br>40<br>40<br>35  | ns   |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Q <sub>n</sub> to Q <sub>n+1</sub><br>(Figures 2 and 5) | 2.0<br>3.0<br>4.5<br>6.0 | 69<br>40<br>17<br>14 | 80<br>45<br>21<br>15  | 90<br>50<br>28<br>22  | ns   |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 2 and 3)                    | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>27<br>15<br>13 | 95<br>32<br>19<br>15  | 110<br>36<br>22<br>19 | ns   |
| C <sub>in</sub>                        | Maximum Input Capacitance                                                          |                          | 10                   | 10                    | 10                    | pF   |

\*For T<sub>A</sub> = 25°C and C<sub>L</sub> = 50 pF, typical propagation delay from Clock to other Q outputs may be calculated with the following equations:

V<sub>CC</sub> = 2.0 V: t<sub>p</sub> = [93.7 + 59.3 (n-1)] ns V<sub>CC</sub> = 4.5 V: t<sub>p</sub> = [30.25 + 14.6 (n-1)] ns

V<sub>CC</sub> = 3.0 V: t<sub>p</sub> = [61.5 + 34.4 (n-1)] ns V<sub>CC</sub> = 6.0V: t<sub>p</sub> = [24.4 + 12 (n-1)] ns

|                 |                                              |                                          |    |
|-----------------|----------------------------------------------|------------------------------------------|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Package)* | Typical @ 25 °C, V <sub>CC</sub> = 5.0 V | pF |
|                 |                                              | 31                                       |    |

\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

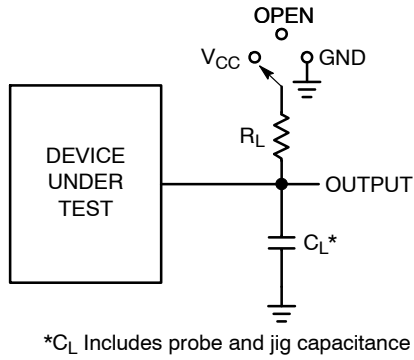
# MC74HC4040A

## TIMING REQUIREMENTS

| Sym-<br>bol                     | Parameter                                                    | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|---------------------------------|--------------------------------------------------------------|----------------------|------------------|--------|---------|------|
|                                 |                                                              |                      | -55 to 25 °C     | ≤85 °C | ≤125 °C |      |
| t <sub>rec</sub>                | Minimum Recovery Time, Reset Inactive to Clock<br>(Figure 4) | 2.0                  | 30               | 40     | 50      | ns   |
|                                 |                                                              | 3.0                  | 20               | 25     | 30      |      |
|                                 |                                                              | 4.5                  | 5                | 8      | 12      |      |
|                                 |                                                              | 6.0                  | 4                | 6      | 9       |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Clock<br>(Figure 3)                     | 2.0                  | 70               | 80     | 90      | ns   |
|                                 |                                                              | 3.0                  | 40               | 45     | 50      |      |
|                                 |                                                              | 4.5                  | 15               | 19     | 24      |      |
|                                 |                                                              | 6.0                  | 13               | 16     | 20      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 4)                     | 2.0                  | 70               | 80     | 90      | ns   |
|                                 |                                                              | 3.0                  | 40               | 45     | 50      |      |
|                                 |                                                              | 4.5                  | 15               | 19     | 24      |      |
|                                 |                                                              | 6.0                  | 13               | 16     | 20      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 3)              | 2.0                  | 1000             | 1000   | 1000    | ns   |
|                                 |                                                              | 3.0                  | 800              | 800    | 800     |      |
|                                 |                                                              | 4.5                  | 500              | 500    | 500     |      |
|                                 |                                                              | 6.0                  | 400              | 400    | 400     |      |

# MC74HC4040A

## SWITCHING WAVEFORMS



| Test                                | Switch Position | C <sub>L</sub> | R <sub>L</sub> |
|-------------------------------------|-----------------|----------------|----------------|
| t <sub>PLH</sub> / t <sub>PHL</sub> | Open            | 50 pF          | 1 kΩ           |
| t <sub>PLZ</sub> / t <sub>PZL</sub> | V <sub>CC</sub> |                |                |
| t <sub>PHZ</sub> / t <sub>PZH</sub> | GND             |                |                |

Figure 2. Test Circuit

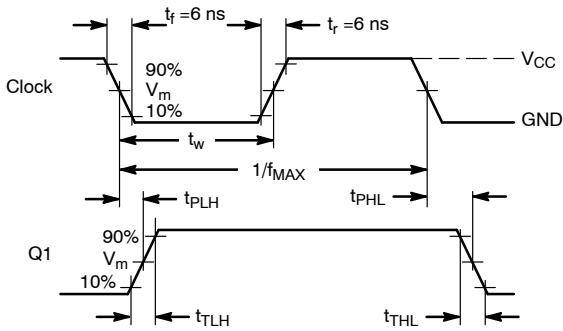


Figure 3.

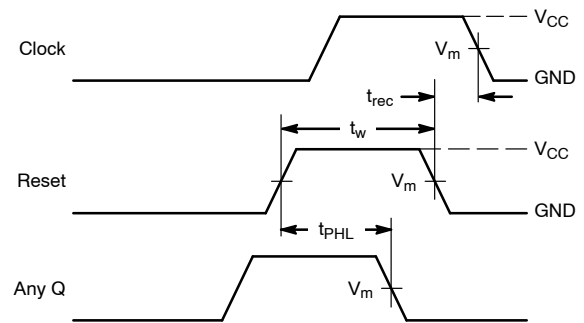


Figure 4.

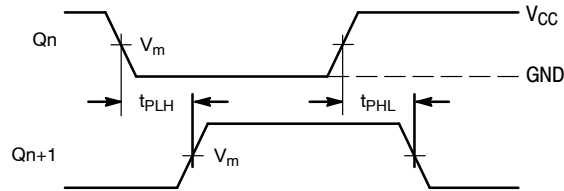


Figure 5.

| Device      | V <sub>IN</sub> , V | V <sub>m</sub> , V    |
|-------------|---------------------|-----------------------|
| MC74HC4040A | V <sub>CC</sub>     | 50% x V <sub>CC</sub> |

# MC74HC4040A

## PIN DESCRIPTIONS

### INPUTS

#### Clock (Pin 10)

Negative-edge triggering clock input. A high-to-low transition on this input advances the state of the counter.

#### Reset (Pin 11)

Active-high reset. A high level applied to this input asynchronously resets the counter to its zero state, thus forcing all Q outputs low.

### OUTPUTS

#### Q1 thru Q12 (Pins 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1)

Active-high outputs. Each Qn output divides the Clock input frequency by  $2^N$ .

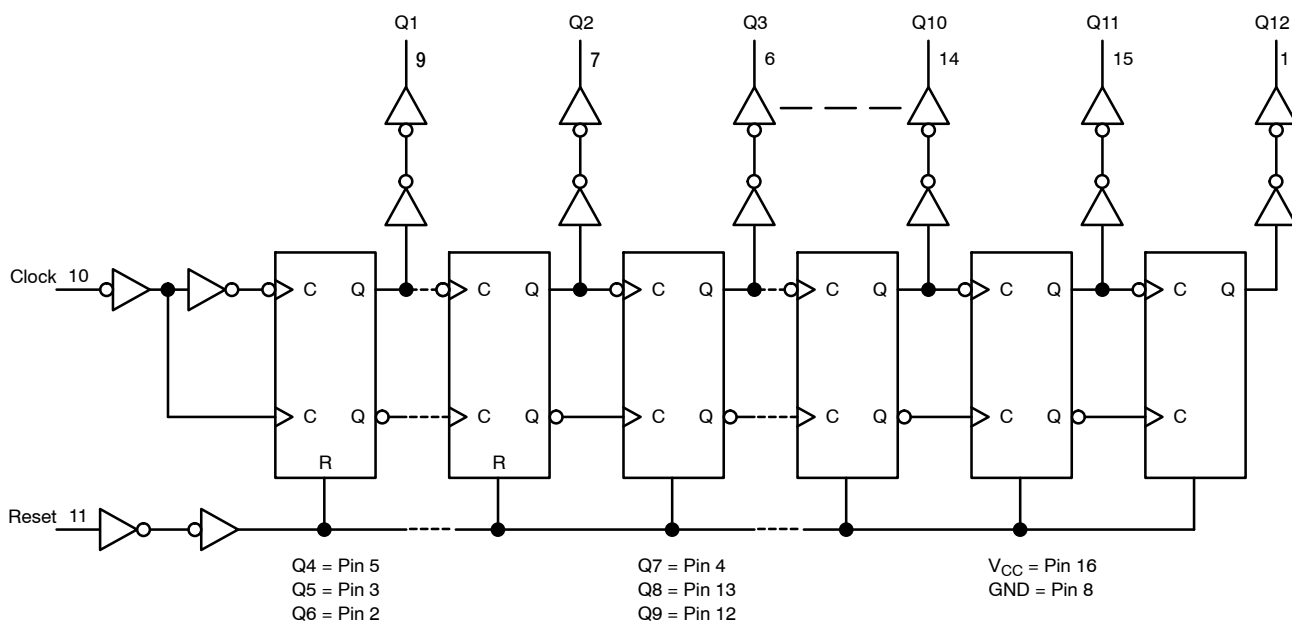


Figure 6. Expanded Logic Diagram

# MC74HC4040A

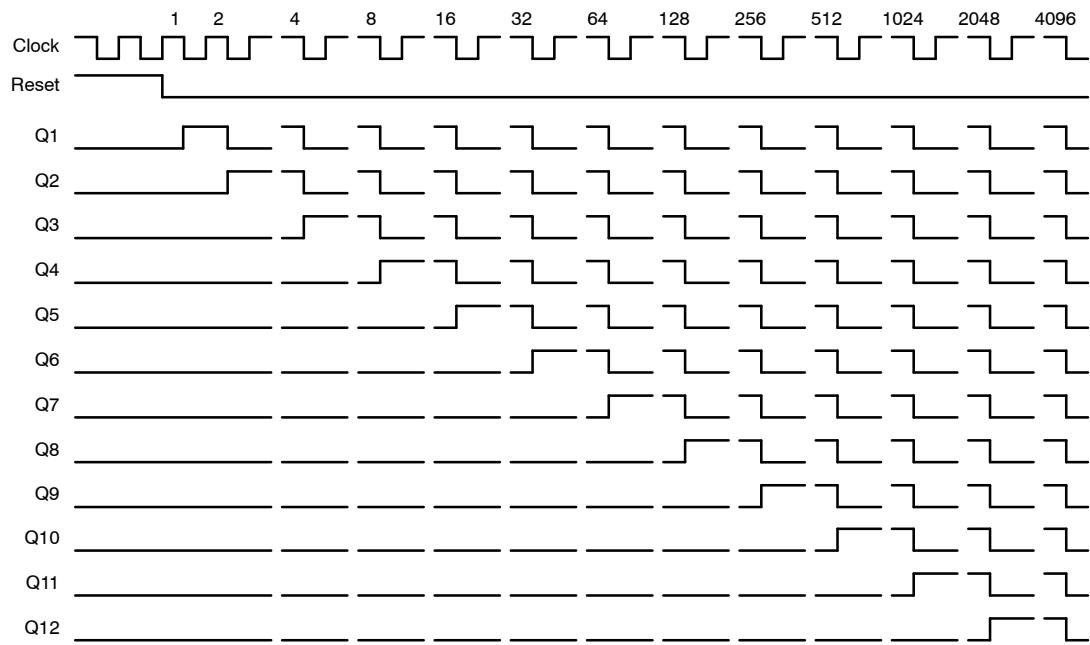


Figure 7. Timing Diagram

# MC74HC4040A

## APPLICATIONS INFORMATION

### Time-Base Generator

A 60 Hz sinewave obtained through a 100k resistor connected to a 120 Vac power line through a step down transformer is applied to the input of the MC54/74HC14A, Schmitt-trigger inverter. The HC14A squares-up the input

waveform and feeds the HC4040A. Selecting outputs Q5, Q10, Q11, and Q12 causes a reset every 3600 clocks. The HC20 decodes the counter outputs, produces a single (narrow) output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.

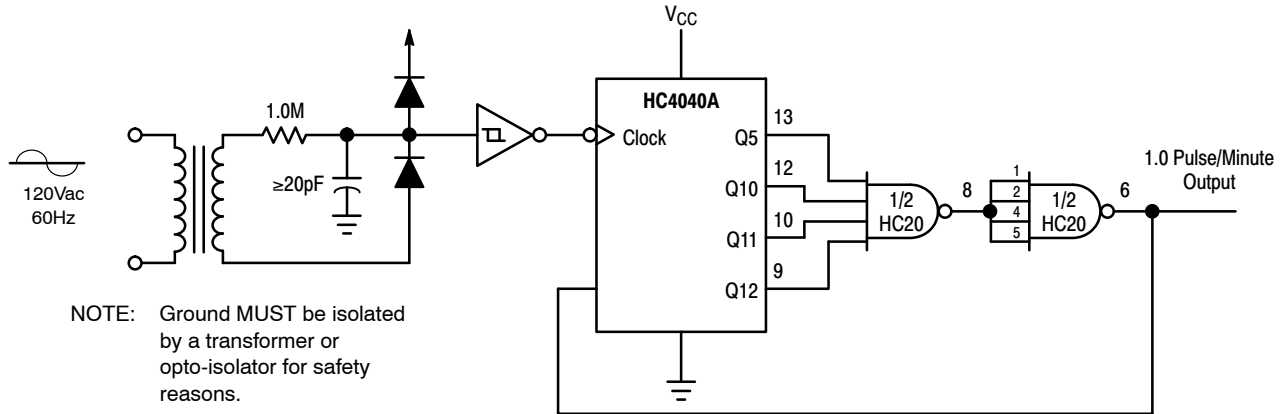


Figure 8. Time-Base Generator

### ORDERING INFORMATION

| Device           | Marking  | Package               | Shipping <sup>†</sup> |
|------------------|----------|-----------------------|-----------------------|
| MC74HC4040ADR2G  | HC4040AG | SOIC-16<br>(Pb-Free)  | 2500 Units / Reel     |
| MC74HC4040ADTR2G | HC4040A  | TSSOP-16<br>(Pb-Free) | 2500 Units / Reel     |

### DISCONTINUED (Note 4)

|                   |  |                      |                   |
|-------------------|--|----------------------|-------------------|
| MC74HC4040ADG     |  | SOIC-16<br>(Pb-Free) | 48 Units / Rail   |
| NLV74HC4040ADR2G* |  | SOIC-16<br>(Pb-Free) | 2500 Units / Reel |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

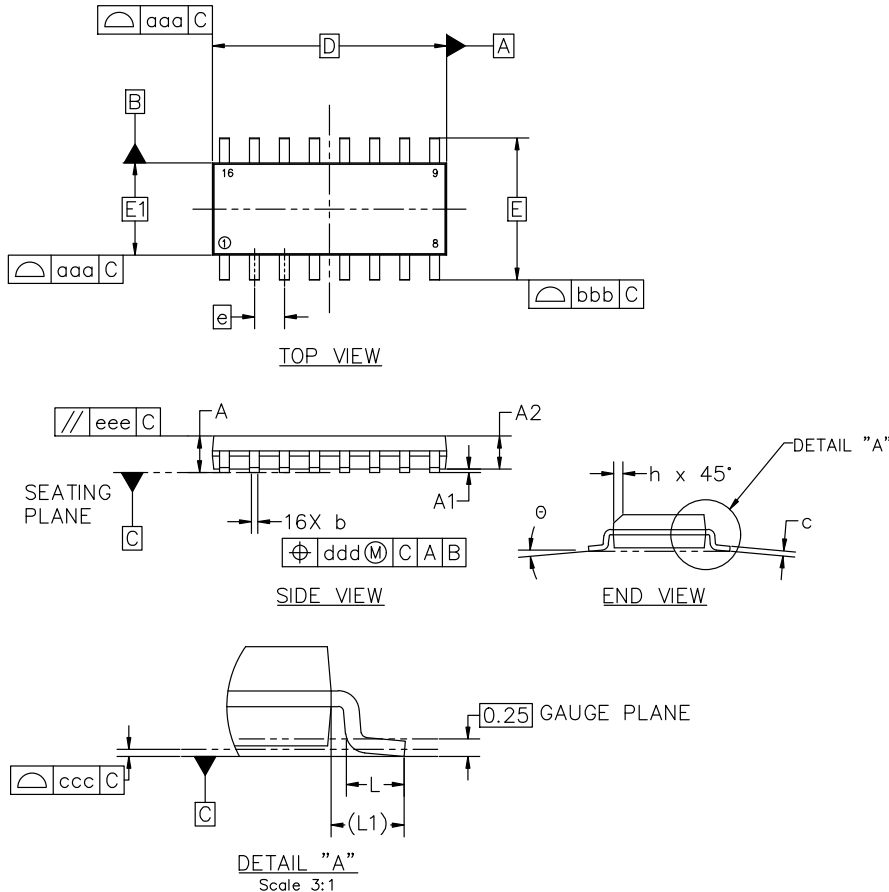
4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](#).


**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

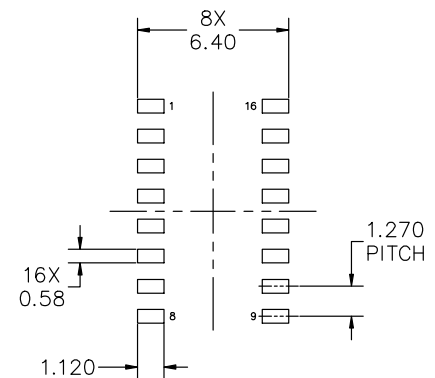
DATE 18 OCT 2024

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



| MILLIMETERS                    |          |      |      |
|--------------------------------|----------|------|------|
| DIM                            | MIN      | NOM  | MAX  |
| A                              | 1.35     | 1.55 | 1.75 |
| A1                             | 0.10     | 0.18 | 0.25 |
| A2                             | 1.25     | 1.37 | 1.50 |
| b                              | 0.35     | 0.42 | 0.49 |
| c                              | 0.19     | 0.22 | 0.25 |
| D                              | 9.90 BSC |      |      |
| E                              | 6.00 BSC |      |      |
| E1                             | 3.90 BSC |      |      |
| e                              | 1.27 BSC |      |      |
| h                              | 0.25     | ---  | 0.50 |
| L                              | 0.40     | 0.83 | 1.25 |
| L1                             | 1.05 REF |      |      |
| θ                              | 0°       | ---  | 7°   |
| TOLERANCE OF FORM AND POSITION |          |      |      |
| aaa                            | 0.10     |      |      |
| bbb                            | 0.20     |      |      |
| ccc                            | 0.10     |      |      |
| ddd                            | 0.25     |      |      |
| eee                            | 0.10     |      |      |



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

|                         |                                     |                                                                                                                                                                                  |
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SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
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DATE 18 OCT 2024

GENERIC  
MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>STYLE 1:</b><br>PIN 1. COLLECTOR<br>2. BASE<br>3. EMITTER<br>4. NO CONNECTION<br>5. EMITTER<br>6. BASE<br>7. COLLECTOR<br>8. COLLECTOR<br>9. BASE<br>10. EMITTER<br>11. NO CONNECTION<br>12. EMITTER<br>13. BASE<br>14. COLLECTOR<br>15. EMITTER<br>16. COLLECTOR                           | <b>STYLE 2:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION<br>4. CATHODE<br>5. CATHODE<br>6. NO CONNECTION<br>7. ANODE<br>8. CATHODE<br>9. CATHODE<br>10. ANODE<br>11. NO CONNECTION<br>12. CATHODE<br>13. CATHODE<br>14. NO CONNECTION<br>15. ANODE<br>16. CATHODE | <b>STYLE 3:</b><br>PIN 1. COLLECTOR, DYE #1<br>2. BASE, #1<br>3. EMITTER, #1<br>4. COLLECTOR, #1<br>5. COLLECTOR, #2<br>6. BASE, #2<br>7. EMITTER, #2<br>8. COLLECTOR, #2<br>9. COLLECTOR, #3<br>10. BASE, #3<br>11. EMITTER, #3<br>12. COLLECTOR, #3<br>13. COLLECTOR, #4<br>14. BASE, #4<br>15. EMITTER, #4<br>16. COLLECTOR, #4                                                                                         | <b>STYLE 4:</b><br>PIN 1. COLLECTOR, DYE #1<br>2. COLLECTOR, #1<br>3. COLLECTOR, #2<br>4. COLLECTOR, #2<br>5. COLLECTOR, #3<br>6. COLLECTOR, #3<br>7. COLLECTOR, #4<br>8. COLLECTOR, #4<br>9. BASE, #4<br>10. EMITTER, #4<br>11. BASE, #3<br>12. EMITTER, #3<br>13. BASE, #2<br>14. EMITTER, #2<br>15. BASE, #1<br>16. EMITTER, #1 |
| <b>STYLE 5:</b><br>PIN 1. DRAIN, DYE #1<br>2. DRAIN, #1<br>3. DRAIN, #2<br>4. DRAIN, #2<br>5. DRAIN, #3<br>6. DRAIN, #3<br>7. DRAIN, #4<br>8. DRAIN, #4<br>9. GATE, #4<br>10. SOURCE, #4<br>11. GATE, #3<br>12. SOURCE, #3<br>13. GATE, #2<br>14. SOURCE, #2<br>15. GATE, #1<br>16. SOURCE, #1 | <b>STYLE 6:</b><br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE<br>4. CATHODE<br>5. CATHODE<br>6. CATHODE<br>7. CATHODE<br>8. CATHODE<br>9. ANODE<br>10. ANODE<br>11. ANODE<br>12. ANODE<br>13. ANODE<br>14. ANODE<br>15. ANODE<br>16. ANODE                                 | <b>STYLE 7:</b><br>PIN 1. SOURCE N-CH<br>2. COMMON DRAIN (OUTPUT)<br>3. COMMON DRAIN (OUTPUT)<br>4. GATE P-CH<br>5. COMMON DRAIN (OUTPUT)<br>6. COMMON DRAIN (OUTPUT)<br>7. COMMON DRAIN (OUTPUT)<br>8. SOURCE P-CH<br>9. SOURCE P-CH<br>10. COMMON DRAIN (OUTPUT)<br>11. COMMON DRAIN (OUTPUT)<br>12. COMMON DRAIN (OUTPUT)<br>13. GATE N-CH<br>14. COMMON DRAIN (OUTPUT)<br>15. COMMON DRAIN (OUTPUT)<br>16. SOURCE N-CH |                                                                                                                                                                                                                                                                                                                                    |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                     |                                                                                                                                                                                     |
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**TSSOP-16 WB**  
**CASE 948F**  
**ISSUE B**

DATE 19 OCT 2006

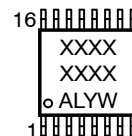

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

**RECOMMENDED  
SOLDERING FOOTPRINT\***


\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

|                         |                    |                                                                                                                                                                                  |
|-------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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