

4.5-V TO 28-V INPUT VOLTAGE, 3.3-V FIXED OUTPUT, 1.7-A OUTPUT CURRENT, NON-SYNCHRONOUS STEP-DOWN REGULATOR WITH INTEGRATED MOSFET

Check for Samples: [TPS5403](#)

FEATURES

- Fixed 3.3-V Output
- 4.5-V to 28-V Wide Input Voltage Range
- Up to 1.7-A Maximum Continuous Output Loading Current
- Pulse Skipping Mode to Achieve High Light Load Efficiency
- Over 80% Efficiency at 10-mA Loading
- Adjustable 50-kHz to 1.1-MHz Switching Frequency Set by an External Resistor (Leave pin ROSC floating. Set frequency to 120 kHz and ground connection to 70 kHz)
- Peak Current-Mode Control
- Cycle-by-Cycle Over Current Protection
- Frequency Spread Spectrum and Switching Node Anti-Ringing to Ease EMI Issue
- External Soft Start
- Available in SOIC8 Package

APPLICATIONS

- 5-V, 9-V, 12-V and 24-V Distributed Power Systems
- Consumer Applications Such as Home Appliances, Set-Top Boxes, CPE Equipment, LCD Displays, Peripherals, and Battery Chargers
- Industrial and Car Entertainment Power Supplies

DESCRIPTION

The TPS5403 is a monolithic non-synchronous buck regulator with wide operating input voltage range from 4.5 V to 28 V. Current mode control with internal slope compensation is implemented to reduce component count.

TPS5403 also features a light load pulse skipping mode, which allows for a power loss reduction from the input power supply to the system at light loading.

The switching frequency of the converters can be set from 50 kHz to 1.1 MHz with an external resistor. Frequency spread spectrum operation is introduced for EMI reduction.

LX anti-ringing is added to address high frequency EMI issues.

A cycle-by-cycle current limit with frequency fold back protects the IC at over loading condition.



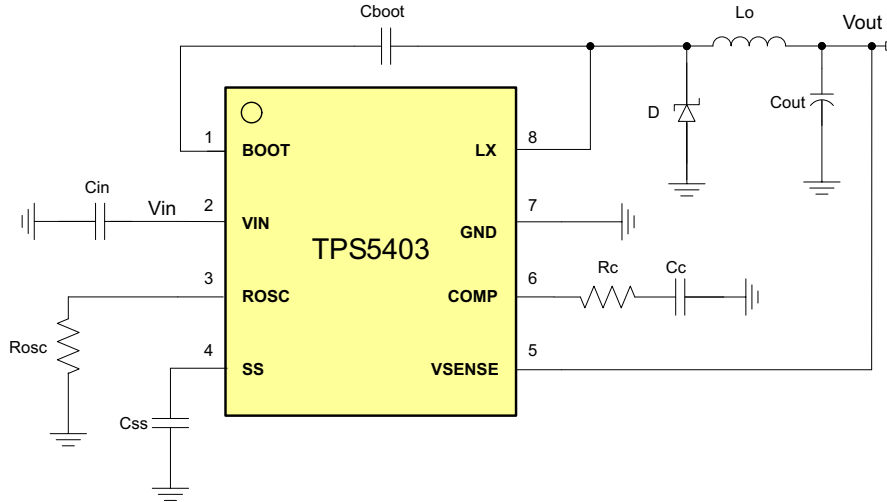
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



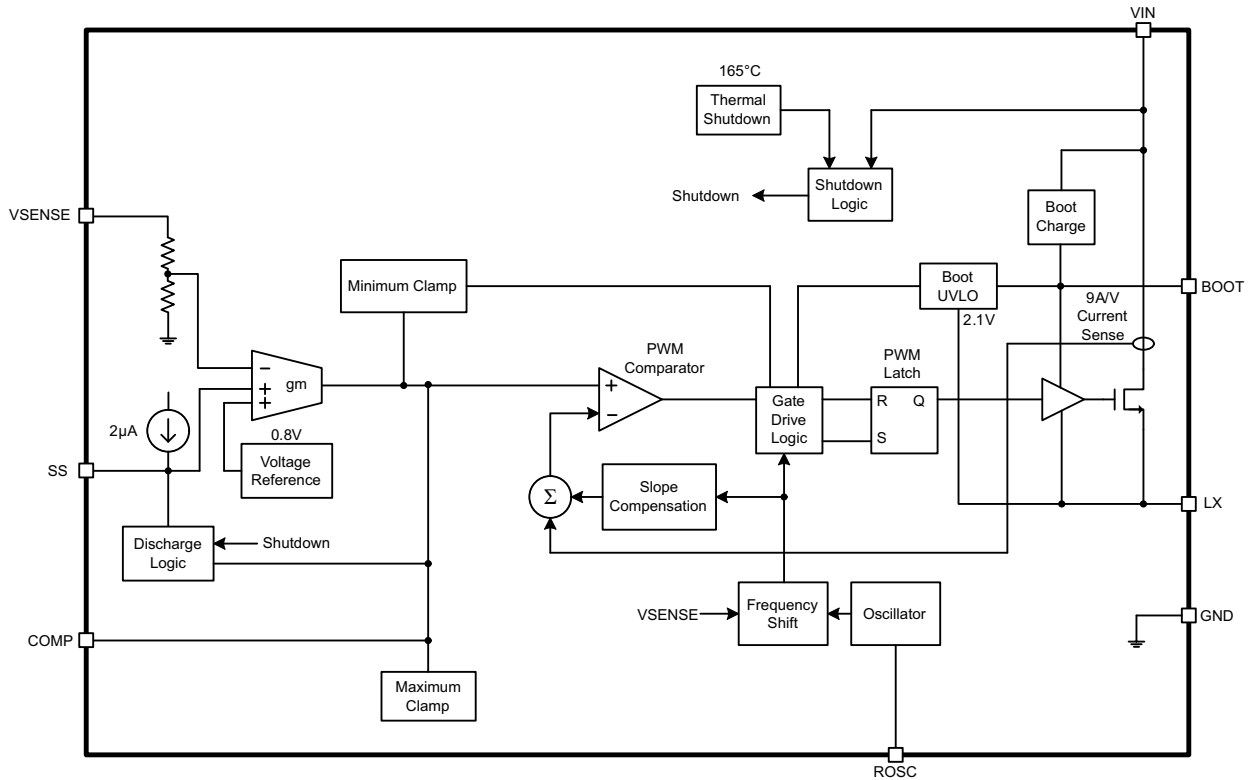
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

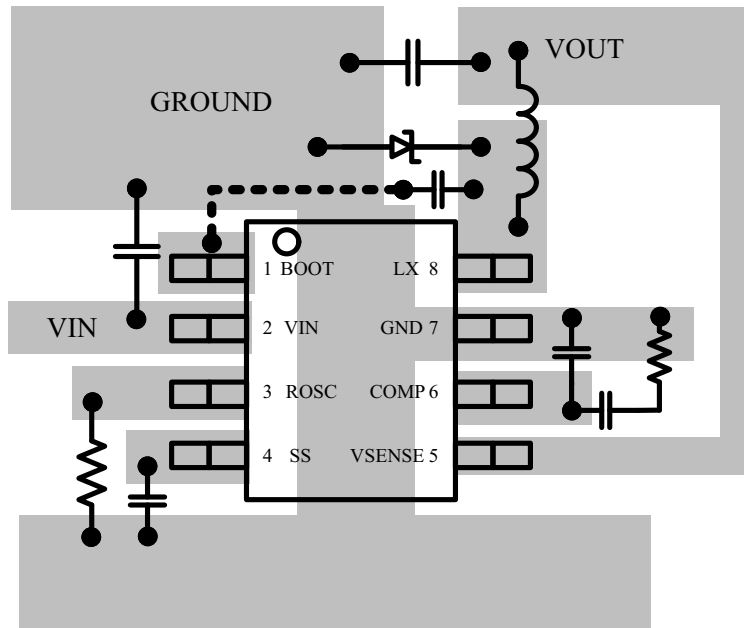
TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



PCB LAYOUT

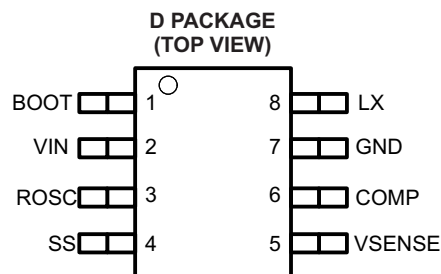


ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|-----------------------|------------------|
| -40°C to 85°C | 8-pin SOIC (D) | TPS5403DR | TPS5403 |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN OUT



TERMINAL FUNCTIONS

| NAME | NO. | DESCRIPTION |
|--------|-----|---|
| BOOT | 1 | A 0.1-μF bootstrap capacitor is required between BOOT and LX. |
| VIN | 2 | Input supply voltage, 4.5 V to 28 V |
| ROSC | 3 | Switching frequency program pin. Connect a resistor to this pin to set the switching frequency. Connect the pin to ground for a default 70-kHz switching frequency. Leave the pin open for 120-kHz switching frequency. |
| SS | 4 | Soft start pin. An external capacitor connected to this pin sets the output rise time. |
| VSENSE | 5 | Output voltage feedback pin |
| COMP | 6 | Error amplifier output and input to the PWM comparator. Connect frequency compensation components to this pin. |
| GND | 7 | Ground |
| LX | 8 | Switching node to external inductor |

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | |
|------------------|---|-------------|----|
| | Voltage range at VIN, LX | –0.3 to 30 | V |
| | Voltage range at LX (maximum withstand voltage transient < 20 ns) | –5 to 30 | V |
| | Voltage from BOOT to LX | –0.3 to 7 | V |
| | Voltage at VSENSE | –0.3 to 7 | V |
| | Voltage at SS | –0.3 to 3 | V |
| | Voltage at ROSC | –0.3 to 3 | V |
| | Voltage at COMP | –0.3 to 3 | V |
| | Voltage at GND | –0.3 to 0.3 | V |
| T _J | Operating junction temperature range | –40 to 125 | °C |
| T _{STG} | Storage temperature range | –55 to 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------|-------------------------|-----|-----|-----|------|
| VIN | Input operating voltage | 4.5 | | 28 | V |
| T _A | Ambient temperature | –40 | | 85 | °C |

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | TPS5403 | UNITS |
|-------------------------------|---|---------|-------|
| | | D | |
| | | 8 PINS | |
| θ _{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 116.7 | °C/W |
| θ _{JCtop} | Junction-to-case (top) thermal resistance ⁽³⁾ | 62.4 | |
| θ _{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 57.0 | |
| ψ _{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 14.5 | |
| ψ _{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 56.5 | |
| θ _{JCbot} | Junction-to-case (bottom) thermal resistance ⁽⁷⁾ | N/A | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS
 $T_A = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 4.5\text{ V}$ to 28 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|---|--|-----|---------|------|--------------------|
| INPUT SUPPLY | | | | | | |
| V_{IN} | Input Voltage range | | 4.5 | | 28 | V |
| I_{DDQ_nsw} | Non switching quiescent power supply current | $V_{SENSE} > 3.5\text{ V}$ | | 100 | | μA |
| $UVLO$ | V_{IN} under voltage lockout | Rising V_{IN} | | 3.5 | | V |
| | | Hysteresis | | 200 | | mV |
| FEEDBACK AND ERROR AMPLIFIER | | | | | | |
| V_{SENSE} | Regulated output voltage | $V_{IN} = 12\text{ V}$ | 3.2 | 3.3 | 3.4 | V |
| G_{m_EA} | Error amplifier trans-conductance | $-2\ \mu\text{A} < I_{COMP} < 2\ \mu\text{A}$, $V_{COMP} = 1\text{ V}$ | | 92 | | μs |
| I_{gm} | Error amplifier source/sink current | $V_{COMP} = 1\text{ V}$, 100 mV overdrive | | ± 7 | | μA |
| G_{m_SRC} | COMP voltage to inductor current G_m | $V_{IN} = 12\text{ V}$ | | 9 | | A/V |
| PFM MODE AND SOFT-START | | | | | | |
| I_{th} | Pulse skipping mode switch current threshold | | | 300 | | mA |
| I_{SS} | Charge current | | | 2 | | μA |
| OSCILLATOR | | | | | | |
| f_{SW_BK} | Switching frequency range | Set by external resistor ROSC | 50 | | 1100 | kHz |
| f_{SW} | Programmable frequency | ROSC = GND | | 70 | | kHz |
| | | ROSC = OPEN | | 120 | | |
| | | ROSC = 85.5 k Ω | | 300 | | |
| f_{jitter} | Frequency spread spectrum in percentage of f_{SW} | $V_{IN} = 12\text{ V}$ | | ± 6 | | % |
| f_{swing} | Jittering swing frequency in percentage of f_{SW} | $V_{IN} = 12\text{ V}$ | | 1/512 | | |
| t_{min_on} | Minimum on time | $V_{IN} = 12\text{ V}$, $T_A = 25^{\circ}\text{C}$ | | 200 | | ns |
| D_{max} | Maximum duty ratio | $V_{IN} = 12\text{ V}$ | | 93 | | % |
| CURRENT LIMIT | | | | | | |
| I_{LIMIT} | Peak inductor current limit | $V_{IN} = 12\text{ V}$ | 2.2 | 2.5 | 3.1 | A |
| MOSFET ON-RESISTANCE | | | | | | |
| R_{dson_HS} | On resistance of high side FET | $V_{IN} = 12\text{ V}$ | | 120 | 240 | m Ω |
| THERMAL SHUTDOWN | | | | | | |
| T_{TRIP} | Thermal protection trip point | Rising temperature | | 165 | | $^{\circ}\text{C}$ |

TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{ V}$, $f_{SW} = 120\text{ kHz}$ (unless otherwise noted)

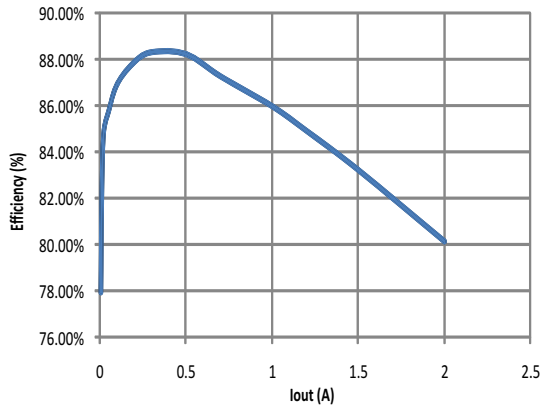


Figure 1. Efficiency
 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$

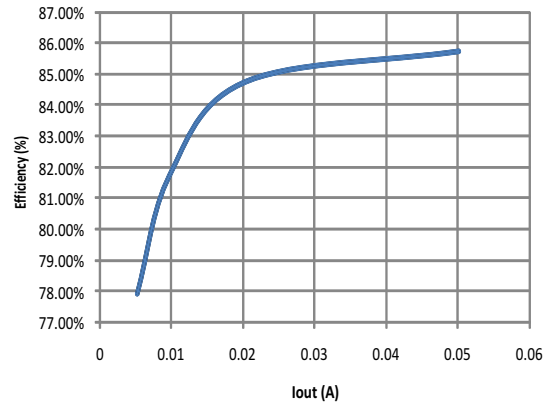


Figure 2. Efficiency
 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$

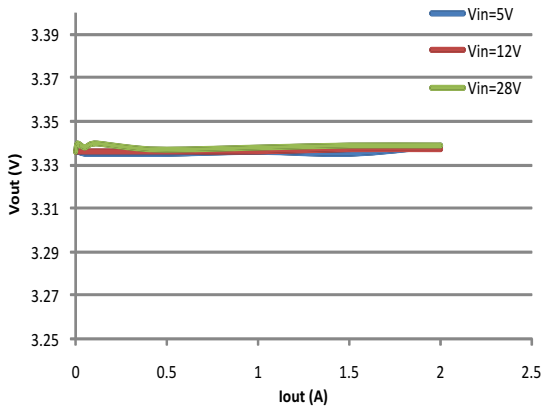


Figure 3. Load Regulation
 $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$

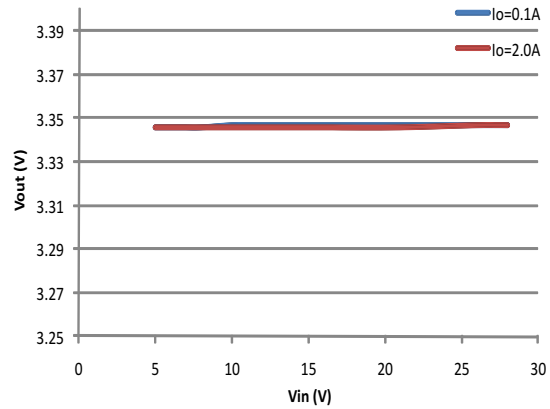


Figure 4. Line Regulation
 $V_{OUT} = 3.3\text{ V}$

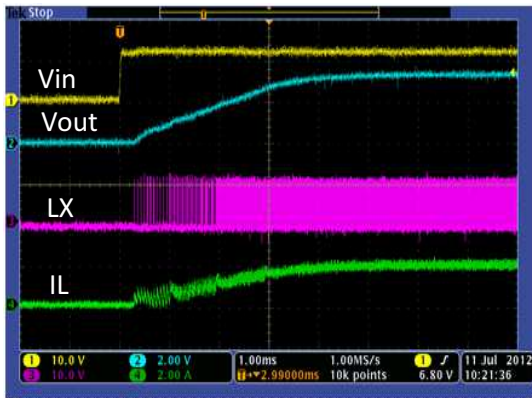


Figure 5. Startup
2-A Preset Loading

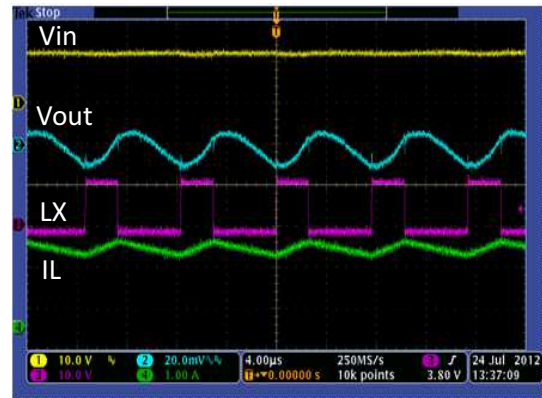


Figure 6. Steady State
 $I_O = 2\text{ A}$

TYPICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{ V}$, $f_{SW} = 120\text{ kHz}$ (unless otherwise noted)

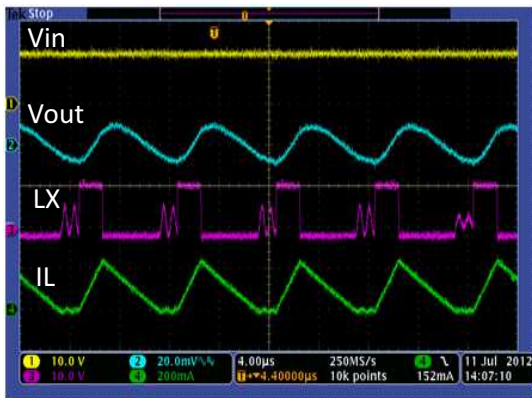


Figure 7. Steady State
 $I_O = 100\text{ mA}$

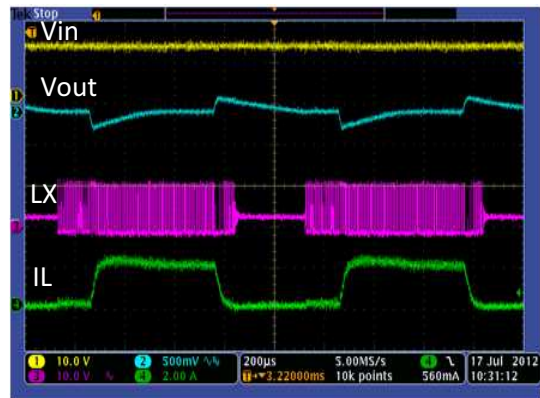


Figure 8. Load Transient
 $I_O = 0.1\text{ A to }1\text{ A}$

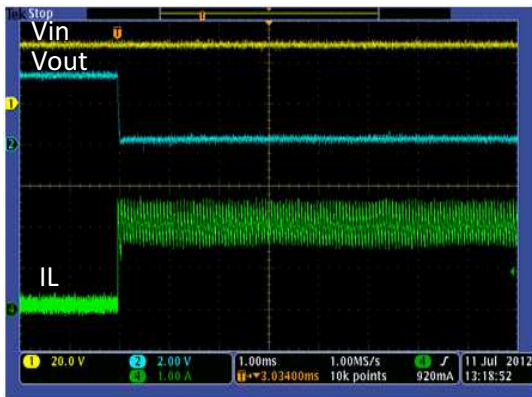


Figure 9. Short Circuit Protection

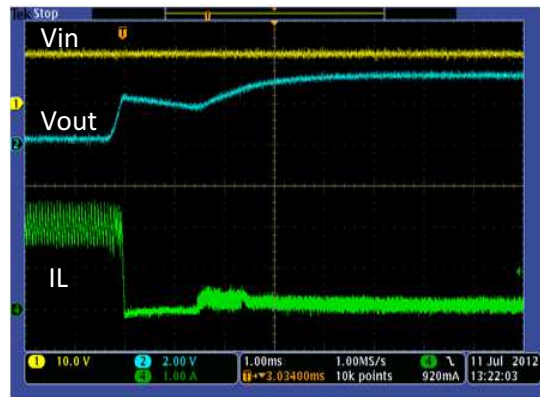


Figure 10. Short Circuit Recovery

OVERVIEW

The TPS5403 is a 28-V, 1.7-A, step-down (buck) converter with an integrated high-side N-channel MOSFET. To improve performance during line and load transients, the device implements a constant frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design.

The TPS5403's switching frequency is adjustable with an external resistor or fixed by connecting the frequency program pin to GND or leaving it unconnected.

The TPS5403 starts switching at V_{IN} equal to 3.5 V. The operating current is 100 μ A typically when not switching and under no load. When the device is disabled, the supply current is 1 μ A typically.

The integrated 120-m Ω high-side MOSFET allows for high efficiency power supply designs with continuous output currents up to 1.7 A.

The TPS5403 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by an external capacitor on the BOOT to PH pins. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high-side MOSFET off when the voltage falls below a preset threshold of 2.1 V typically.

By adding an external capacitor, the slow start time of the TPS5403 can be adjustable which enables flexible output filter selection. To improve the efficiency at light load conditions, the TPS5403 enters a special pulse skipping mode when the peak inductor current drops below 300 mA typically. The frequency foldback reduces the switching frequency during startup and over current conditions to help control the inductor current. The thermal shut down gives the additional protection under fault conditions.

DETAILED DESCRIPTION

Adjustable Frequency PWM Control

The TPS5403 uses an external resistor to adjust the switching frequency. Connecting the ROsc pin to ground fixes the switching frequency at 70 kHz, leaving it open gives 120-kHz switching frequency.

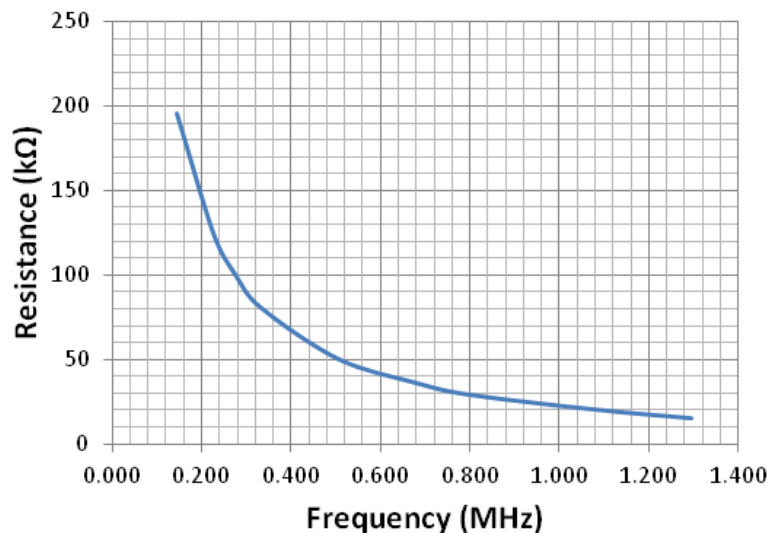


Figure 11. ROsc vs Switching Frequency

$$R_{OSC}(k\Omega) = 21.82 \cdot f_{SW}^{-1.167} \quad (1)$$

For operation at 300 kHz, an 85.5-k Ω resistor is required.

Pulse Skipping Mode

The TPS5403 is designed to operate in pulse skipping mode at light load currents to boost light load efficiency. When the peak inductor current is lower than 300 mA typically, the COMP pin voltage falls to 0.5 V typically and the device enters pulse skipping mode. When the device is in pulse skipping mode, the COMP pin voltage is clamped at 0.5 V internally which prevents the high side integrated MOSFET from switching. The peak inductor current must rise above 300 mA for the COMP pin voltage to rise above 0.5 V and exit pulse skipping mode. Since the integrated current comparator catches the peak inductor current only, the average load current entering pulse skipping mode varies with the applications and external output filters.

Voltage Reference (V_{SENSE})

The voltage reference system produces a $\pm 3\%$ accuracy voltage reference by scaling the output of a temperature stable bandgap circuit. The typical voltage reference is designed at 0.8 V. For $V_{IN} < 6.5$ V, in order to maintain a stable 3.3-V output voltage, a minimum 15-mA current is needed to apply at the output.

Bootstrap Voltage (BOOT)

The TPS5403 has an integrated boot regulator and requires a 0.1- μ F ceramic capacitor between the BOOT and LX pins to provide the gate drive voltage for the high-side MOSFET. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS5403 is designed to operate at 100% duty cycle as long as the BOOT to LX pin voltage is greater than 2.1 V typically.

Programmable Slow Start Using SS Pin

It is recommended to program the slow start time externally because no slow start time is implemented internally. The TPS5403 effectively uses the lower voltage of the internal voltage reference or the SS pin voltage as the power supply's reference voltage fed into the error amplifier and will regulate the output accordingly. A capacitor (C_{SS}) on the SS pin to ground implements a slow start time. The TPS5403 has an internal pull-up current source of 2 μ A that charges the external slow start capacitor. The equation for the slow start time (10% to 90%) is shown in [Equation 2](#). The internal V_{ref} is 0.8 V and the I_{SS} current is 2 μ A.

$$t_{ss}(\text{ms}) = \frac{C_{ss}(\text{nF}) \times V_{ref}(\text{V})}{I_{ss}(\mu\text{A})} \quad (2)$$

The slow start time should be set between 1 ms to 10 ms to ensure good start-up behavior. The slow start capacitor should be no more than 27 nF.

If during normal operation, the input voltage drops below the V_{IN} UVLO threshold, or a thermal shutdown event occurs, the TPS5403 stops switching.

Error Amplifier

The TPS5403 has a transconductance amplifier for the error amplifier. The error amplifier compares the V_{SENSE} voltage to the internal effective voltage reference presented at the input of the error amplifier. The transconductance of the error amplifier is 92 μ A/V during normal operation. Frequency compensation components are connected between the COMP pin and ground.

Slope Compensation

To prevent the sub-harmonic oscillations when operating the device at duty cycles greater than 50%, the TPS5403 adds a built-in slope compensation which is a compensating ramp to the switch current signal.

Overcurrent Protection and Frequency Shift

The TPS5403 implements current mode control that uses the COMP pin voltage to turn off the high-side MOSFET on a cycle by cycle basis. Every cycle the switch current and the COMP pin voltage are compared; when the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limits the output current.

The TPS5403 provides robust protection during short circuits. There is potential for overcurrent runaway in the output inductor during a short circuit at the output. The TPS5403 solves this issue by increasing the off time during short circuit conditions by lowering the switching frequency. The switching frequency is divided by 8, 4, 2, and 1 as the voltage ramps from 0 V to 3.3 V on the VSENSE pin. The relationship between the switching frequency and the VSENSE pin voltage is shown in [Table 1](#).

Table 1. Switching Frequency Conditions

| SWITCHING FREQUENCY | VSENSE PIN VOLTAGE |
|---------------------|---|
| f_{sw} | $V_{SENSE} \geq 2.4 \text{ V}$ |
| $f_{sw}/2$ | $2.4 \text{ V} > V_{SENSE} \geq 1.65 \text{ V}$ |
| $f_{sw}/4$ | $1.65 \text{ V} > V_{SENSE} \geq 0.825 \text{ V}$ |
| $f_{sw}/8$ | $0.825 \text{ V} > V_{SENSE}$ |

Spread Spectrum

In order to reduce EMI, TPS5403 introduces frequency spread spectrum. The jittering span is $\pm 6\%$ of the switching frequency with $1/512$ swing frequency.

Switching Node Anti-Ringing

When the non-synchronous buck converter operates in DCM mode, the filter inductor and the parasitic capacitance in the switching node (LX) form an LC resonant circuit; due to its high Q factor, lengthy high frequency oscillation can be observed in the switching node. This ringing could cause radiated EMI issues in some systems. TPS5403 adds an anti-ringing circuit to prevent the ringing from happening, when the inductor current crosses zero and LX starts to climb up, an internal MOSFET between LX and VSENSE is turned on, providing a damping path for the resonant circuit so as to eliminate the ringing.

Overvoltage Transient Protection

The TPS5403 incorporates an overvoltage transient protection (OVTP) circuit to minimize output voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and internal thresholds. When the VSENSE pin voltage goes above $109\% \times V_{ref}$, the high-side MOSFET will be forced off. When the VSENSE pin voltage falls below $107\% \times V_{ref}$, the high-side MOSFET will be enabled again.

Inductor Selection

The higher operating frequency allows the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of switching loss and MOSFET gate charge losses. In addition to this basic trade-off, the effect of the inductor value on ripple current and low current operation must also be considered. The ripple current depends on the inductor value. The inductor ripple current (i_L) decreases with higher inductance or higher frequency and increases with higher input voltage (V_{IN}). Accepting larger values of i_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses.

To calculate the value of the output inductor, use [Equation 3](#). LIR is a coefficient that represents inductor peak-to-peak ripple to DC load current. It is recommended to set LIR to 0.1 ~ 0.3 for most applications.

Actual core loss of the inductor is independent of core size for a fixed inductor value, but it is very dependent on the inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. It results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate. It is important that the RMS current and saturation current ratings are not exceeding the inductor specification. The RMS and peak inductor current can be calculated from [Equation 5](#) and [Equation 6](#).

$$L = \frac{V_{IN} - V_{OUT}}{I_O \cdot LIR} \cdot \frac{V_{OUT}}{V_{IN} \cdot f_{SW}} \quad (3)$$

$$\Delta i_L = \frac{V_{IN} - V_{OUT}}{I_O} \cdot \frac{V_{OUT}}{V_{IN} \cdot f_{SW}} \quad (4)$$

$$i_{LRMS} = \sqrt{I_O^2 + \frac{\left(\frac{V_{OUT} \cdot (V_{INmax} - V_{OUT})}{V_{INmax} \cdot L \cdot f_{SW}}\right)^2}{12}} \quad (5)$$

$$I_{Lpeak} = I_O + \frac{\Delta i_L}{2} \quad (6)$$

For this design example, use LIR = 0.3 and the inductor is calculated to be 13.3 μ H with $V_{IN} = 12$ V, $V_{OUT} = 3.3$ V and $f_{SW} = 300$ kHz. Choose 13 μ H value for the standard inductor and the peak to peak inductor ripple is about 34% of 2-A DC load current.

Output Capacitor Selection

There are two primary considerations for selecting the value of the output capacitor. The output capacitors are selected to meet load transient and output ripple's requirements.

[Equation 7](#) gives the minimum output capacitance to meet the transient specification. For this example, $L = 13$ μ H, $\Delta I_{OUT} = 2$ A – 0.0 A = 2 A and $\Delta V_{OUT} = 330$ mV (10% of regulated 3.3V). Using these numbers gives a minimum capacitance of 24 μ F. A standard 33- μ F ceramic is chosen in the design.

$$C_O > \frac{\Delta I_{OUT}^2 \cdot L}{2 \cdot V_{OUT} \cdot \Delta V_{OUT}} \quad (7)$$

The selection of C_O is driven by the effective series resistance (ESR). [Equation 8](#) calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, ΔV_{OUT} is the maximum allowable output voltage ripple, and Δi_L is the inductor ripple current. In this case, the maximum output voltage ripple is 33 mV (1% of regulated 3.3 V). From [Equation 4](#), the output current ripple is 0.6 A. From [Equation 8](#), the minimum output capacitance meeting the output voltage ripple requirement is 8.3 μ F with 3-m Ω ESR resistance.

$$C_O > \frac{1}{8 \cdot f_{SW}} \cdot \frac{1}{\frac{\Delta V_{OUT}}{\Delta i_L} - ESR} \quad (8)$$

After considering both requirements, for this example, one 22- μ F, 6.3-V X7R ceramic capacitor with 3-m Ω ESR should be used.

Input Capacitor Selection

A minimum 10- μ F X7R/X5R ceramic input capacitor is recommended to be added between V_{IN} and GND. These capacitors should be connected as close as physically possible to the input pins of the converters as they handle the RMS ripple current shown in [Equation 9](#). For this example, $I_{OUT} = 2$ A, $V_{OUT} = 3.3$ V, minimum $V_{INmin} = 9.6$ V, from [Equation 9](#), the input capacitors must support a ripple current of 1.15-A RMS.

$$I_{INRMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{INmin}} \cdot \frac{(V_{INmin} - V_{OUT})}{V_{INmin}}} \quad (9)$$

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using [Equation 10](#). Using the design example values, $I_{OUTmax} = 2$ A, $C_{IN} = 10$ μ F, $f_{SW} = 300$ kHz, yields an input voltage ripple of 167 mV.

$$\Delta V_{IN} = \frac{I_{OUTmax} \cdot 0.25}{C_{IN} \cdot f_{SW}} \quad (10)$$

To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current must be used.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 165°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 165°C, the device reinitiates the power up sequence.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS5403DR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T5403 |
| TPS5403DR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T5403 |
| TPS5403DRG4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T5403 |
| TPS5403DRG4.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T5403 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS5403DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS5403DRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS5403DR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TPS5403DRG4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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