

SN54ABT543A, SN74ABT543A OCTAL REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS157F – JANUARY 1991 – REVISED MAY 1997

- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

description

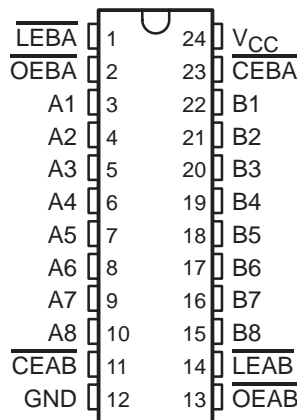
The 'ABT543A octal transceivers contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (\overline{CEAB}) input must be low to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

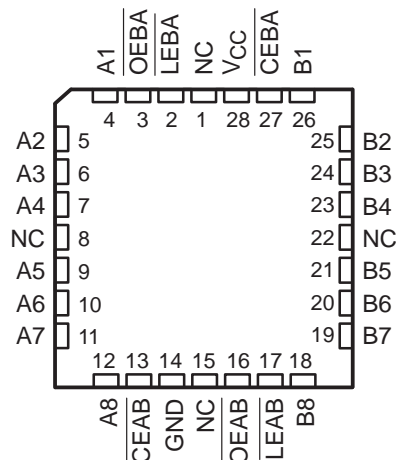
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT543A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT543A is characterized for operation from -40°C to 85°C .

SN54ABT543A . . . JT OR W PACKAGE
SN74ABT543A . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT543A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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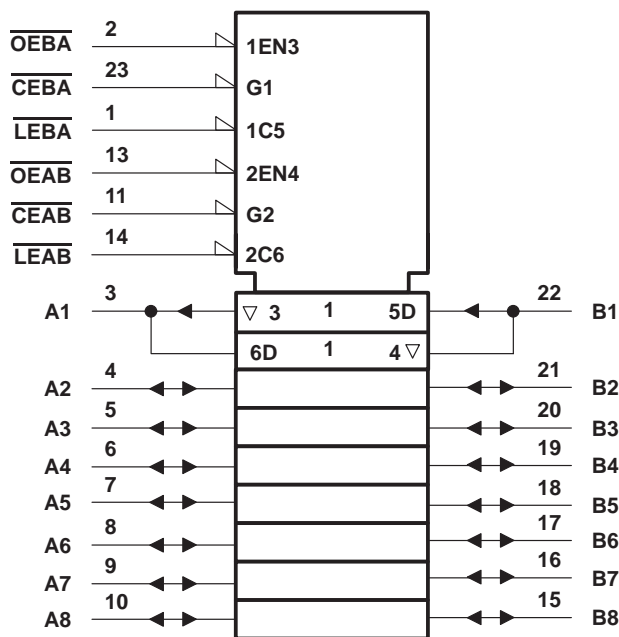
FUNCTION TABLE†

INPUTS				OUTPUT B
\overline{CEAB}	\overline{LEAB}	\overline{OEAB}	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^\ddagger
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} .

‡ Output level before the indicated steady-state input conditions were established

logic symbols§

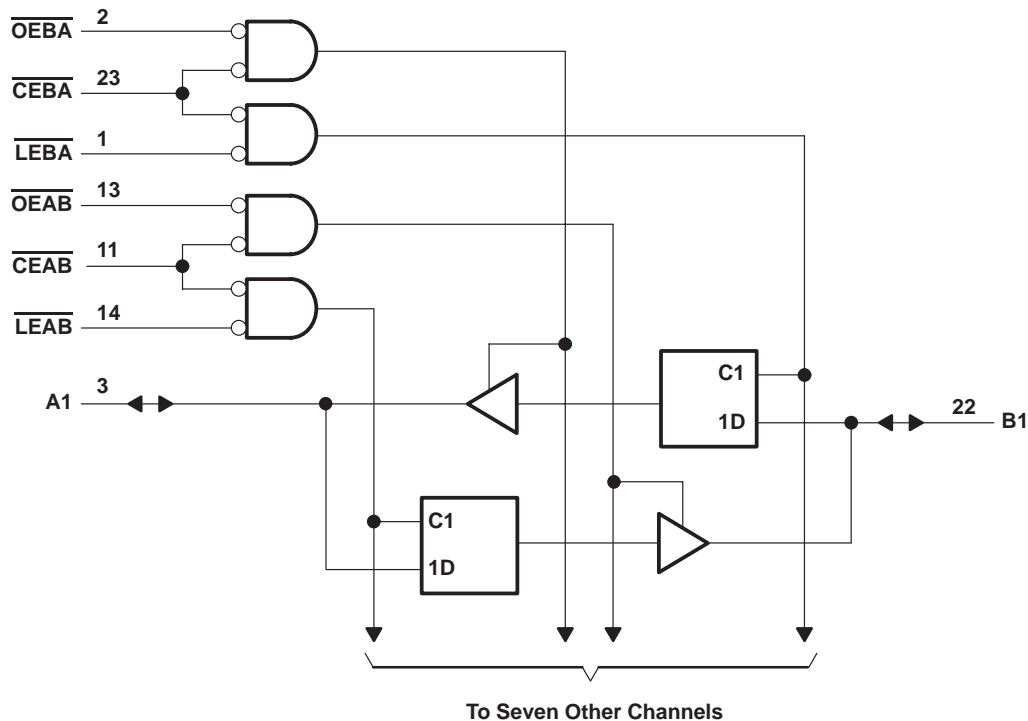


§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT543A	96 mA
SN74ABT543A	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

		SN54ABT543A		SN74ABT543A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		5	5	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT543A		SN74ABT543A		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5		2.5		2.5		V	
	V _{CC} = 5 V, I _{OH} = -3 mA		3		3		3			
	V _{CC} = 4.5 V	I _{OH} = -24 mA		2		2				
								2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V	
		I _{OL} = 64 mA		0.55*			0.55			
V _{hys}			100						mV	
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1		±1		±1	μA	
	A or B ports			±100		±100		±100		
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V			10§		10§		10§	μA	
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V			-10§		-10§		-10§	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	μA	
I _O ¶	V _{CC} = 5.5 V, V _O = 2.5 V		-50*	-100	-180*	-50	-200	-50	-180	mA
I _{CC}	A or B ports	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	1	250*		350		250	μA
			Outputs low	24	30*		34		30	mA
			Outputs disabled	0.5	250*		350		250	μA
ΔI _{CC} #	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA	
C _i	Control inputs	V _I = 2.5 V or 0.5 V		4					pF	
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		7					pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ This data sheet limit may vary among suppliers.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



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OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABT543A		UNIT		
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX
			MIN	MAX			
t _w	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low		3.5	3.5	ns		
t _{su}	Setup time	Data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	High	2.5	2.5	ns	
			Low	3	3		
	Data before $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	High	2.5	2.5			
		Low	3	3			
t _h	Hold time	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$		1	1	ns	
		Data after $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$		1	1		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN74ABT543A		UNIT		
			V _{CC} = 5 V, T _A = 25°C			MIN	MAX
			MIN	MAX			
t _w	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low		3.5	3.5	ns		
t _{su}	Setup time	Data before $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	High	3.5	3.5	ns	
			Low	3	3		
	Data before $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	High	3.5	3.5			
		Low	3	3			
t _h	Hold time	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$		0.5	0.5	ns	
		Data after $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$		0.5	0.5		



SN54ABT543A, SN74ABT543A
OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT543A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.6†	4.4	4.4	1.6†	5.5	ns
t_{PHL}			1.6	4.4	5.1	1.6	6.2	
t_{PLH}	\overline{LEBA} or \overline{LEAB}	A or B	1.6†	4.1	5.1	1.6†	6.6	ns
t_{PHL}			1.6	4.6	5.4	1.6	6.4	
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	1.4	3.9	4.1	1.4	5.1	ns
t_{PZL}			2	5	4.9	2	5.8	
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	2.5†	5.9	5.8	2.5†	6.9	ns
t_{PLZ}			2.5†	5.5	6.1	2.5†	7.6	
t_{PZH}	\overline{CEBA} or \overline{CEAB}	A or B	1.4	3.9	4.7	1.4	5.6	ns
t_{PZL}			2	5	5.7	2	6.2	
t_{PHZ}	CEBA or CEAB	A or B	3.2†	5.9	6.5	3.2†	7.3	ns
t_{PLZ}			2.5†	5.5	6.7	2.5†	7.8	

† This data sheet limit may vary among suppliers.

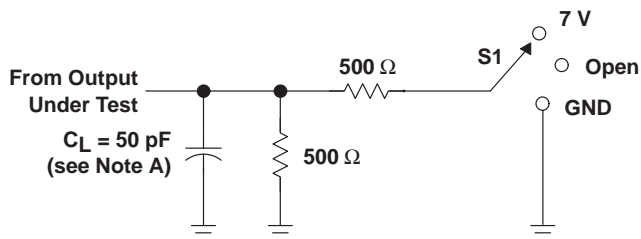
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT543A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.8†	4.4	5.9	1.8†	6.9	ns
t_{PHL}			1.9	4.4	5.9	1.9	6.9	
t_{PLH}	\overline{LEBA} or \overline{LEAB}	A or B	1.5†	4.1	5.6	1.5†	6.6	ns
t_{PHL}			2.1	4.6	6.1	2.1	7.1	
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	1.4	3.9	5.4	1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5	7.5	
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	2.5†	5.9	7.4	2.5†	8.4	ns
t_{PLZ}			2.5†	5.5	7	2.5†	8	
t_{PZH}	\overline{CEBA} or \overline{CEAB}	A or B	1.4	3.9	5.4	1.4	6.4	ns
t_{PZL}			2.5	5	6.5	2.5	7.5	
t_{PHZ}	\overline{CEBA} or \overline{CEAB}	A or B	2.9†	5.9	7.4	2.9†	8.4	ns
t_{PLZ}			2.4†	5.5	7	2.4†	8	

† This data sheet limit may vary among suppliers.

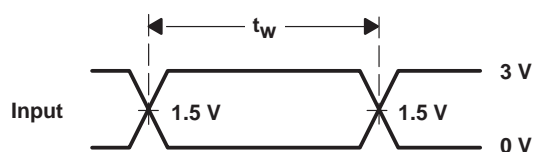


PARAMETER MEASUREMENT INFORMATION

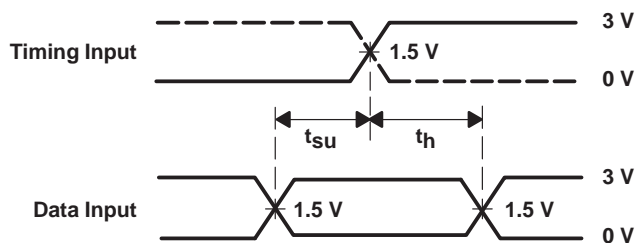


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

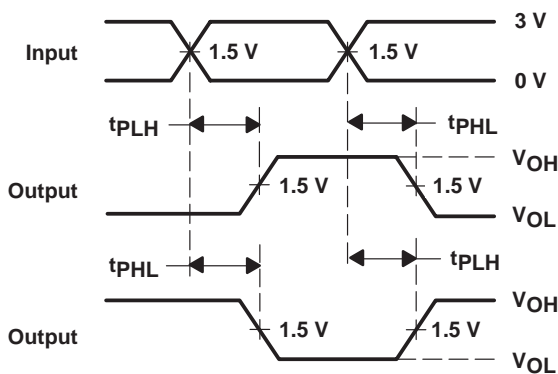
LOAD CIRCUIT



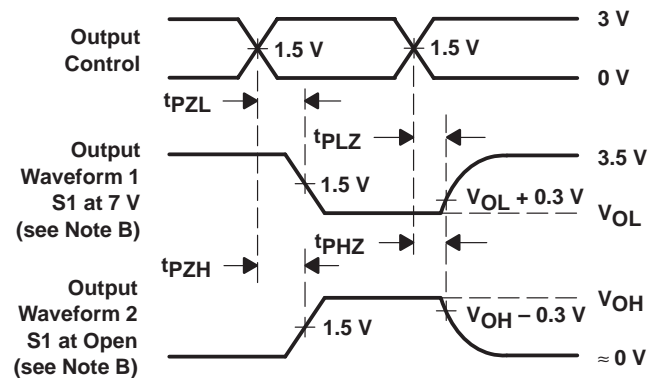
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9231402Q3A	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9231402Q3A SNJ54 ABT543AFK
SN74ABT543ADBR	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A
SN74ABT543ADBR.B	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A
SN74ABT543ADBRG4	Active	Production	SSOP (DB) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A
SN74ABT543ADW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT543A
SN74ABT543ADW.B	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT543A
SN74ABT543ADWR	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT543A
SN74ABT543ADWR.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT543A
SN74ABT543ADWRG4.B	Active	Production	SOIC (DW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT543A
SN74ABT543APW	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A
SN74ABT543APW.B	Active	Production	TSSOP (PW) 24	60 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A
SN74ABT543APWR	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A
SN74ABT543APWR.B	Active	Production	TSSOP (PW) 24	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB543A
SNJ54ABT543AFK	Active	Production	LCCC (FK) 28	42 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9231402Q3A SNJ54 ABT543AFK

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ABT543A, SN74ABT543A :

- Catalog : [SN74ABT543A](#)
- Military : [SN54ABT543A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

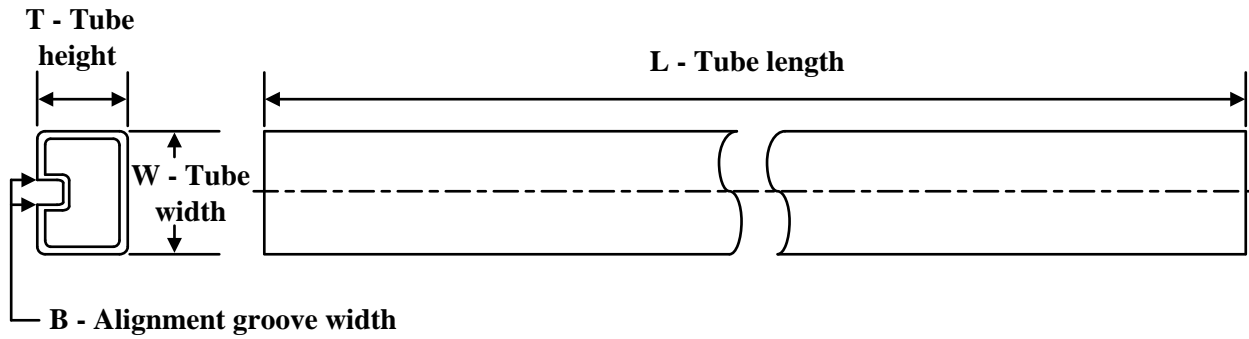
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT543ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT543ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74ABT543APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT543ADBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74ABT543ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74ABT543APWR	TSSOP	PW	24	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT543ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT543ADW.B	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ABT543APW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74ABT543APW.B	PW	TSSOP	24	60	530	10.2	3600	3.5

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

EXAMPLE BOARD LAYOUT

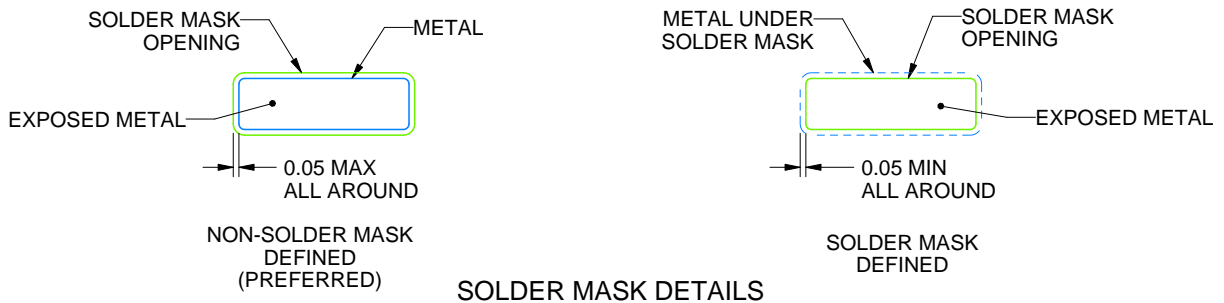
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

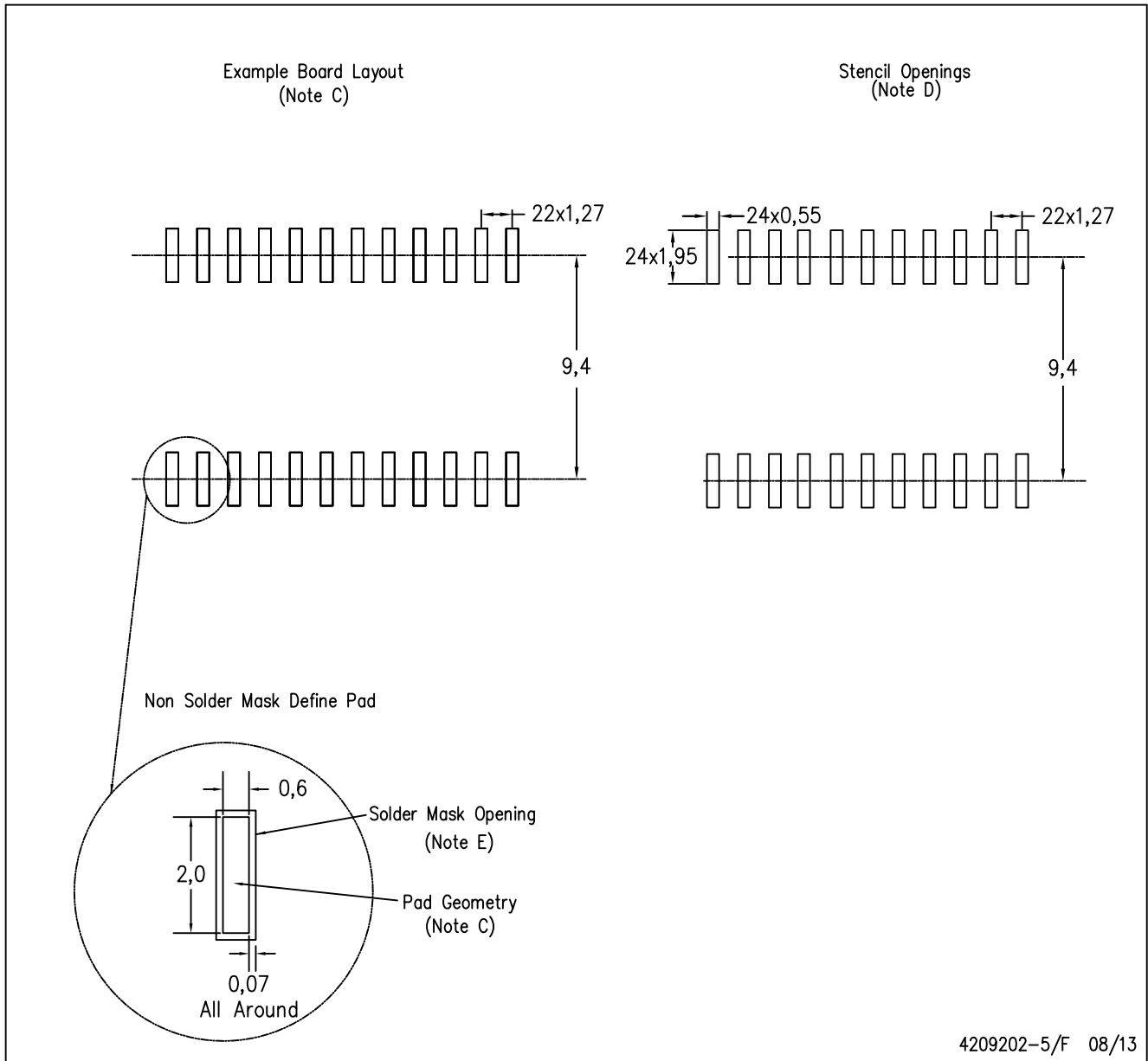
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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