

# SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

SDAS224B – JUNE 1982 – REVISED NOVEMBER 1995

- Compare Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- SN74ALS518 and 'ALS520 Have 20-kΩ Pullup Resistors on Q Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

TYPE	INPUT PULLUP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
SN74ALS518	Yes	P = Q open collector
'ALS520	Yes	$\overline{P = Q}$ totem pole
SN74ALS521 <sup>‡</sup>	No	P = Q totem pole

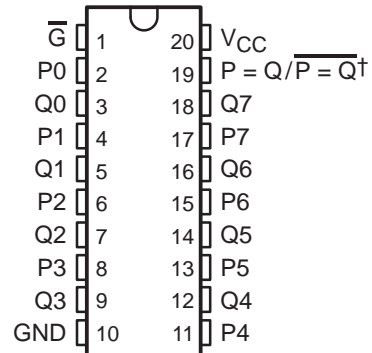
<sup>‡</sup> SN74ALS521 is identical to 'ALS688.

## description

These identity comparators perform comparisons on two 8-bit binary or BCD words. The SN74ALS518 provides P = Q outputs, while the 'ALS520 and SN74ALS521 provide  $\overline{P = Q}$  outputs. The SN74ALS518 has an open-collector output. The SN74ALS518 and 'ALS520 feature 20-kΩ pullup resistors on the Q inputs for analog or switch data.

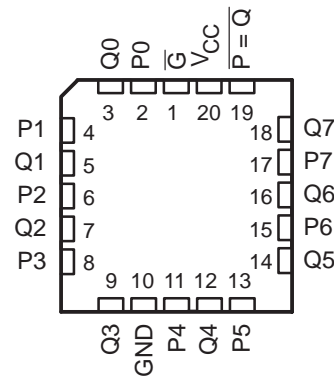
The SN54ALS520 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74ALS518, SN74ALS520, and SN74ALS521 are characterized for operation from 0°C to 70°C.

SN54ALS520 . . . J PACKAGE  
SN74ALS518, SN74ALS520,  
SN74ALS521 . . . DW OR N PACKAGE  
(TOP VIEW)



<sup>†</sup> P = Q for SN74ALS518  
P = Q for 'ALS520 and SN74ALS521

SN54ALS520 . . . FK PACKAGE  
(TOP VIEW)



FUNCTION TABLE

INPUTS		OUTPUTS	
DATA P, Q	ENABLE $\overline{G}$	P = Q	$\overline{P = Q}$
P = Q	L	H	L
P > Q	L	L	H
P < Q	L	L	H
X	H	L	H

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



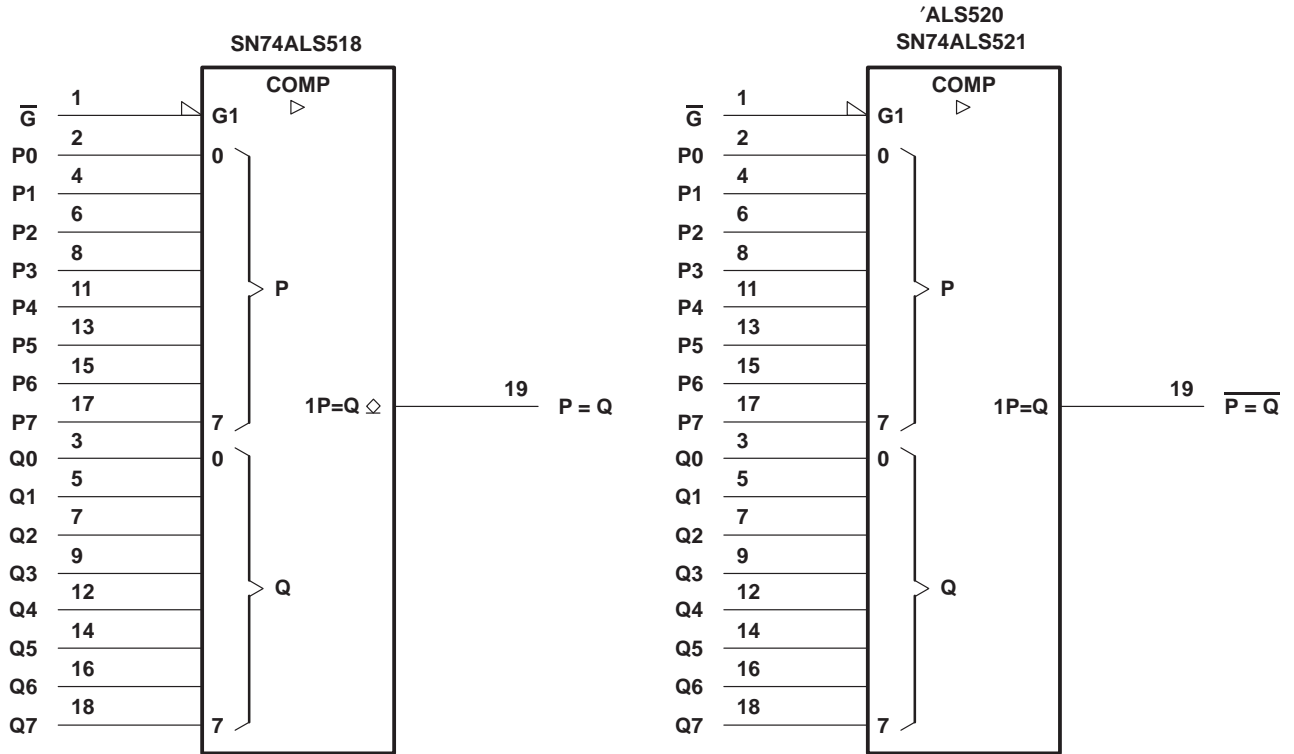
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# SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

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## logic symbols†

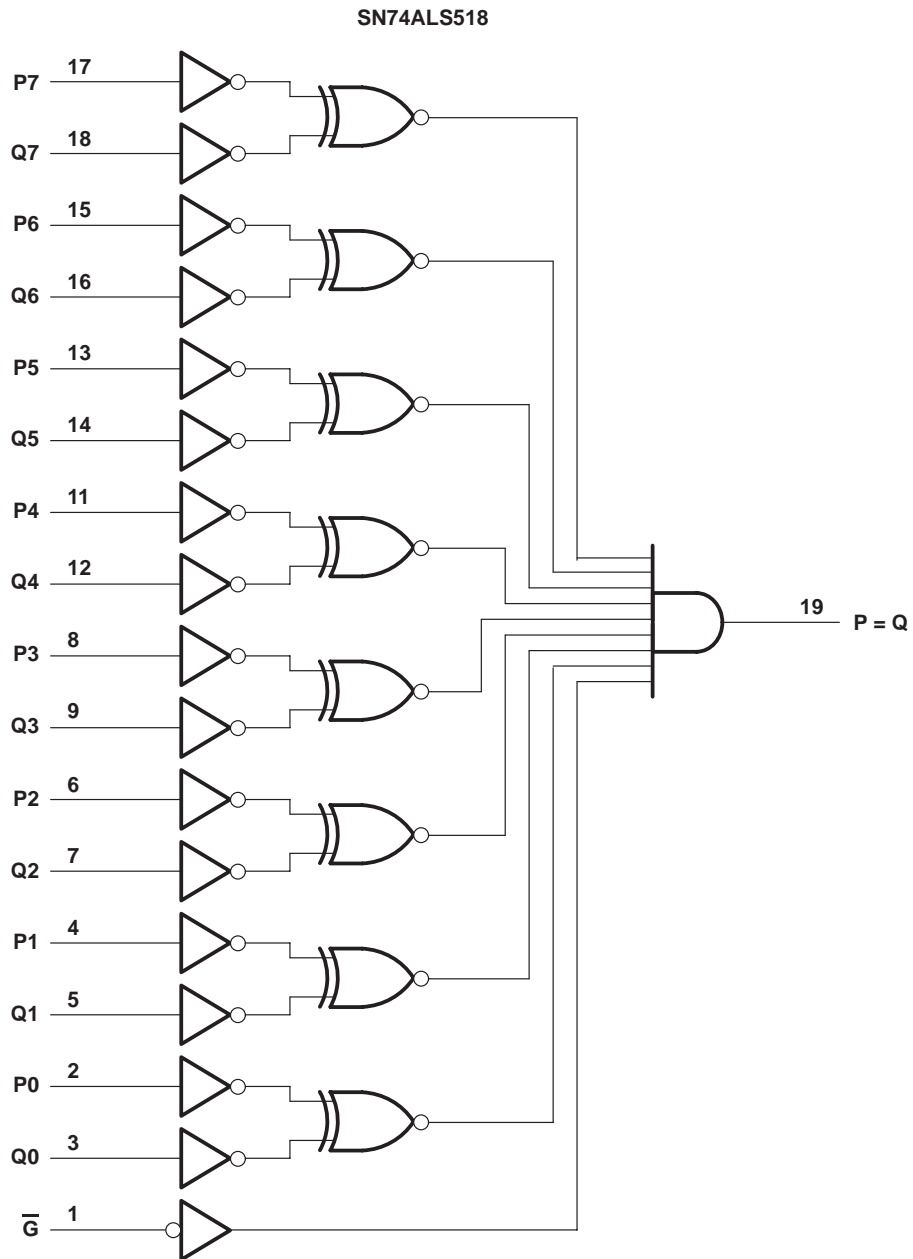


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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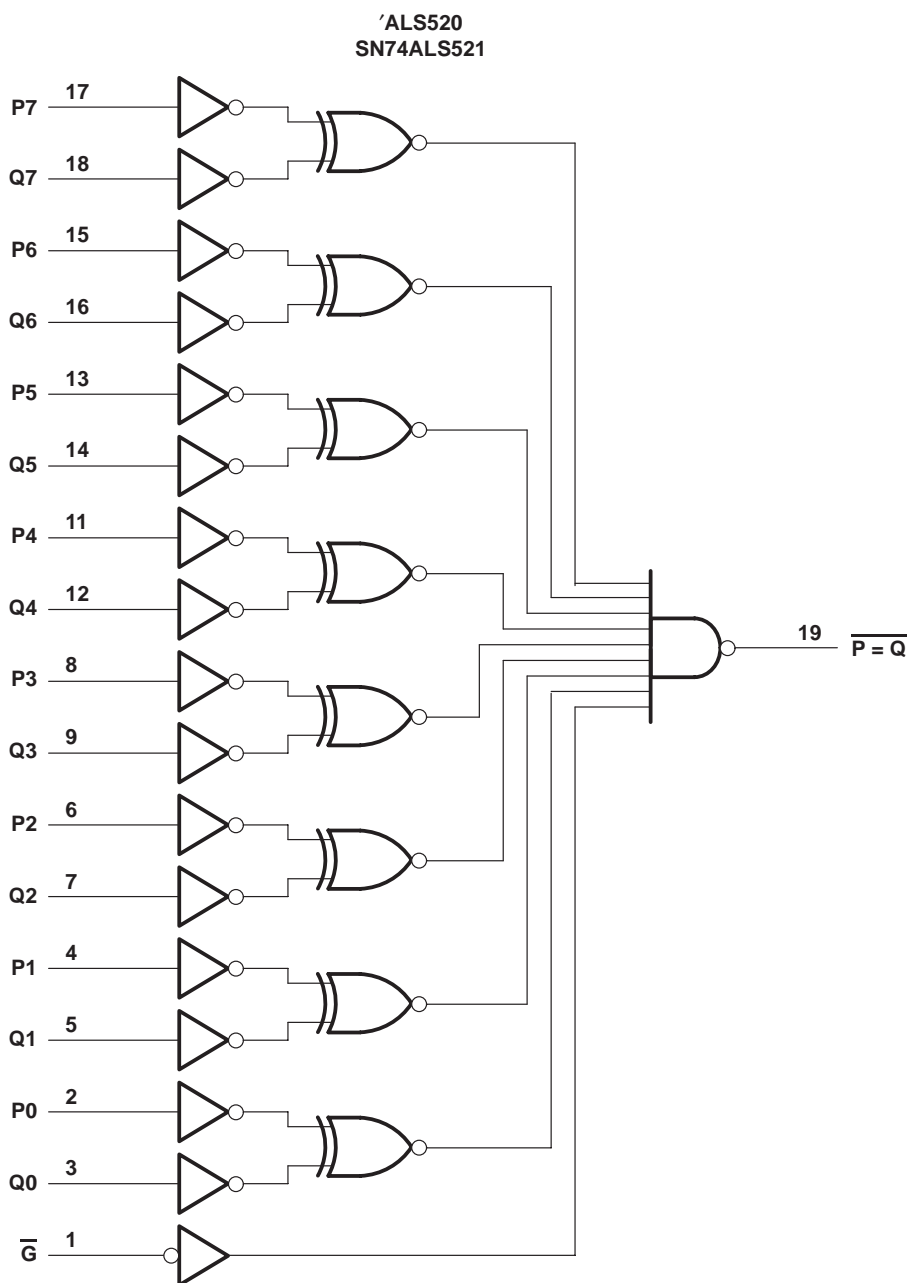
## logic diagrams (positive logic)



# SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

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## logic diagrams (positive logic) (continued)



# SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ : Q inputs .....	$V_{CC} + 0.5$ V or 5.5 V, whichever is less
All other inputs .....	7 V
Off-state output voltage .....	7 V
Operating free-air temperature range, $T_A$ : SN74ALS518 .....	0°C to 70°C
Storage temperature range .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		SN74ALS518			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$V_{OH}$	High-level output voltage			5.5	V
$I_{OL}$	Low-level output current			24	mA
$T_A$	Operating free-air temperature	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS518		UNIT
				MIN	TYP‡	
$V_{IK}$		$V_{CC} = 4.5$ V,	$I_I = -18$ mA		–1.5	V
$I_{OH}$		$V_{CC} = 5.5$ V,	$V_{OH} = 5.5$ V		0.1	mA
$V_{OL}$		$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA	0.25	0.4	V
			$I_{OL} = 24$ mA	0.35	0.5	
$I_I$	Q inputs	$V_{CC} = 5.5$ V	$V_I = 5.5$ V		0.1	mA
	All other inputs		$V_I = 7$ V		0.1	
$I_{IH}$	Q inputs	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V		–0.2	mA
	All other inputs				20	
$I_{IL}$	Q inputs	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V		–0.6	mA
	All other inputs				–0.1	
$I_{CC}$		$V_{CC} = 5.5$ V,	See Note 1	11	17	mA

‡ All typical values are at  $V_{CC} = 5$  V,  $T_A = 25$ °C.

NOTE 1:  $I_{CC}$  is measured with  $\bar{G}$  grounded, and P and Q at 4.5 V.



# SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

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## switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 680 Ω, T <sub>A</sub> = MIN to MAX†		UNIT
			SN74ALS518		
			MIN	MAX	
t <sub>PLH</sub>	P or Q	P = Q	15	33	ns
t <sub>PHL</sub>			3	15	
t <sub>PLH</sub>	$\bar{G}$	P = Q	15	33	ns
t <sub>PHL</sub>			3	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V <sub>CC</sub>	7 V
Input voltage, V <sub>I</sub> : Q inputs of 'ALS520	V <sub>CC</sub> + 0.5 V or 5.5 V, whichever is less
All other inputs	7 V
Operating free-air temperature range, T <sub>A</sub> : SN54ALS520	–55°C to 125°C
SN74ALS520, SN74ALS521	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

	SN54ALS520			SN74ALS520 SN74ALS521			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub> High-level input voltage	2			2			V
V <sub>IL</sub> Low-level input voltage			0.7			0.8	V
I <sub>OH</sub> High-level output current			–1			–2.6	mA
I <sub>OL</sub> Low-level output current			12			24	mA
T <sub>A</sub> Operating free-air temperature	–55		125	0		70	°C

# SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

SDAS224B – JUNE 1982 – REVISED NOVEMBER 1995

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	SN54ALS520			SN74ALS520 SN74ALS521			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$	-1.5			-1.5			V
$V_{OH}$		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
		$V_{CC} = 4.5\text{ V}$ $I_{OH} = -1\text{ mA}$	2.4	3.3					
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ $I_{OL} = 12\text{ mA}$	0.25	0.4	0.25	0.4			V
		$V_{CC} = 4.5\text{ V}$ $I_{OL} = 24\text{ mA}$			0.35	0.5			
$I_I$	'ALS520 Q inputs	$V_{CC} = 5.5\text{ V}$ $V_I = 5.5\text{ V}$	0.1			0.1			mA
	All other inputs		0.1			0.1			
$I_{IH}$	'ALS520 Q inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 2.7\text{ V}$	-0.2			-0.2			mA
	All other inputs		20			20			
$I_{IL}$	'ALS520 Q inputs	$V_{CC} = 5.5\text{ V}$ , $V_I = 0.4\text{ V}$	-0.6			-0.6			mA
	All other inputs		-0.1			-0.1			
$I_O^\ddagger$		$V_{CC} = 5.5\text{ V}$ , $V_O = 2.25\text{ V}$	-20	-112	-30	-112			mA
$I_{CC}$	'ALS520	$V_{CC} = 5.5\text{ V}$ , See Note 1	12	19	12	19			mA
	SN74ALS521		12	19	12	19			

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .

NOTE 1:  $I_{CC}$  is measured with  $\bar{G}$  grounded, and P and Q at 4.5 V.

## switching characteristics (see Figure 1)

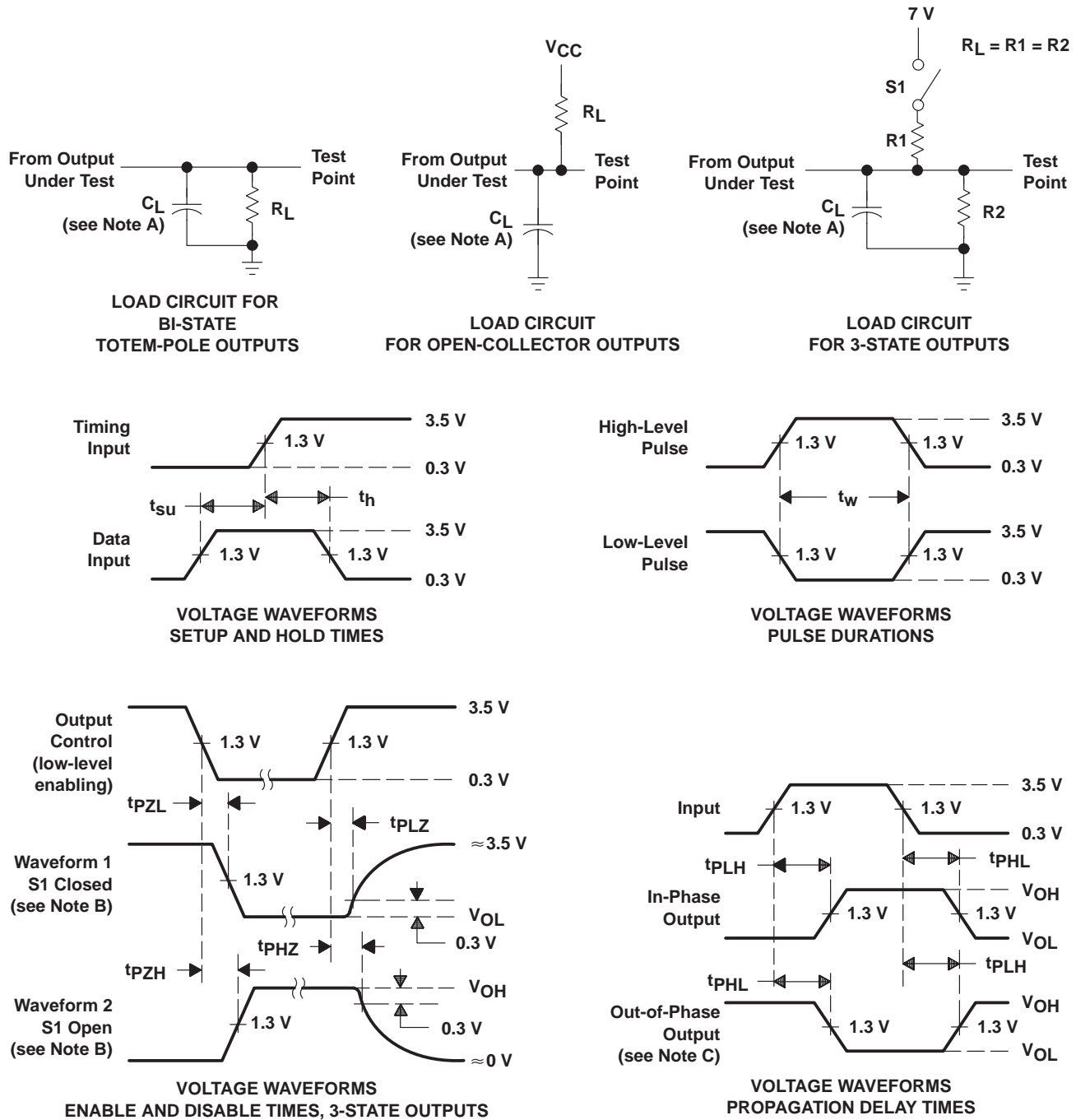
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $C_L = 50\text{ pF}$ , $R_L = 500\ \Omega$ , $T_A = \text{MIN to MAX}^\S$				UNIT
			SN54ALS520		SN74ALS520 SN74ALS521		
			MIN	MAX	MIN	MAX	
$t_{PLH}$	P or Q	$\overline{P = Q}$	3	19	3	12	ns
$t_{PHL}$			3	25	5	20	
$t_{PLH}$	G	$P = Q$	2	18	2	12	ns
$t_{PHL}$			5	23	5	22	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

# SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-88691012A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88691012A SNJ54ALS 520FK
<a href="#">5962-8869101RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8869101RA SNJ54ALS520J
<a href="#">SN54ALS520J</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS520J
<a href="#">SN54ALS520J.A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS520J
<a href="#">SN74ALS518DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS518
<a href="#">SN74ALS518DW.A</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS518
<a href="#">SN74ALS518DWE4</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS518
<a href="#">SN74ALS518N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS518N
<a href="#">SN74ALS518N.A</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS518N
<a href="#">SN74ALS520DW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS520
<a href="#">SN74ALS520DW.A</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS520
<a href="#">SN74ALS520N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS520N
<a href="#">SN74ALS520N.A</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS520N
<a href="#">SN74ALS520NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS520
<a href="#">SN74ALS520NSR.A</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS520
<a href="#">SN74ALS521DW</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	0 to 70	ALS521
<a href="#">SN74ALS521DWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS521
<a href="#">SN74ALS521DWR.A</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS521
<a href="#">SN74ALS521N</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS521N
<a href="#">SN74ALS521N.A</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS521N
<a href="#">SN74ALS521NSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS521
<a href="#">SN74ALS521NSR.A</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS521
<a href="#">SNJ54ALS520FK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88691012A SNJ54ALS 520FK

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ALS520FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 88691012A SNJ54ALS 520FK
<a href="#">SNJ54ALS520J</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8869101RA SNJ54ALS520J
SNJ54ALS520J.A	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8869101RA SNJ54ALS520J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54ALS520, SN74ALS520 :**

- Catalog : [SN74ALS520](#)
- Military : [SN54ALS520](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

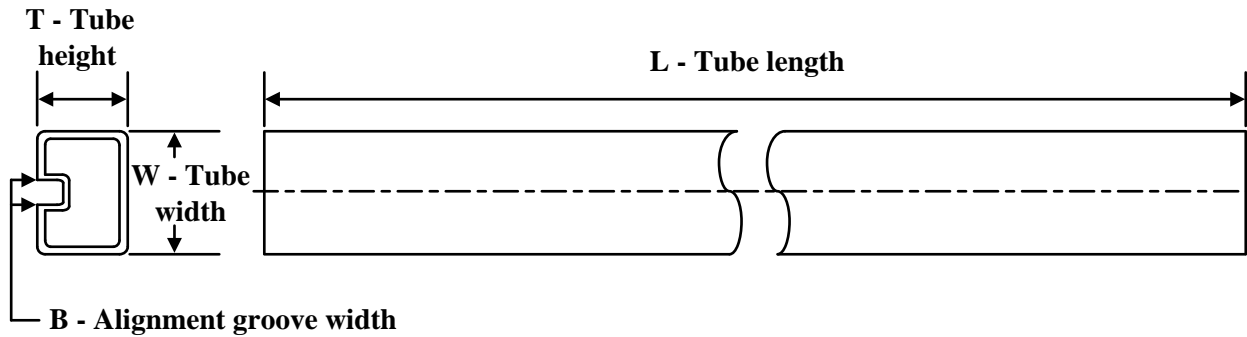

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS520NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS521DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS521NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS520NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74ALS521DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS521NSR	SOP	NS	20	2000	367.0	367.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-88691012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS518DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS518DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS518DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS518N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS518N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS520DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS520DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS520N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS520N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS521N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS521N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS520FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS520FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



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**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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