SN74LVC595A 8-Bit Shift Register With 3-State Output Registers

1 Features

- Operating range from 1.1V to 3.6V
- Over-voltage tolerant inputs support up to 5.5V independent of V_{CC}
- Supports partial-power-down with back drive protection (I_{off})
- High push-pull output drive strength:
  - ±24mA at 3.3V
  - ±8mA at 2.3V
  - ±4mA at 1.65V
- Latch-up performance exceeds 250mA per JESD78

2 Applications

- Network switches
- Power infrastructures
- LED displays
- Servers

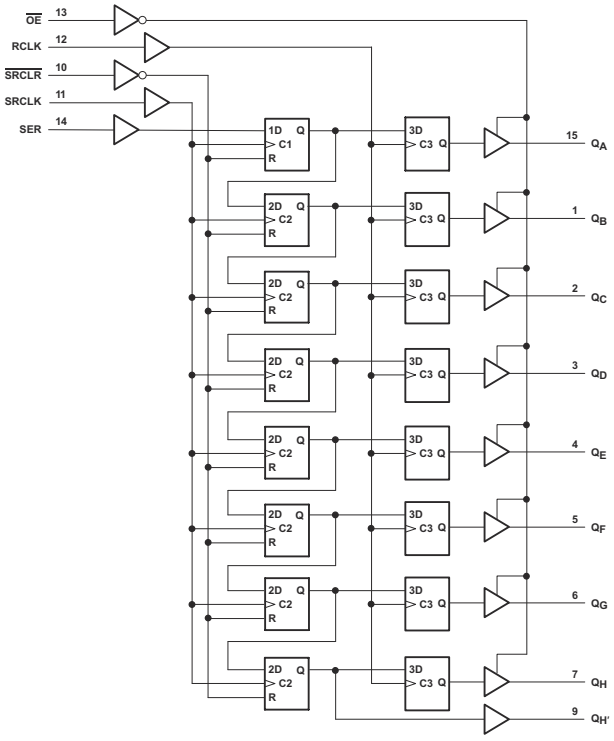
3 Description

The SN74LVC595A device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear ($\overline{SRCLR}$) input, a serial (SER) input, and a serial output for cascading. When the output-enable ($\overline{OE}$) input is high, all outputs except QH′ are in the high-impedance state.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74LVC595A	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.4mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length x width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

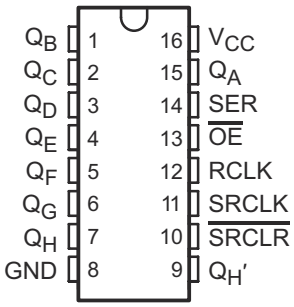

Figure 4-1. PW Package 16-Pin TSSOP (Top View)

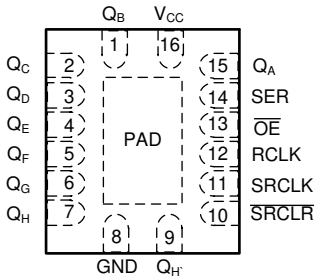

Figure 4-2. BQB Package, 16-Pin WQFN (Top View)

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	8	—	Ground Pin
$\overline{OE}$	13	I	Output Enable
Q_A	15	O	Q_A Output
Q_B	1	O	Q_B Output
Q_C	2	O	Q_C Output
Q_D	3	O	Q_D Output
Q_E	4	O	Q_E Output
Q_F	5	O	Q_F Output
Q_G	6	O	Q_G Output
Q_H	7	O	Q_H Output
$Q_{H'}$	9	O	$Q_{H'}$ Output
RCLK	12	I	RCLK Input
SER	14	I	SER Input
SRCLK	11	I	SRCLK Input
$\overline{SRCLR}$	10	I	$\overline{SRCLR}$ Input
V_{CC}	16	—	Power Pin

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range(2)		-0.5	6.5	V
V_O	Output voltage range(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0V		-50	mA
I_{OK}	Output clamp current	V_O < 0V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SPECIFICATION	DESCRIPTION	CONDITION	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	3.6	V
V_I	Input voltage			5.5	V
V_O	Output voltage	(High or low state)		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8V		-4	mA
		V_{CC} = 2.3V		-8	
		V_{CC} = 2.7V		-12	
		V_{CC} = 3V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 2.7V		12	
		V_{CC} = 3V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	125	°C
V_{IH}	High-level input voltage	V_{CC} = 1.1V	0.75		V
V_{IH}	High-level input voltage	V_{CC} = 1.2V	0.78		V
V_{IH}	High-level input voltage	V_{CC} = 1.5V	0.975		V
V_{IH}	High-level input voltage	V_{CC} = 1.65V	1.075		V
V_{IH}	High-level input voltage	V_{CC} = 1.95V	1.2675		V
V_{IH}	High-level input voltage	V_{CC} = 2.3V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 2.7V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 3.6V	2		V
V_{IL}	Low-Level input voltage	V_{CC} = 1.1V		0.40	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.2V		0.42	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.5V		0.525	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65V		0.5775	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.95V		0.6825	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.3V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.7V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 3.6V		0.8	V

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
PW (TSSOP)	16	136.2	73.6	94.3	18.2	93.3	-	°C/W
BQB (WQFN)	16	84.4	88.8	54.5	14.1	54.4	30.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –100 µA	1.1V to 3.6V	V_{CC} - 0.2			V
V_{OH}	I_{OH}= –100 µA	1.2V to 3.6V	V_{CC} - 0.2			V
V_{OH}	I_{OH}= –4 mA	1.65V	1.2			V
V_{OH}	I_{OH}= –8 mA	2.3V	1.75			V
V_{OH}	I_{OH}= –12 mA	2.7V	2.2			V
V_{OH}		3V	2.4			V
V_{OH}	I_{OH}= –24 mA	3V	2.2			V
V_{OL}	I_{OL}= 100 µA	1.1V to 3.6V			0.15	V
V_{OL}	I_{OL}= 100 µA	1.2V to 3.6V			0.2	V
V_{OL}	I_{OL}= 4 mA	1.65V			0.45	V
V_{OL}	I_{OL}= 8 mA	2.3V			0.7	V
V_{OL}	I_{OL}= 12 mA	2.7V			0.4	V
V_{OL}		3V			0.45	V
V_{OL}	I_{OL}= 24 mA	3V			0.55	V
I_I	V_I = V_{CC} or GND	3.6V			±5	µA
I_{off}	V_I or V_O = V_{CC}	0V			±10	µA
I_{OZ}	V_O = V_{CC} or GND	3.6V			±15	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6V			40	µA
ΔI_{CC}	One input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND	2.7V to 3.6V			500	µA
C_I	V_I = V_{CC} or GND	3.3V				pF
C_O	V_O = V_{CC} or GND	3.3V				pF
V_{POR}	V_{CC} ramp rate of 1ms/V to 100ms/V	1.1V to 1.62V			1.0	V
V_{POR}	V_{CC} ramp rate of 6µs/V to 100ms/V	1.65V to 3.6V			1.5	V
C_{PD}	f = 10 MHz	1.8V		31		pF
C_{PD}	f = 10 MHz	2.5V		31		pF
C_{PD}	f = 10 MHz	3.3V		32		pF
C_{PD}	Outputs disabled, f = 10 MHz	1.8V				pF
		2.5V				
		3.3V				

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5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See #i#Parameter Measurement Information

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	RCLK	QA - QH	C_L = 15pF	1.2V ± 0.1V		43.5	56.5	ns
t_{pd}	RCLK	QA - QH	C_L = 15pF	1.5V ± 0.12V		15	16.9	ns
t_{pd}	RCLK	QA - QH	C_L = 30pF	1.8V ± 0.15V	2.0	11.4	18.2	ns
t_{pd}	RCLK	QA - QH	C_L = 30pF	2.5V ± 0.2V	1.5	6.8	9.3	ns
t_{pd}	RCLK	QA - QH	C_L = 50pF	2.7V	1.5	6.5	8.7	ns
t_{pd}	RCLK	QA - QH	C_L = 50pF	3.3V ± 0.3V	1.2	3.4	7.7	ns
t_{pd}	SRCLK	QH'	C_L = 15pF	1.2V ± 0.1V		44	57	ns
t_{pd}	SRCLK	QH'	C_L = 15pF	1.5V ± 0.12V		15.8	16.8	ns
t_{pd}	SRCLK	QH'	C_L = 30pF	1.8V ± 0.15V	2.0	11	18.2	ns
t_{pd}	SRCLK	QH'	C_L = 30pF	2.5V ± 0.2V	1.5	6.4	9.3	ns
t_{pd}	SRCLK	QH'	C_L = 50pF	2.7V	1.5	6.1	8.7	ns
t_{pd}	SRCLK	QH'	C_L = 50pF	3.3V ± 0.3V	1.5	3.4	7.7	ns
t_{pd}	$\overline{\text{SRCLR}}$	QH'	C_L = 15pF	1.2V ± 0.1V		36	43	ns
t_{pd}	$\overline{\text{SRCLR}}$	QH'	C_L = 15pF	1.5V ± 0.12V		15.5	16.6	ns
t_{pd}	$\overline{\text{SRCLR}}$	QH'	C_L = 30pF	1.8V ± 0.15V	2.0	11.2	18.2	ns
t_{pd}	$\overline{\text{SRCLR}}$	QH'	C_L = 30pF	2.5V ± 0.2V	1.5	6.55	9.3	ns
t_{pd}	$\overline{\text{SRCLR}}$	QH'	C_L = 50pF	2.7V	1.5	6.5	8.7	ns
t_{pd}	$\overline{\text{SRCLR}}$	QH'	C_L = 50pF	3.3V ± 0.3V	1.2	3.5	7.7	ns
t_{pzh}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.2V ± 0.1V		34	42	ns
t_{pzh}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.5V ± 0.12V		13.6	14.3	ns
t_{pzh}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	1.8V ± 0.15V	2.0	10	16.2	ns
t_{pzh}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	2.5V ± 0.2V	1.5	6.1	9.2	ns
t_{pzh}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	2.7V	1.5	6.6	8.7	ns
t_{pzh}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	3.3V ± 0.3V	1.2	3.5	7.7	ns
t_{pzl}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.2V ± 0.1V		31	40.5	ns
t_{pzl}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.5V ± 0.12V		13	13.5	ns
t_{pzl}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	1.8V ± 0.15V	2.0	10	16.2	ns
t_{pzl}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	2.5V ± 0.2V	1.5	6.4	9.2	ns
t_{pzl}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	2.7V	1.5	6.6	8.7	ns
t_{pzl}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	3.3V ± 0.3V	1.2	3.5	7.7	ns
t_{phz}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.2V ± 0.1V		27.5	32	ns
t_{phz}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.5V ± 0.12V		13.5	15.5	ns
t_{phz}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	1.8V ± 0.15V	2.0	10.5	11.2	ns
t_{phz}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	2.5V ± 0.2V	1.2	6	6.6	ns
t_{phz}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	2.7V	1.2	6.41	7.1	ns
t_{phz}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	3.3V ± 0.3V	1.2	3.5	6.5	ns
t_{plz}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.2V ± 0.1V		26.5	32	ns
t_{plz}	$\overline{\text{OE}}$	QA - QH	C_L = 15pF	1.5V ± 0.12V		12.1	13.4	ns
t_{plz}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	1.8V ± 0.15V	2.0	9.2	11.2	ns
t_{plz}	$\overline{\text{OE}}$	QA - QH	C_L = 30pF	2.5V ± 0.2V	1.2	5.9	6.62	ns
t_{plz}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	2.7V	1.2	6.5	7.1	ns
t_{plz}	$\overline{\text{OE}}$	QA - QH	C_L = 50pF	3.3V ± 0.3V	1.2	3.5	6.81	ns

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over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See #i#Parameter Measurement Information

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
$t_{sk(o)}$				3.3V ± 0.3V			1	ns
C_{PD}		Outputs Enabled		1.8V		45		pf
C_{PD}		Outputs Enabled		2.5V		40		pf
C_{PD}		Outputs Enabled		3.3V		35		pf
C_{PD}		Outputs Disabled		1.8V		22		pf
C_{PD}		Outputs Disabled		2.5V		23		pf
C_{PD}		Outputs Disabled		3.3V		24		pf

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5.7 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
f_{clock}	Clock frequency		1.2V ± 0.1V		20	MHz
			1.5V ± 0.12V		100	
f_{clock}	Clock frequency		1.8V ± 0.15V		104	MHz
			2.5V ± 0.2V		115	
			2.7V		105	
			3.3V ± 0.3V		104	
t_W	Pulse duration	SRCLK high or low	1.2V ± 0.1V	20		nS
			1.5V ± 0.12V	7		
		RCLK high or low	1.2V ± 0.1V	20		
			1.5V ± 0.12V	7		
		$\overline{SRCLR}$ low	1.2V ± 0.1V	7		nS
			1.5V ± 0.12V	7		nS
t_W	Pulse duration	SRCLK high or low	1.8V ± 0.15V	7		nS
			2.5V ± 0.2V	5.5		
			2.7V	5		
			3.3V ± 0.3V	4.5		
		RCLK high or low	1.8V ± 0.15V	7		
			2.5V ± 0.2V	5.5		
			2.7V	5		
			3.3V ± 0.3V	4.5		
		$\overline{SRCLR}$ low	1.8V ± 0.15V	5.5		nS
			2.5V ± 0.2V	4.5		nS
			2.7V	3		nS
			3.3V ± 0.3V	3		nS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V_{CC}	-40°C to 125°C		UNIT
				MIN	MAX	
t_{SU}	Setup time	SER before SRCLK↑	1.2V ± 0.1V	21		nS
			1.5V ± 0.12V	5.5		
		SRCLK↑ before RCLK↑	1.2V ± 0.1V	46		
			1.5V ± 0.12V	9.5		
		$\overline{SRCLR}$ low before SRCLK↑	1.2V ± 0.1V	25.4		nS
			1.5V ± 0.12V	9.25		nS
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	1.2V ± 0.1V	12.6		nS
			1.5V ± 0.12V	5.5		nS
		$\overline{SRCLR}$ high (inactive) before RCLK↑	1.2V ± 0.1V	25.4		nS
			1.5V ± 0.12V	9.25		nS
t_{SU}	Setup time before CLK↑	SER before SRCLK↑	1.8V ± 0.15V	5.5		nS
			2.5V ± 0.2V	4.5		
			2.7V	2.5		
			3.3V ± 0.3V	2.5		
		SRCLK↑ before RCLK↑	1.8V ± 0.15V	6		
			2.5V ± 0.2V	3.5		
			2.7V	2.5		
			3.3V ± 0.3V	2.5		
		$\overline{SRCLR}$ low before SRCLK↑	1.8V ± 0.15V	8.5		nS
			2.5V ± 0.2V	5.5		nS
			2.7V	4.5		nS
			3.3V ± 0.3V	4.5		nS
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	1.8V ± 0.15V	5.5		nS
			2.5V ± 0.2V	4.5		nS
			2.7V	2.5		nS
			3.3V ± 0.3V	2.5		nS
		$\overline{RCLR}$ high (inactive) before RCLK↑	1.8V ± 0.15V	5.5		nS
			2.5V ± 0.2V	4.5		nS
			2.7V	2.5		nS
			3.3V ± 0.3V	2.5		nS
t_H	Hold time	SER after SRCLK↑	1.2V ± 0.1V	6		nS
			1.5V ± 0.12V	2.0		
t_H	Hold time	SER after SRCLK↑	1.8V ± 0.15V	2.0		nS
			2.5V ± 0.2V	2.0		
			2.7V	2.0		
			3.3V ± 0.3V	1.5		

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5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

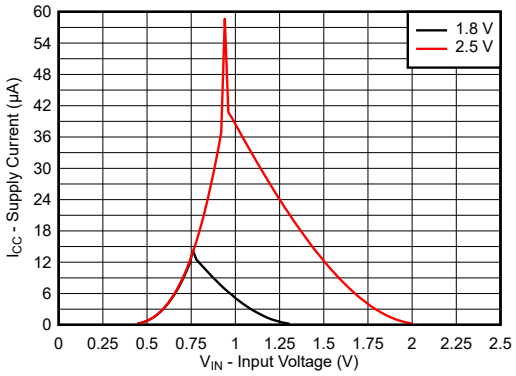


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

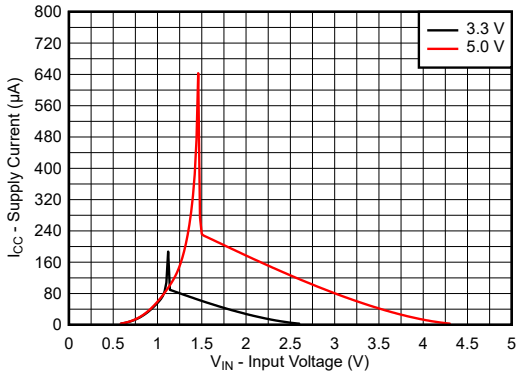


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

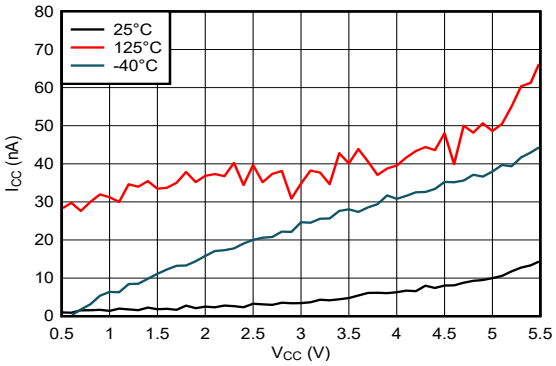


Figure 5-3. Supply Current Across Supply Voltage

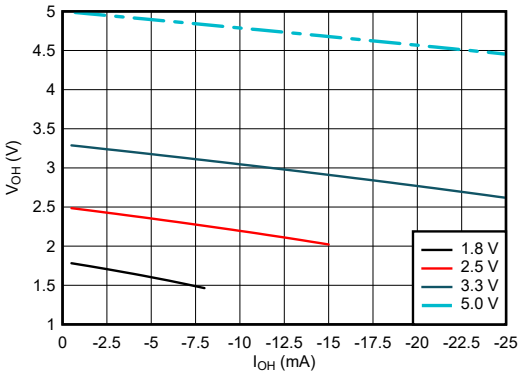


Figure 5-4. Output Voltage vs Current in HIGH State

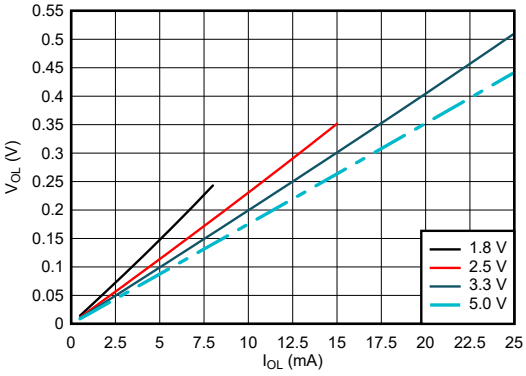


Figure 5-5. Output Voltage vs Current in LOW State

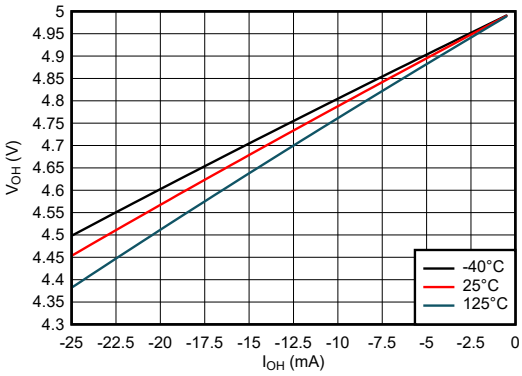


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

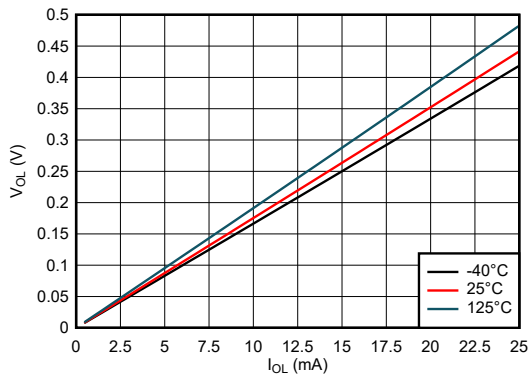


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

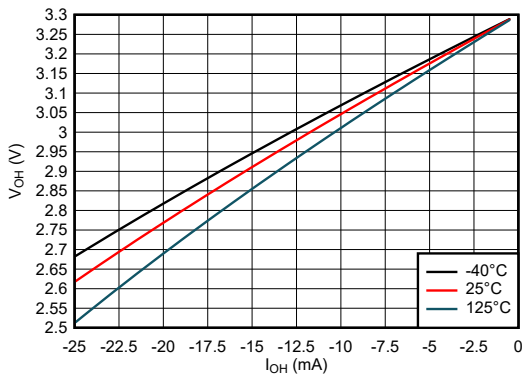


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

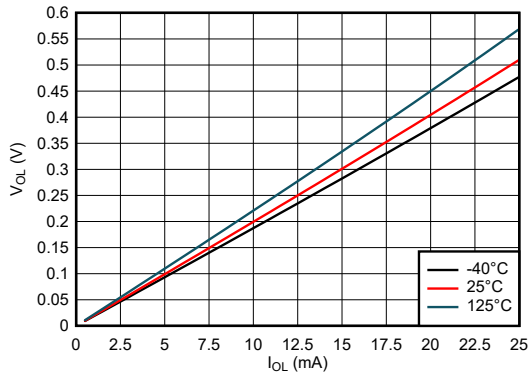


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

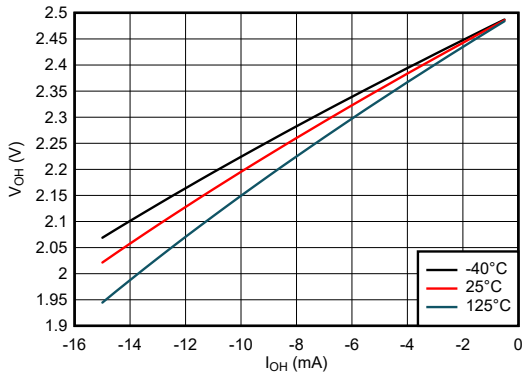


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

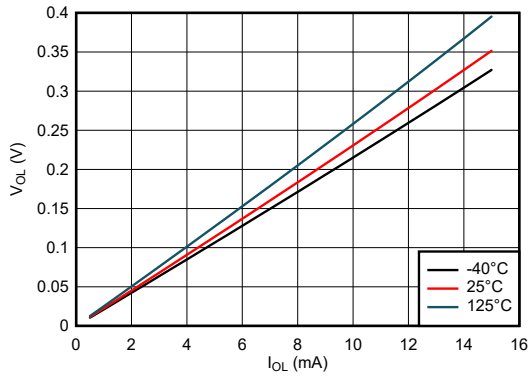


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

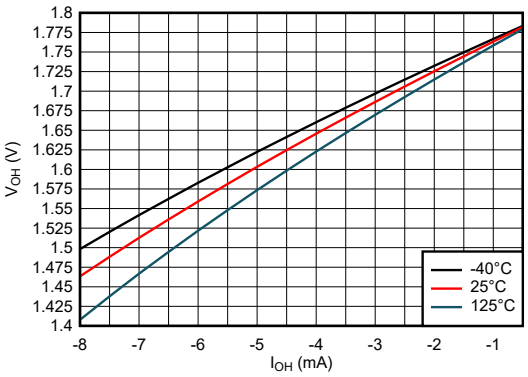


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

ADVANCE INFORMATION

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

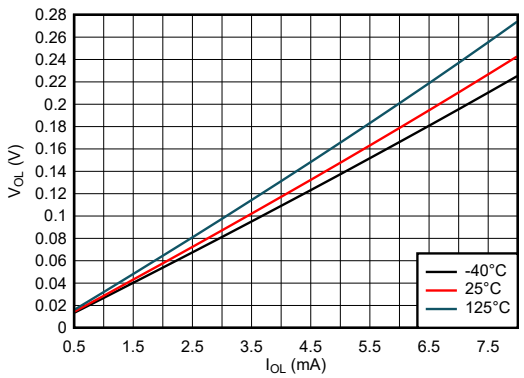


Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

ADVANCE INFORMATION

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

The outputs are measured individually with one input transition per measurement.

Table 6-1. 3-State Outputs

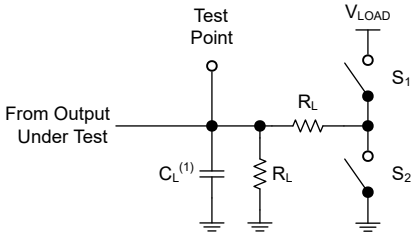
TEST	S1	S2	R_L	C_L	ΔV	V_{LOAD}
t_{PLH}, t_{PHL}	OPEN	OPEN	500Ω	50pF	—	—
t_{PLZ}, t_{PZL}	CLOSED	OPEN	500Ω	50pF	0.3V	2×V_{CC}
t_{PHZ}, t_{PZH}	OPEN	CLOSED	500Ω	50pF	0.3V	—

Table 6-2. 3-State or Open-Drain Outputs

V_{CC}	V_t	R_L	C_L	ΔV	V_{LOAD}
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V	2×V_{CC}
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V	2×V_{CC}
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V	2×V_{CC}
2.7V	1.5V	500Ω	50pF	0.3V	6V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V	6V

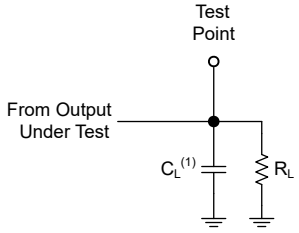
Table 6-3. Push-Pull Outputs

V_{CC}	V_t	R_L	C_L	ΔV
1.2V ± 0.1V	V_{CC}/2	2kΩ	15pF	0.1V
1.5V ± 0.12V	V_{CC}/2	2kΩ	15pF	0.1V
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



(1) C_L includes probe and test-fixture capacitance.

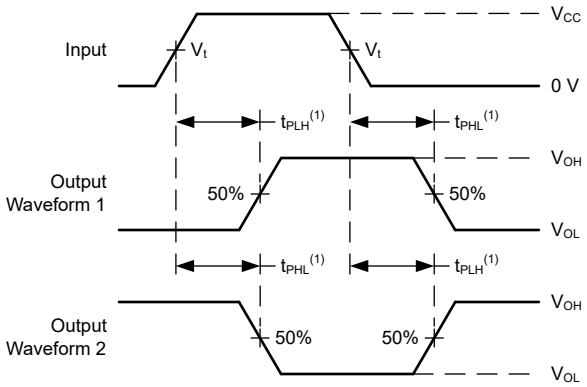
Figure 6-1. Load Circuit for 3-State Outputs



(1) C_L includes probe and test-fixture capacitance.

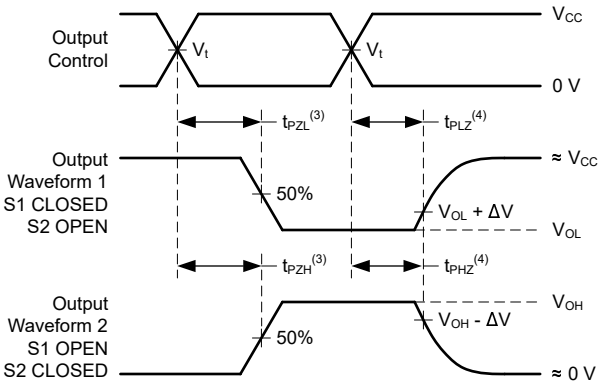
Figure 6-2. Load Circuit for Push-Pull Outputs

ADVANCE INFORMATION



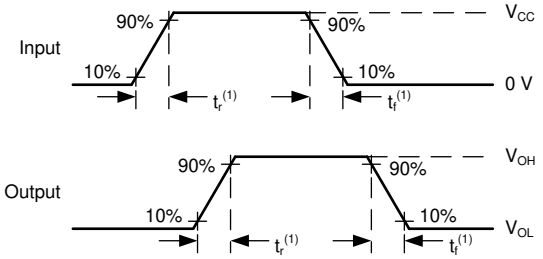
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.
(2) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-5. Voltage Waveforms, Input and Output Transition Times

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

Figure 7-1 describes the SN74LVC595A, an 8-bit shift register that feeds an 8-bit D-type storage register. Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register. Outputs Q_A through Q_H are controlled by the output enable ($\overline{OE}$) input. The serial output $Q_{H'}$ is always active.

7.2 Functional Block Diagram

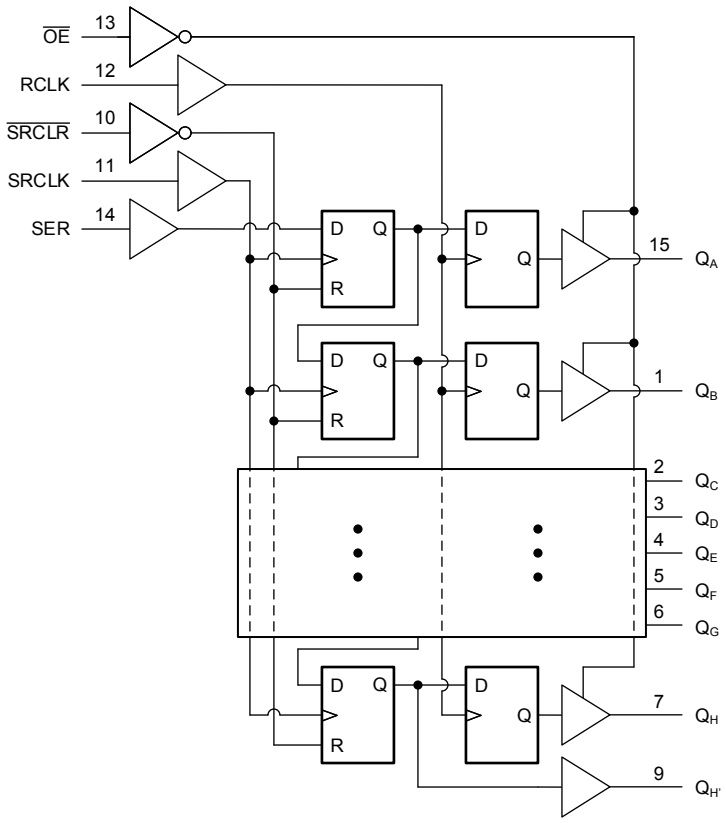


Figure 7-1. Logic Diagram (Positive Logic) for the SN74LVC595A

ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.4 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

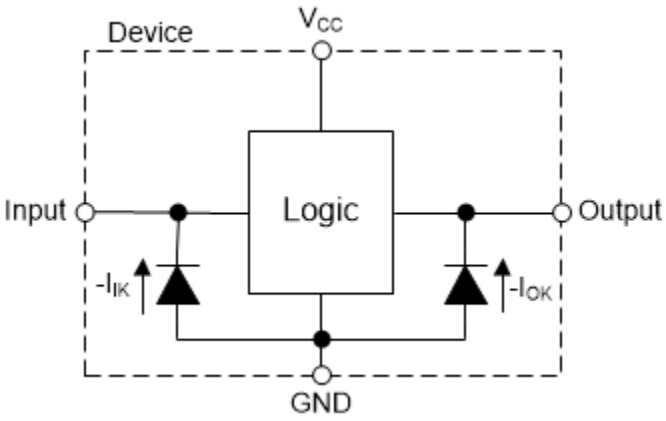


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Function Table lists the functional modes of the SN74LVC595A.

Table 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{OE}}$	
X	X	X	X	H	Outputs Q_A – Q_H are disabled
X	X	X	X	L	Outputs Q_A – Q_H are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	H	↑	X	Shift-register data is stored in the storage register.
X	↑	H	↑	X	Data in shift register is stored in the storage register, the data is then shifted through.

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74LVC595A is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen to four. Unlike other I/O expanders, the SN74LVC595A does not need a communication interface for control. It can be easily operated with simple GPIO pins.

The $\overline{OE}$ pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74LVC595A can be controlled accordingly to turn off all the outputs reducing the I/O needed to three. There is no practical limitation to how many SN74LVC595A devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register. As shown in the Typical Application Block Diagram, an RC circuit can be connected to the $\overline{SRCLR}$ pin to initialize the shift register to all zeros. With the $\overline{OE}$ pin pulled up with a resistor, this process can be performed while the outputs are in a high-impedance state eliminating any erroneous data causing issues with the displays.

8.2 Typical Application

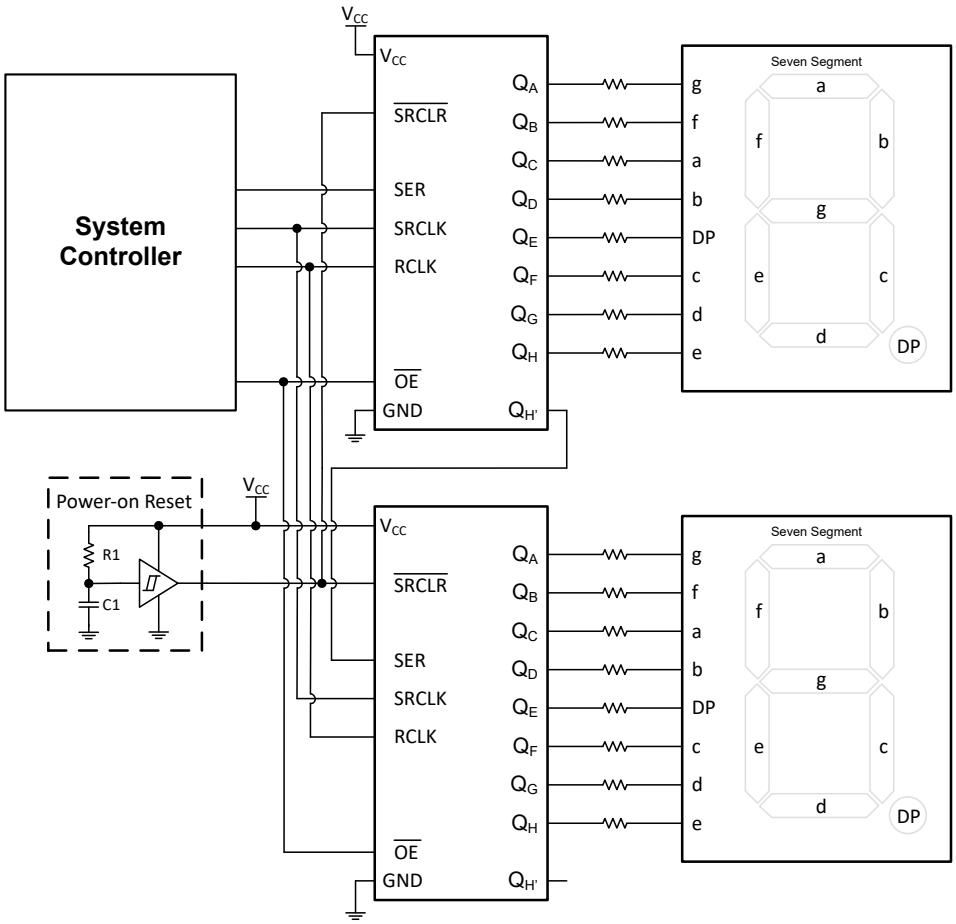


Figure 8-1. Typical Application Block Diagram

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8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC595A plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC595A plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC595A can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC595A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC595A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC595A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC595A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

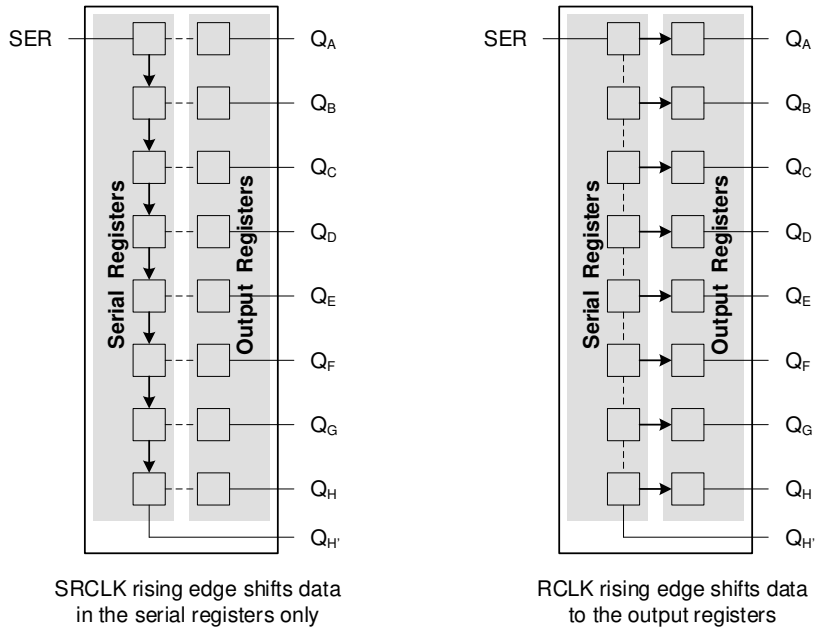


Figure 8-2. Simplified Functional Diagram Showing Clock Operation

ADVANCE INFORMATION

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

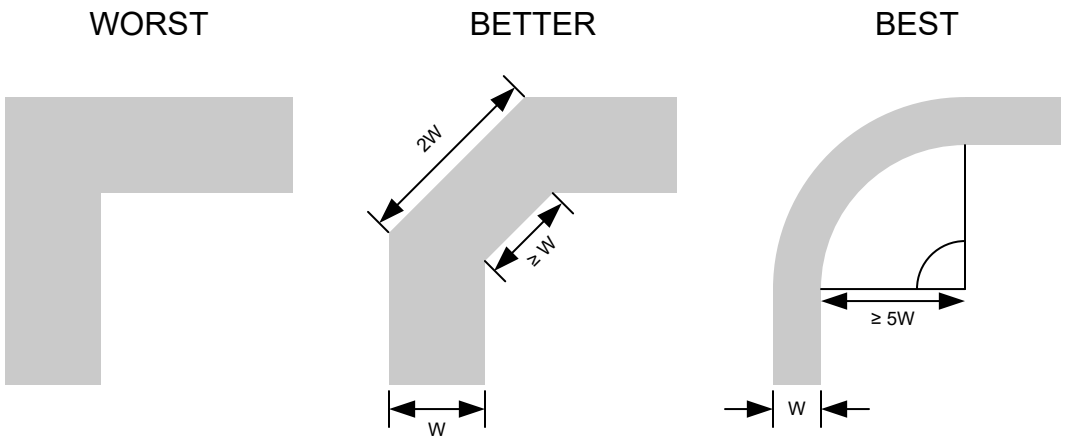


Figure 8-3. Example Trace Corners for Improved Signal Integrity

ADVANCE INFORMATION

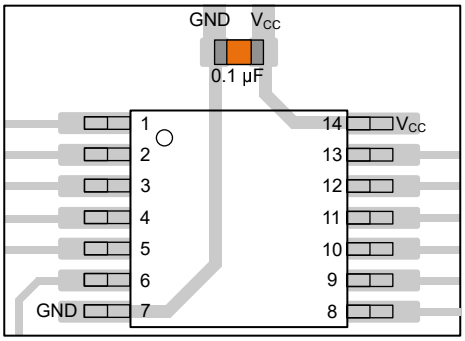


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

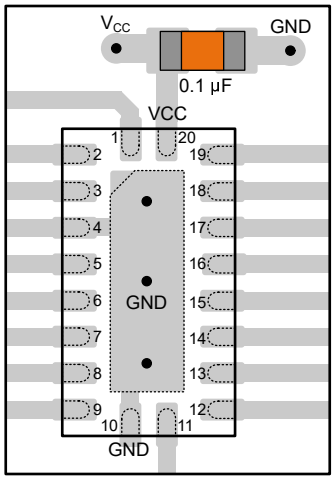


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

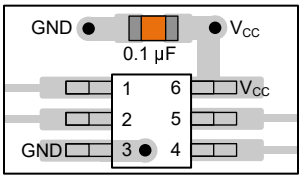


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

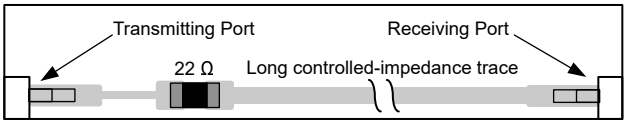


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Advance Information Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

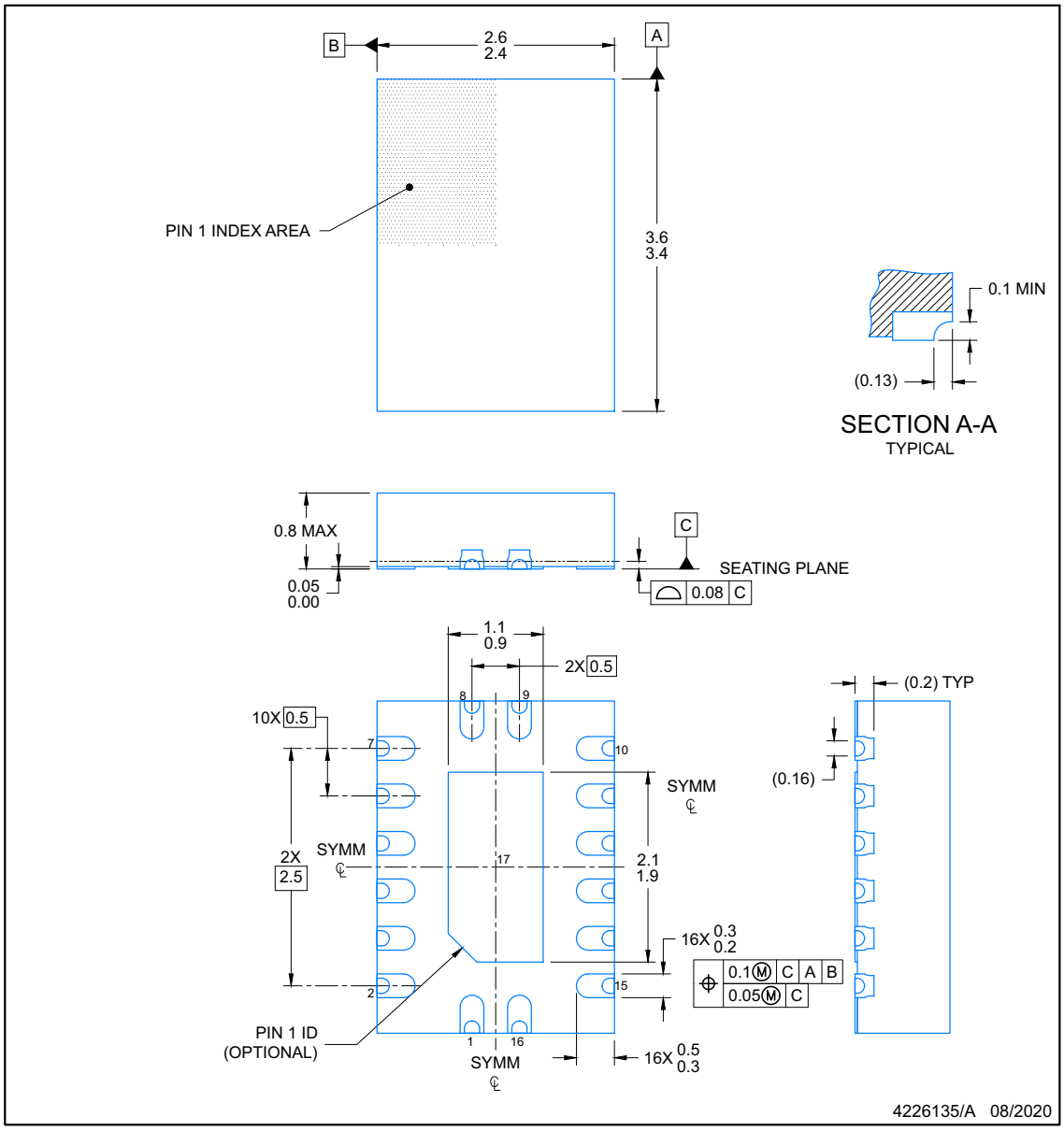
ADVANCE INFORMATION

11.1 Mechanical Data

PACKAGE OUTLINE

BQB0016B — **WQFN - 0.8 mm max height**

INDSTNAME



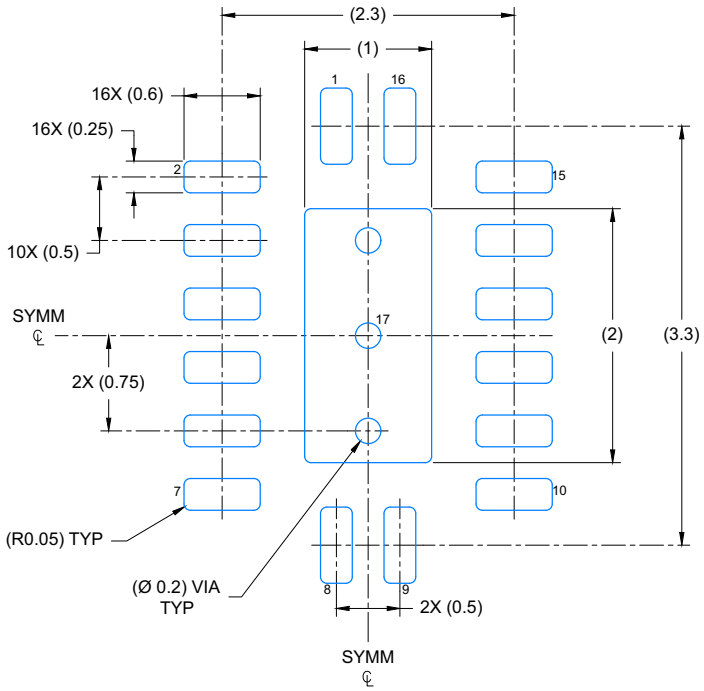
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQB0016B — **WQFN - 0.8 mm max height**

INDSTNAME



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

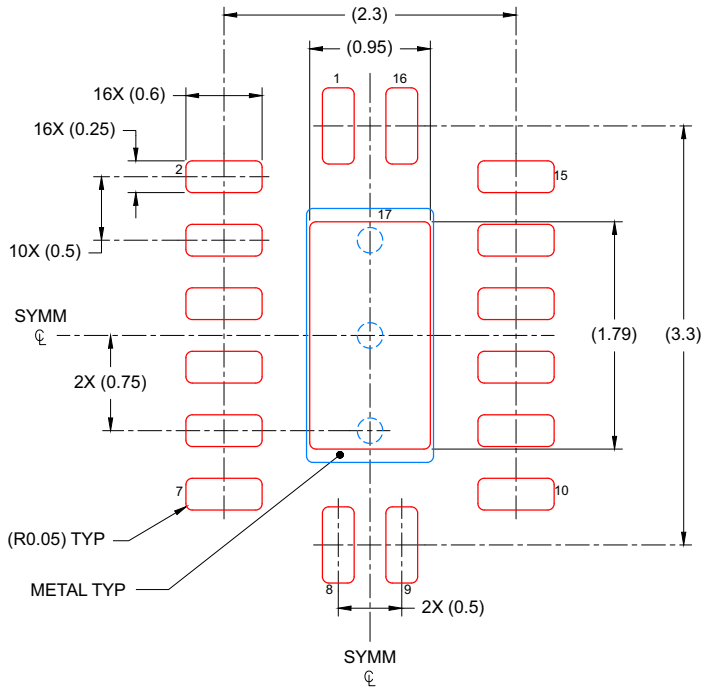
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

BQB0016B — **WQFN - 0.8 mm max height**

INDSTNAME



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

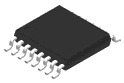
EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

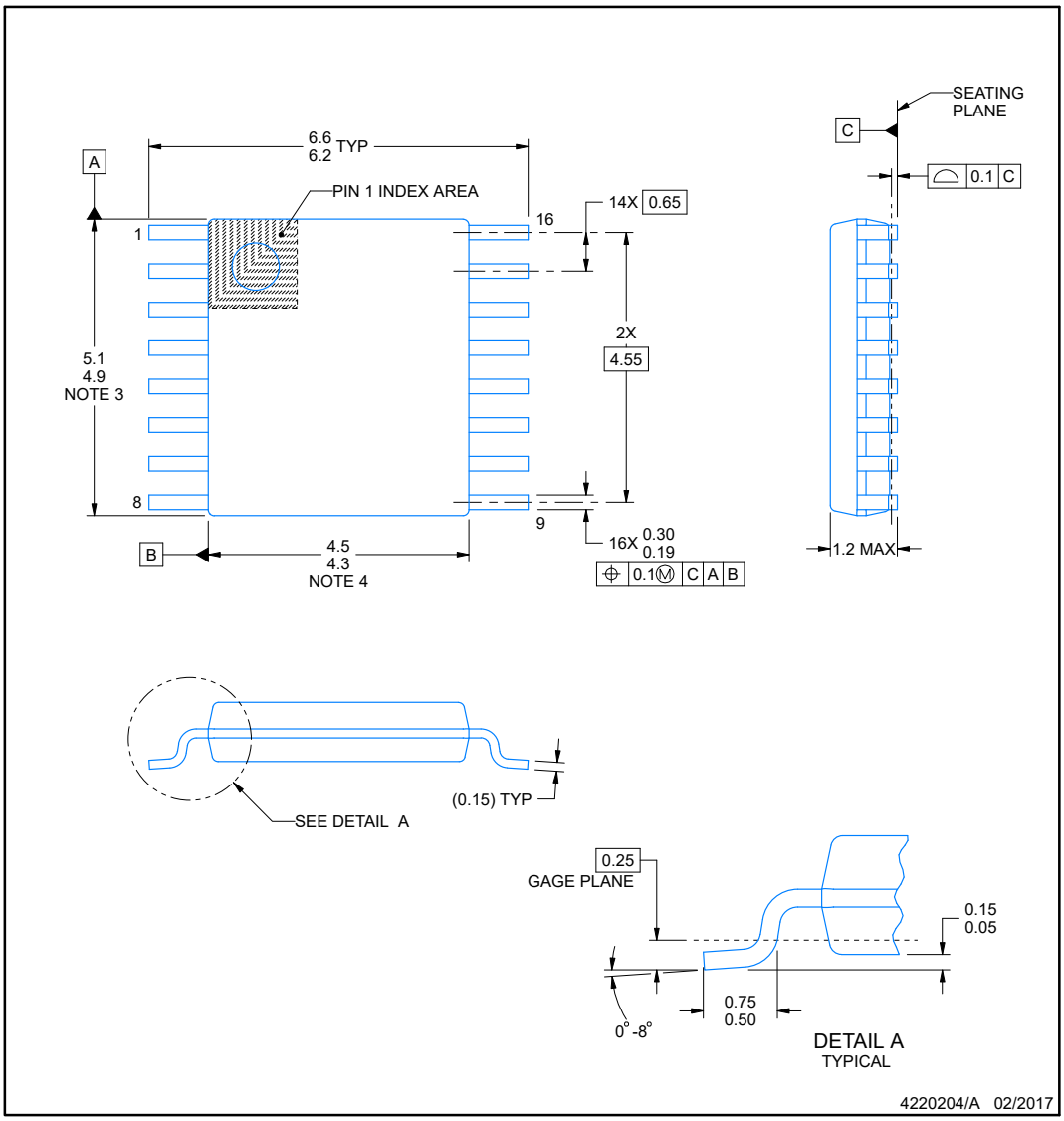
PACKAGE OUTLINE



PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

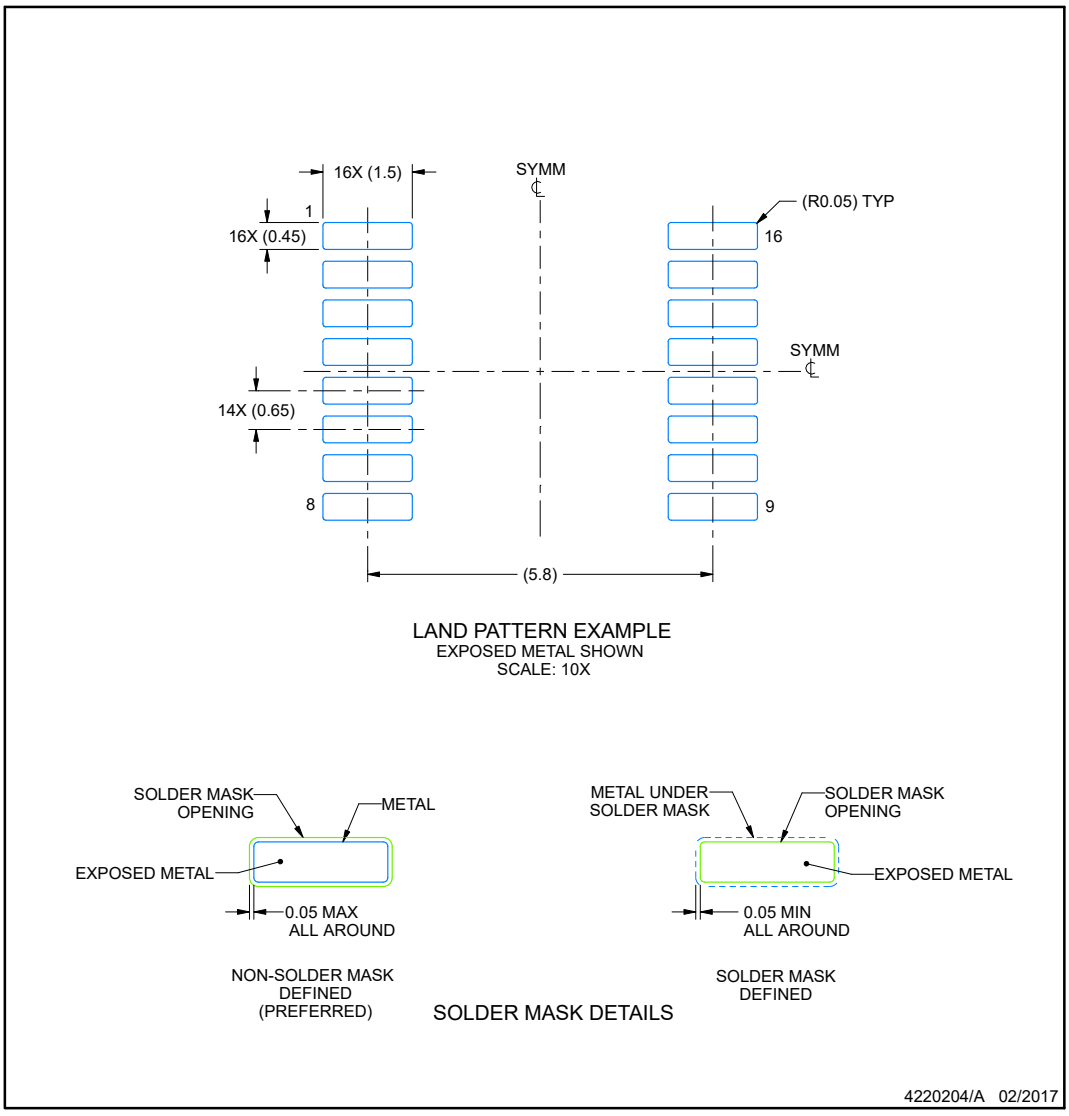
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

PW0016A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



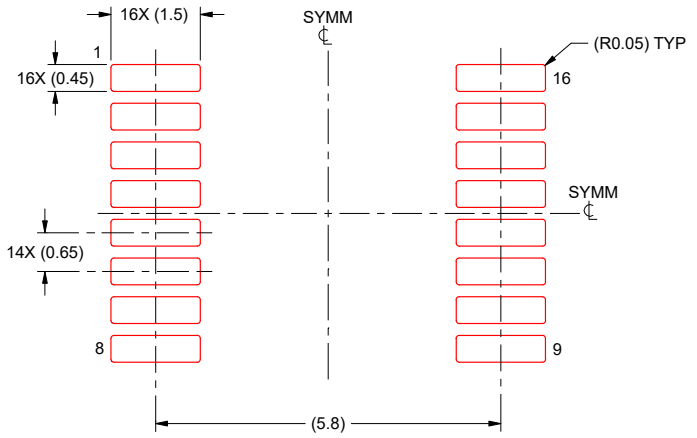
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A — **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN74LVC595ABQBR	Active	Preproduction	WQFN (BQB) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-	
PSN74LVC595APWR	Active	Preproduction	TSSOP (PW) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74LVC595A :

- Automotive : SN74LVC595A-Q1

NOTE: Qualified Version Definitions:

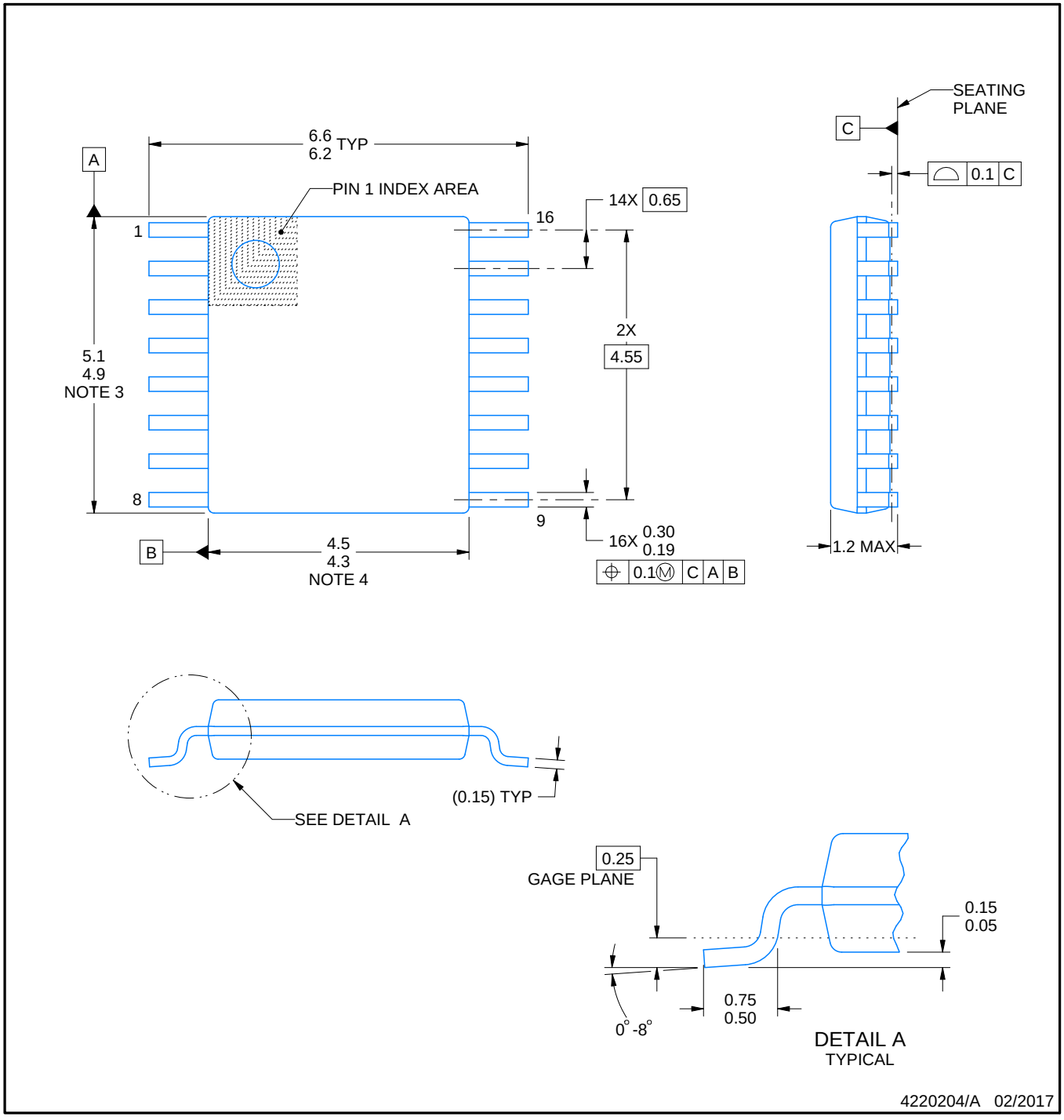
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

PW0016A

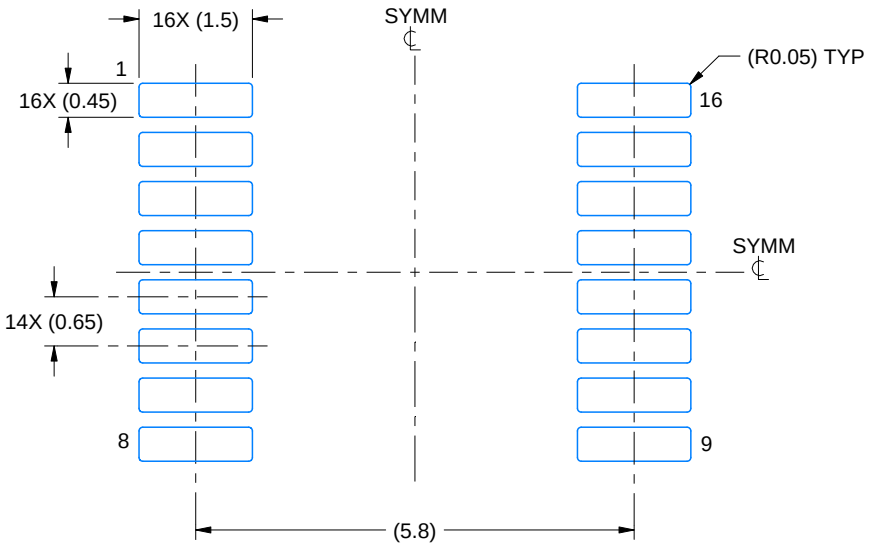
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

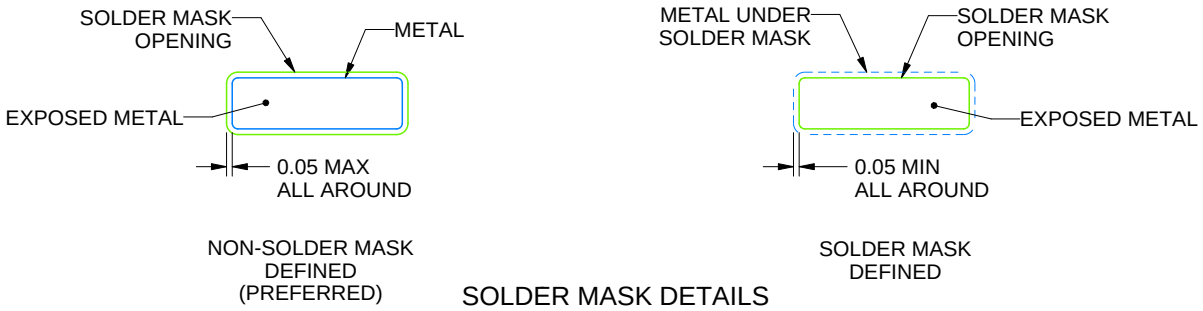


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

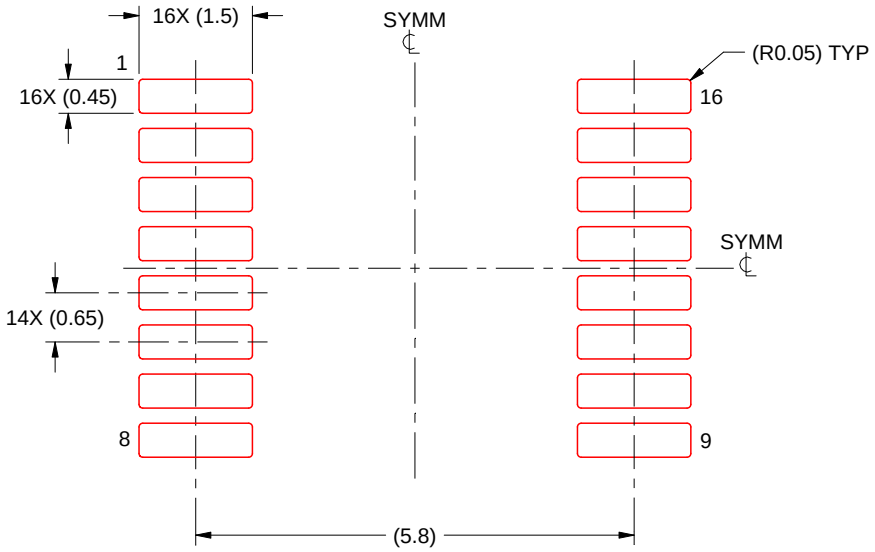


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

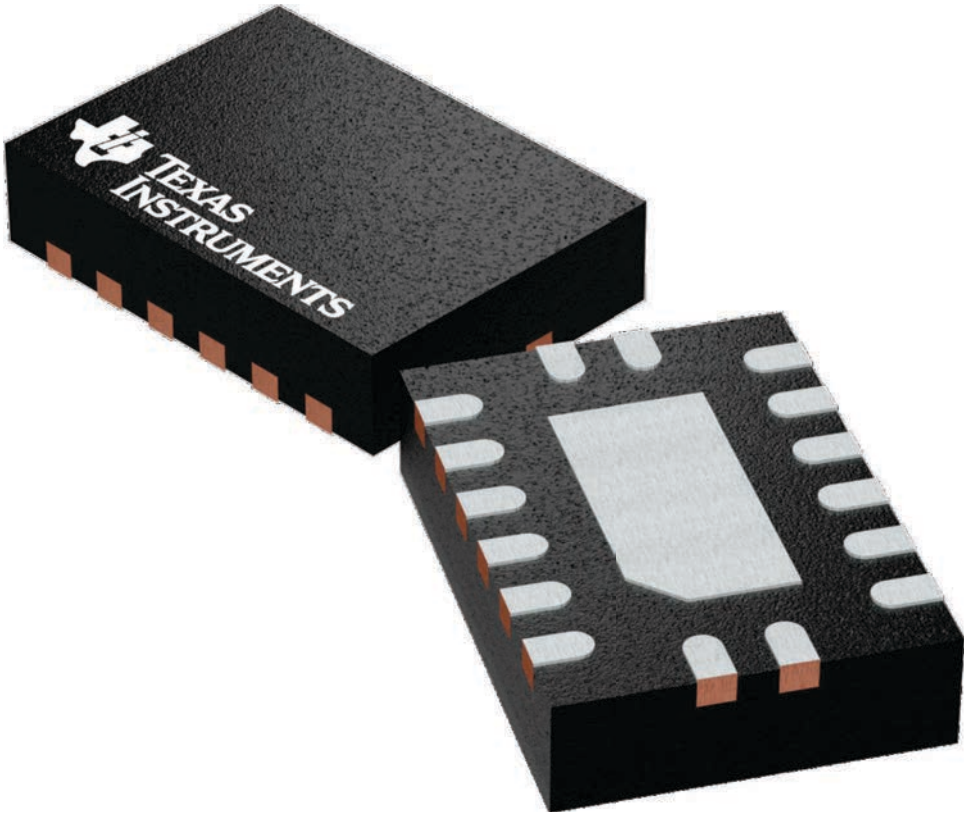
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226161/A

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