SN74CB3T3245 8-Bit FET Bus Switch 2.5V and 3.3V Low-Voltage With 5V-Tolerant Level Shifter

1 Features

- Standard '245-type pinout
- Output voltage translation tracks V_{CC}
- Supports mixed-mode signal operation on all data I/O ports
  - 5V Input down to 3.3V output level shift with 3.3V V_{CC}
  - 5V/3.3V input down to 2.5V output level shift with 2.5V V_{CC}
- 5V-tolerant I/Os with device powered up or powered down
- Bidirectional data flow with near-zero propagation delay
- Low ON-state resistance (r_{on}) characteristics (r_{on} = 5Ω typical)
- Low Input, output capacitance minimizes loading ($C_{io(OFF)}$ = 5pF typical)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption (I_{CC} = 40µA maximum)
- V_{CC} operating range from 2.3V to 3.6V
- Data I/Os support 0 to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control inputs can be driven by TTL or 5V/3.3V CMOS outputs
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250mA per JESD 17
- ESD performance tested per JESD 22
  - 2000V human-body model (A114-B, Class II)
  - 1000V charged-device model (C101)
- Designed for low-power portable equipment

2 Applications

- Supports digital applications:
  - Level translation
  - PCI interface
  - USB interface
  - Memory interleaving
  - Bus isolation

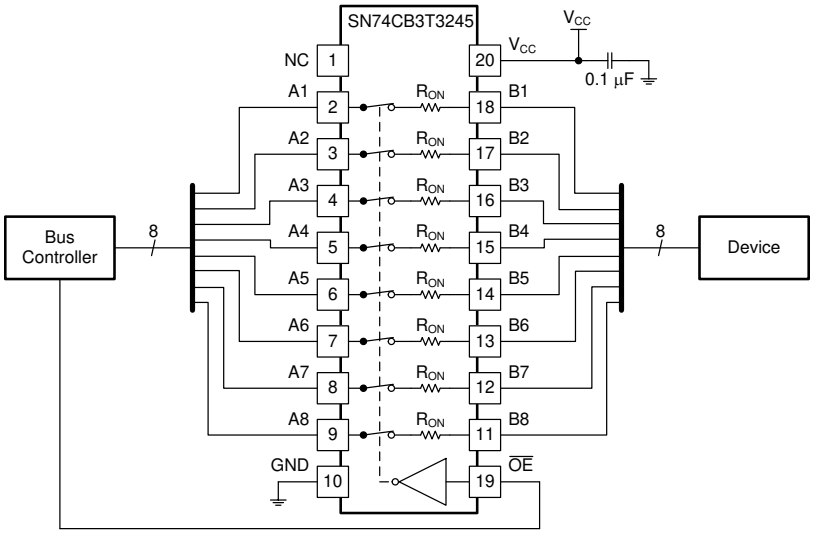
3 Description

The SN74CB3T3245 device is a high-speed, TTL-compatible, 8-bit FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
SN74CB3T3245DBQ	DBQ (SSOP, 20)	8.65mm × 6mm
SN74CB3T3245DGV	DGV (TVSOP, 20)	5.00mm × 6.4mm
SN74CB3T3245DW	DW (SOIC, 20)	12.8mm × 10.3mm
SN74CB3T3245PW	PW (TSSOP, 20)	6.5mm × 6.4mm
SN74CB3T3245DGS	DGS (VSSOP, 20)	5.10mm × 4.9mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Functional Diagram

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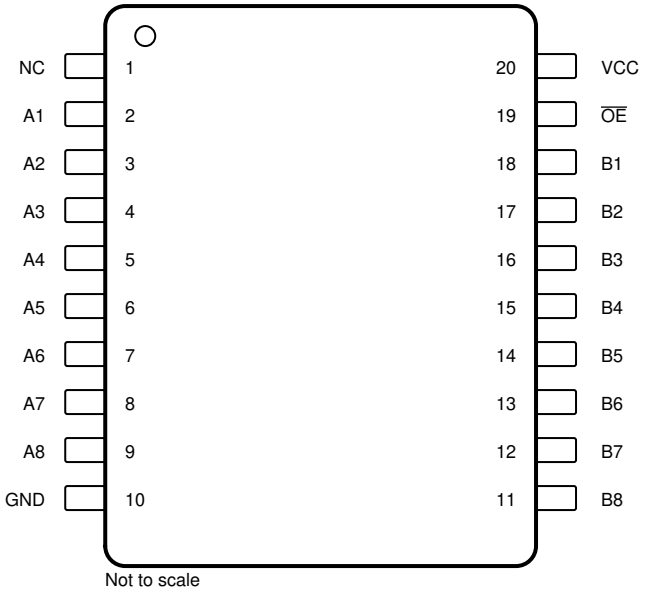
4 Pin Configuration and Functions



NC — No internal connection

Figure 4-1. DGS, DBQ, DGV, DW, and PW Package 20-Pin VSSOP, SSOP, TVSOP, SOIC, TSSOP Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NC	—	Not internally connected
2	A1	I/O	Switch 1 A terminal
3	A2	I/O	Switch 2 A terminal
4	A3	I/O	Switch 3 A terminal
5	A4	I/O	Switch 4 A terminal
6	A5	I/O	Switch 5 A terminal
7	A6	I/O	Switch 6 A terminal
8	A7	I/O	Switch 7 A terminal
9	A8	I/O	Switch 8 A terminal
10	GND	—	Ground
11	B8	I/O	Switch 8 B terminal
12	B7	I/O	Switch 7 B terminal
13	B6	I/O	Switch 6 B terminal
14	B5	I/O	Switch 5 B terminal
15	B4	I/O	Switch 4 B terminal
16	B3	I/O	Switch 3 B terminal
17	B2	I/O	Switch 2 B terminal
18	B1	I/O	Switch 1 B terminal
19	$\overline{OE}$	I	Output enable, active low
20	V_{CC}	—	Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	7	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7	5.5	V
		V_{CC} = 2.7V to 3.6V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.7	V
		V_{CC} = 2.7V to 3.6V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

5.4 Thermal Information

THERMAL METRIC[1]		SN74CB3T3245					UNIT
		DGS(VSSOP)	DBQ (SSOP)	DGV(TVSOP)	DW(SOIC)	PW(TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127	102.4	123.7	58	112.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = –18 mA				–1.2	V
V_{OH}		See and Figure 5-1					
I_{IN}	Control inputs	V_{CC} = 3.6 V, V_{IN} = 3.6 V to 5.5 V or GND				±10	µA
I_I		V_{CC} = 3.6 V, Switch ON, V_{IN} = V_{CC} or GND	V_I = V_{CC} – 0.7 V to 5.5 V			±20	µA
			V_I = 0.7 V to V_{CC} – 0.7 V			–40	
			V_I = 0 to 0.7 V			±5	
I_{OZ} (3)		V_{CC} = 3.6 V, V_O = 0 to 5.5 V, V_I = 0, Switch OFF, V_{IN} = V_{CC} or GND				±10	µA
I_{off}		V_{CC} = 0, V_O = 0 to 5.5 V, V_I = 0,				10	µA
I_{CC}		V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF, V_{IN} = V_{CC} or GND	V_I = V_{CC} or GND			40	µA
			V_I = 5.5 V			40	
ΔI_{CC} (4)	Control inputs	V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				300	µA
C_{in}	Control inputs	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND			4		pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, $V_{I/O}$ = 5.5 V, 3.3 V, or GND, Switch OFF, V_{IN} = V_{CC} or GND			5		pF
$C_{io(ON)}$		V_{CC} = 3.3 V, Switch ON, V_{IN} = V_{CC} or GND	$V_{I/O}$ = 5.5 V or 3.3 V		5		pF
			$V_{I/O}$ = GND		13		
r_{on} (5)		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V, V_I = 0	I_O = 24 mA		5	8.5	Ω
			I_O = 16 mA		5	8.5	
		V_{CC} = 3 V, V_I = 0	I_O = 64 mA		5	7	
			I_O = 32 mA		5	7	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

5.6 Switching Characteristics 85C

over operating free-air temperature range (unless otherwise noted)

Parameter with Test conditions		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd}	R_L = 1GΩ, C_L = 30pF, V_{load} = 0V. Calculated Tpd with switch resistance*CL	A or B	B or A	2.5 V ± 0.2 V			0.15	ns
t_{pd}	R_L = 1GΩ, C_L = 50pF, V_{load} = 0V. Calculated Tpd with switch resistance*CL	A or B	B or A	3.3 V ± 0.3 V			0.25	ns
t_{en}	ZL: R_L = 250Ω, C_L = 30pF, V_{load} = VCC, ZH: RL = 500Ω, CL = 30pF, Vload = GND, 50ohm termination at input	OE	A or B	2.5 V ± 0.2 V			11.7	ns
t_{en}	ZL: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC} ZH: RL = 500Ω, CL = 50pF, Vload = GND, 50ohm termination at input	OE	A or B	3.3 V ± 0.3 V			8	ns
t_{dis}	LZ: R_L = 250Ω, C_L = 30pF, V_{load} = V_{CC}, Vt = 0.15V; HZ: RL = 500Ω, CL = 30pF, Vload = GND, Vt = 0.15V; 50ohm termination at input	OE	A or B	2.5 V ± 0.2 V	1		8	ns

5.6 Switching Characteristics 85C (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter with Test conditions		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{dis}	LZ: R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, Vt = 0.3V; HZ: RL = 500Ω, CL = 50pF, Vload = GND, Vt = 0.3V; 50ohm termination at input	OE	A or B	3.3 V ± 0.3 V	1		8.8	ns

5.7 Typical Characteristics

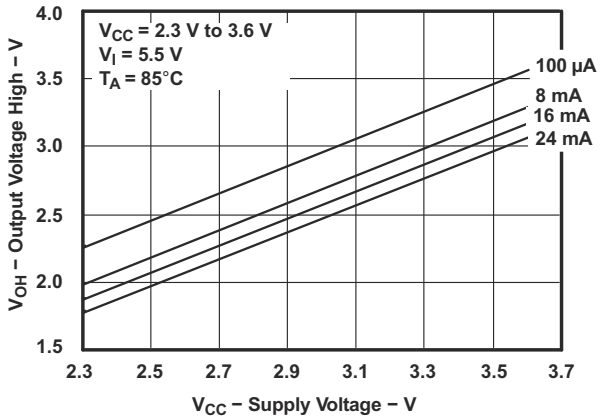


Figure 5-1. V_{OH} vs V_{CC}

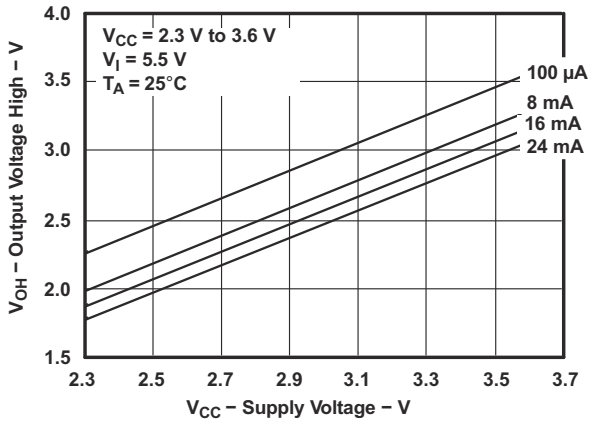


Figure 5-2. V_{OH} vs V_{CC}

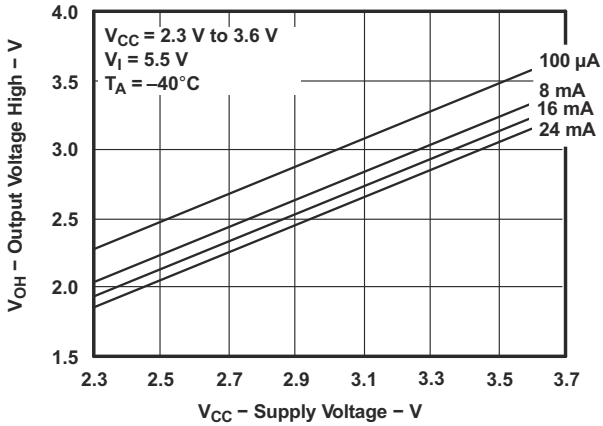
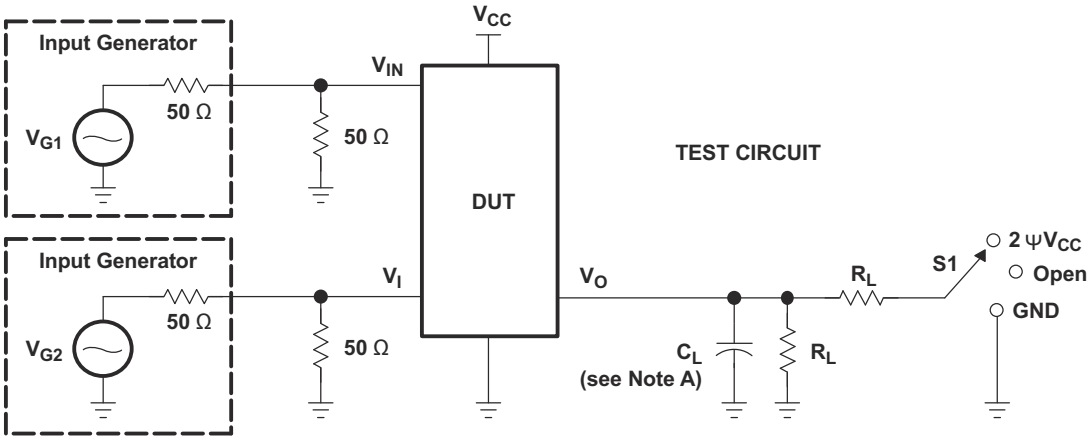
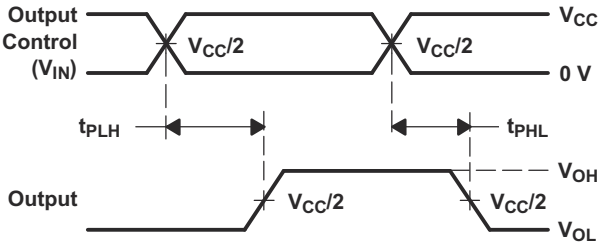


Figure 5-3. V_{OH} vs V_{CC}

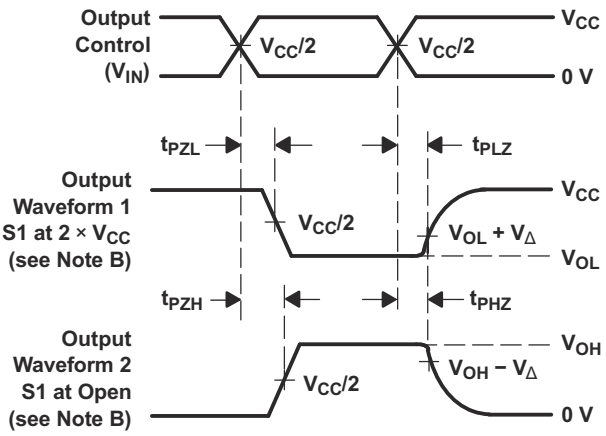
6 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V or GND 5.5 V or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	3.6 V 5.5 V	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

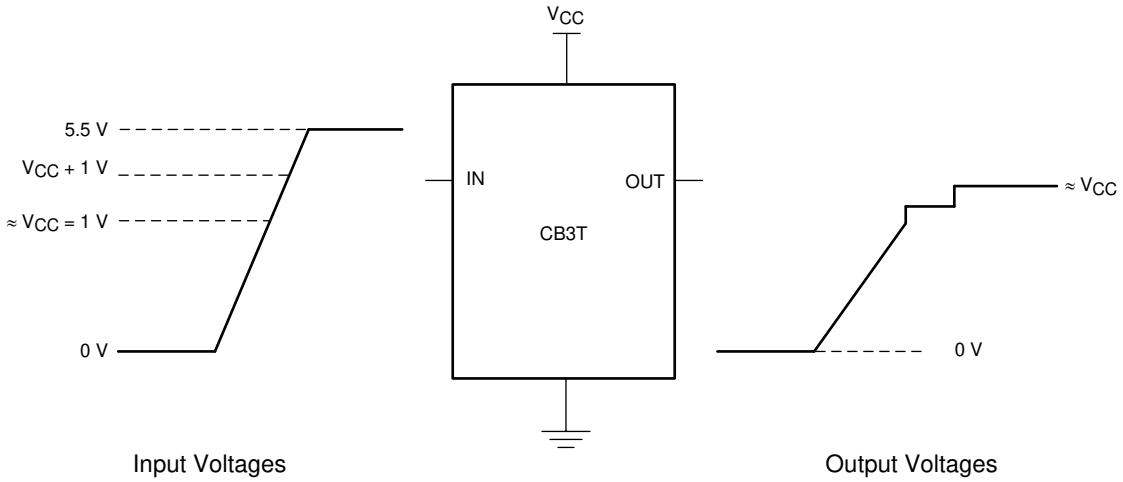
The SN74CB3T3245 device is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. The device fully supports mixed-mode signal operation on all data I/O ports by providing voltage translation that tracks V_{CC}. The SN74CB3T3245 device supports systems using 5-V TTL, 3.3-V LVTTL, and 2.5-V CMOS switching standards, as well as user-defined switching levels (see Figure 7-1).

The SN74CB3T3245 device is an 8-bit bus switch with a single output-enable ($\overline{OE}$) input and a standard '245 pinout. When $\overline{OE}$ is low, the 8-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the 8-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature certifies that damaging current does not backflow through the device when the device is powered down. The device has isolation during power off.

To establish the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



If the input high voltage (V_{IH}) level is greater than or equal to V_{CC} + 1V, and less than or equal to 5.5V, the output high voltage (V_{OH}) level is equal to approximately the V_{CC} voltage level.

Figure 7-1. Typical DC Voltage Translation Characteristics

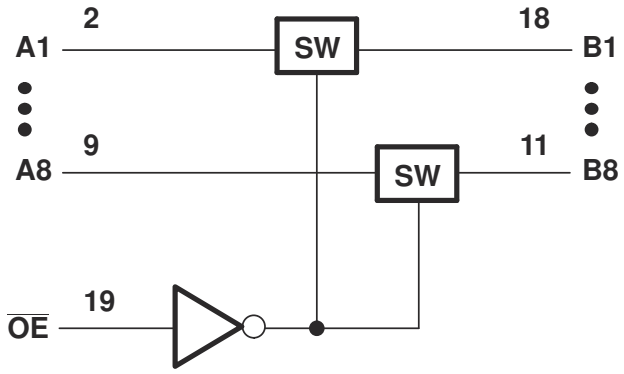
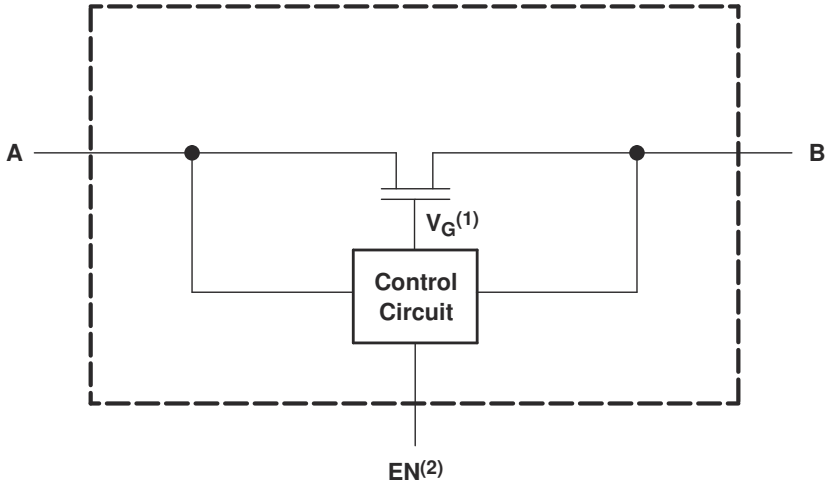


Figure 7-2. Logic Diagram (Positive Logic)



1) Gate Voltage (V_G) is approximately equal to $V_{CC} + V_T$ when the switch is ON and $V_I > (V_{CC} + V_T)$.
2) EN is the internal enable signal applied to the switch.

Figure 7-3. Simplified Schematic, Each FET Switch (SW)

7.3 Feature Description

The SN74CB3T3245 device uses the standard '245-type pinout. The output voltage tracks V_{CC}, allowing for easy down-translation. The device is prime for low-power portable equipment.

Mixed-mode signal operation is supported on all data I/O ports. 5V input down to 3.3V output level shift with 3.3V V_{CC} and 5V/3.3V input down to 2.5V output level shift With 2.5V V_{CC} are possible due to overvoltage tolerant inputs.

This part is friendly to partial power down systems. The I/Os are 5V-tolerant with the device powered up or powered down and I_{off} supports partial-power-down mode operation.

The SN74CB3T3245 has a bidirectional data flow with near-zero propagation delay.

The SN74CB3T3245 has low ON-state resistance (r_{on}) characteristics (r_{on} = 5Ω typical).

The SN74CB3T3245 has both low input and output capacitance minimizes loading ($C_{io(OFF)}$ = 5pF typical).

Data and control inputs provide undershoot clamp diodes.

The SN74CB3T3245 has low power consumption (I_{CC} = 40µA Maximum).

The SN74CB3T3245 has a V_{CC} operating range from 2.3V to 3.6V.

The data I/Os support 0V to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V).

Control inputs can be driven by TTL or 5V/3.3V CMOS outputs.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74CB3T3245.

Table 7-1. Function Table

INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

This application is specifically to connect a 5V bus to a 3.3V device. Assume that communication in this particular application is one-directional, going from the bus controller to the device.

8.2 Typical Application

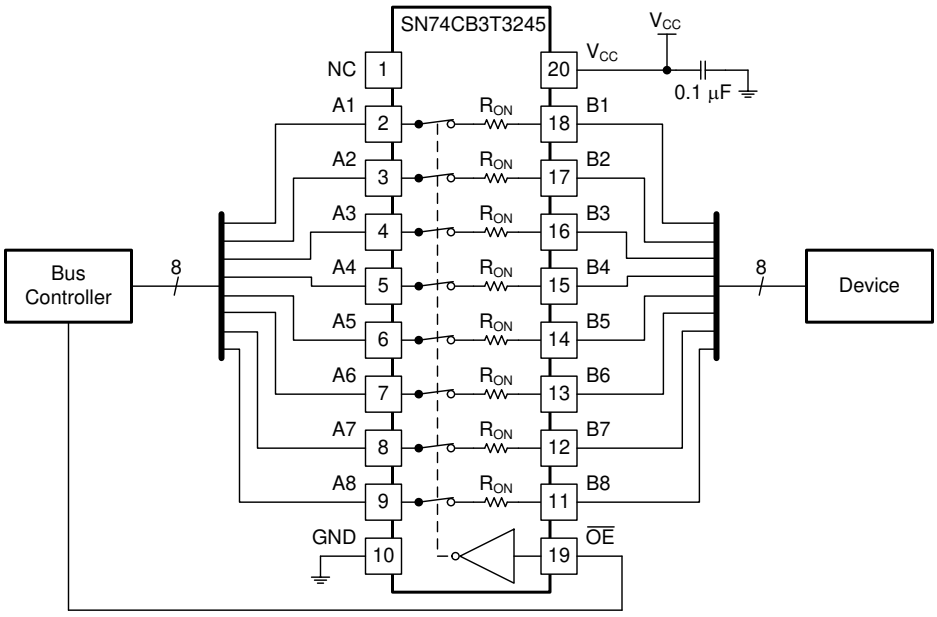


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because bus contention can drive currents that can exceed maximum limits.

Because this design is for down-translating voltage, no pullup resistors are required.

8.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant allowing them to go as high as 7V at any valid V_{CC}.
2. Recommend output conditions
   - Load currents must not exceed 128mA on each channel.

8.2.3 Application Curves

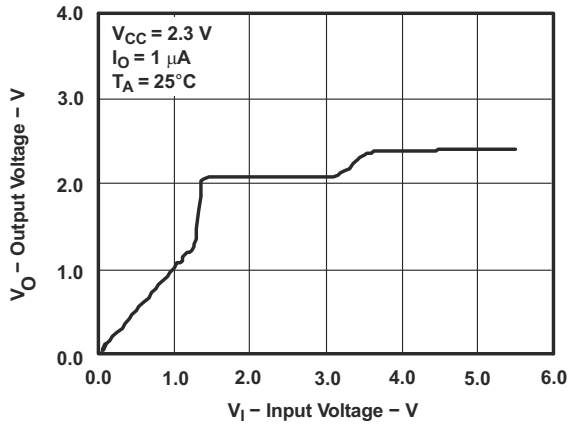


Figure 8-2. Data Output Voltage vs Data Input Voltage

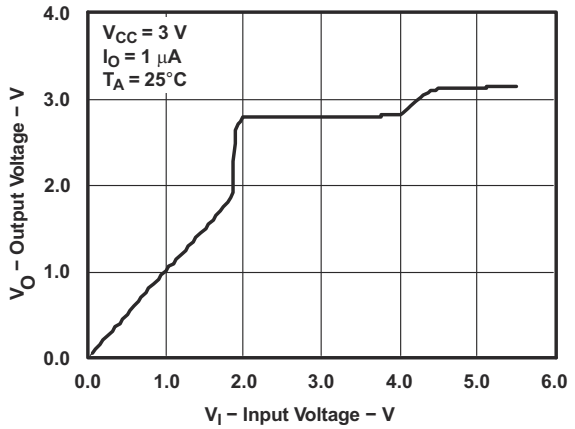


Figure 8-3. Data Output Voltage vs Data Input Voltage

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1μF bypass capacitor. If there are multiple pins labeled V_{CC}, then TI recommends a 0.01μF or 0.022μF capacitor for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1μF bypass capacitor is recommended for each supply pin. Paralleling multiple bypass capacitors to reject different frequencies of noise is acceptable. 0.1μF and 1μF capacitors are commonly used in parallel. For best results, install the bypass capacitor as close to the power terminal.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

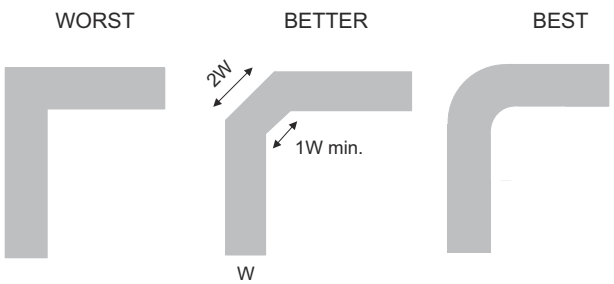


Figure 8-4. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2018) to Revision D (May 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the DGS package throughout the document	1
• Updated specs in the *Switching Characteristics* table	4
• Added the latest information and new package to the *Thermal Information* table	4

Changes from Revision B (June 2015) to Revision C (May 2018)	Page
• Changed the pin out image appearance	3
• Changed I_O = 1mA To: I_O = 1µA in Figure 8-2 and Figure 8-3	12

Changes from Revision A (August 2012) to Revision B (June 2015)	Page
• Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power*	

Supply Recommendations section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Removed *Ordering Information* table..... 1

Changes from Revision * (March 2005) to Revision A (August 2012) **Page**

- Updated graphic note and picture in Figure 1..... 9

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3T3245DBQR	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245
SN74CB3T3245DBQR.A	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245
SN74CB3T3245DBQR.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245
SN74CB3T3245DBQRG4	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245
SN74CB3T3245DBQRG4.A	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245
SN74CB3T3245DBQRG4.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CB3T3245
SN74CB3T3245DGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245DGVR.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245DGVR.B	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245DGVRG4	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245DGVRG4.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245DGVRG4.B	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245
SN74CB3T3245DW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245
SN74CB3T3245DWG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245
SN74CB3T3245DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245
SN74CB3T3245DWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3T3245
SN74CB3T3245PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	KS245
SN74CB3T3245PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245PWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245PWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245
SN74CB3T3245PWRG4.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	KS245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

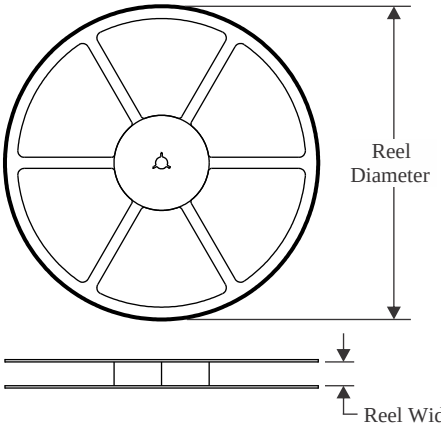
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

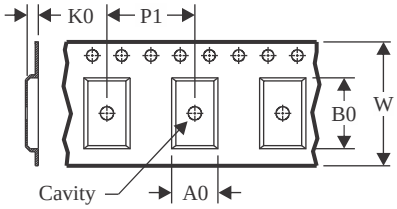
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

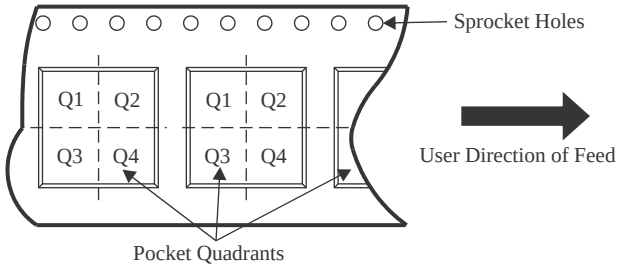


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

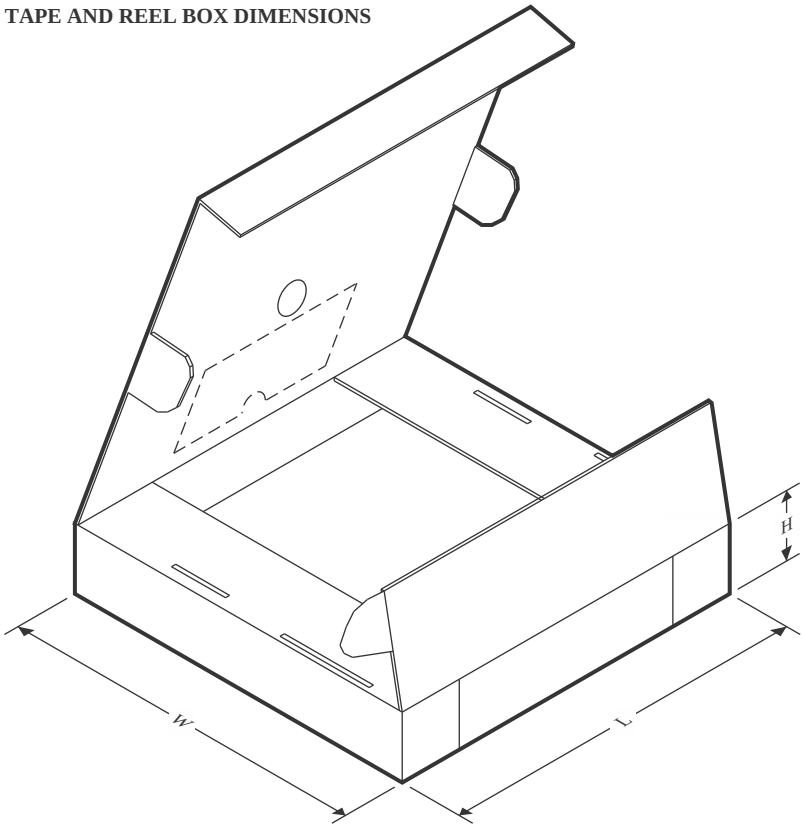
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3245DBQRG4	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3245DGVRG4	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3T3245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74CB3T3245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74CB3T3245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

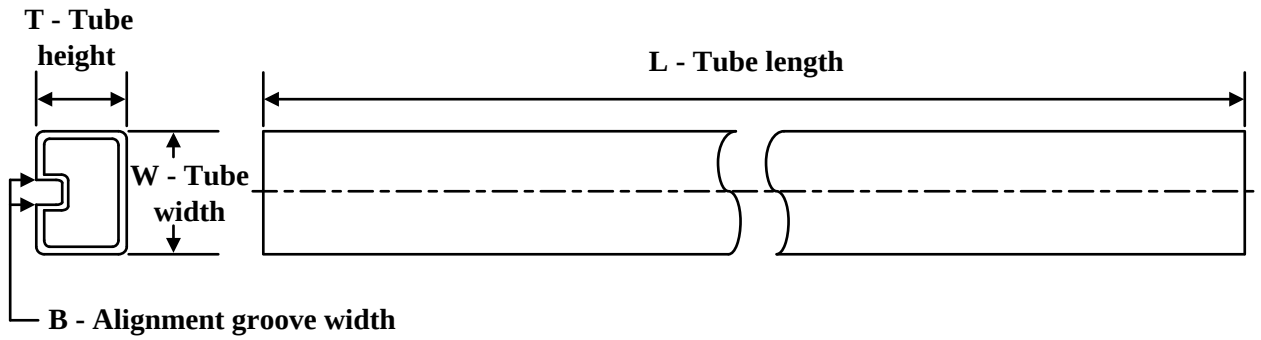
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3T3245DBQR	SSOP	DBQ	20	2500	356.0	356.0	35.0
SN74CB3T3245DBQRG4	SSOP	DBQ	20	2500	356.0	356.0	35.0
SN74CB3T3245DGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CB3T3245DGVRG4	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74CB3T3245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74CB3T3245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74CB3T3245PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0

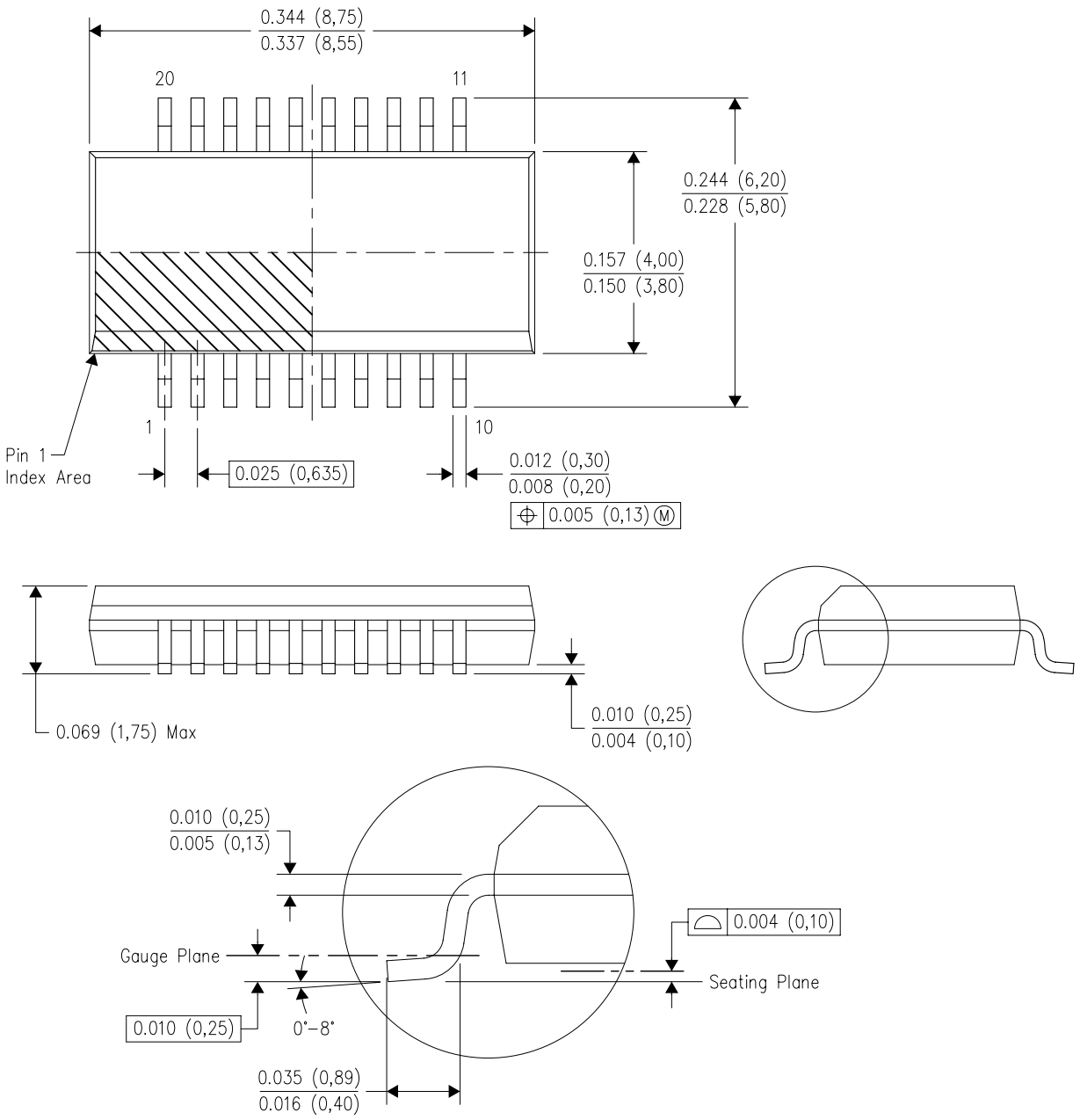
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74CB3T3245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CB3T3245DW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74CB3T3245DWG4	DW	SOIC	20	25	507	12.83	5080	6.6

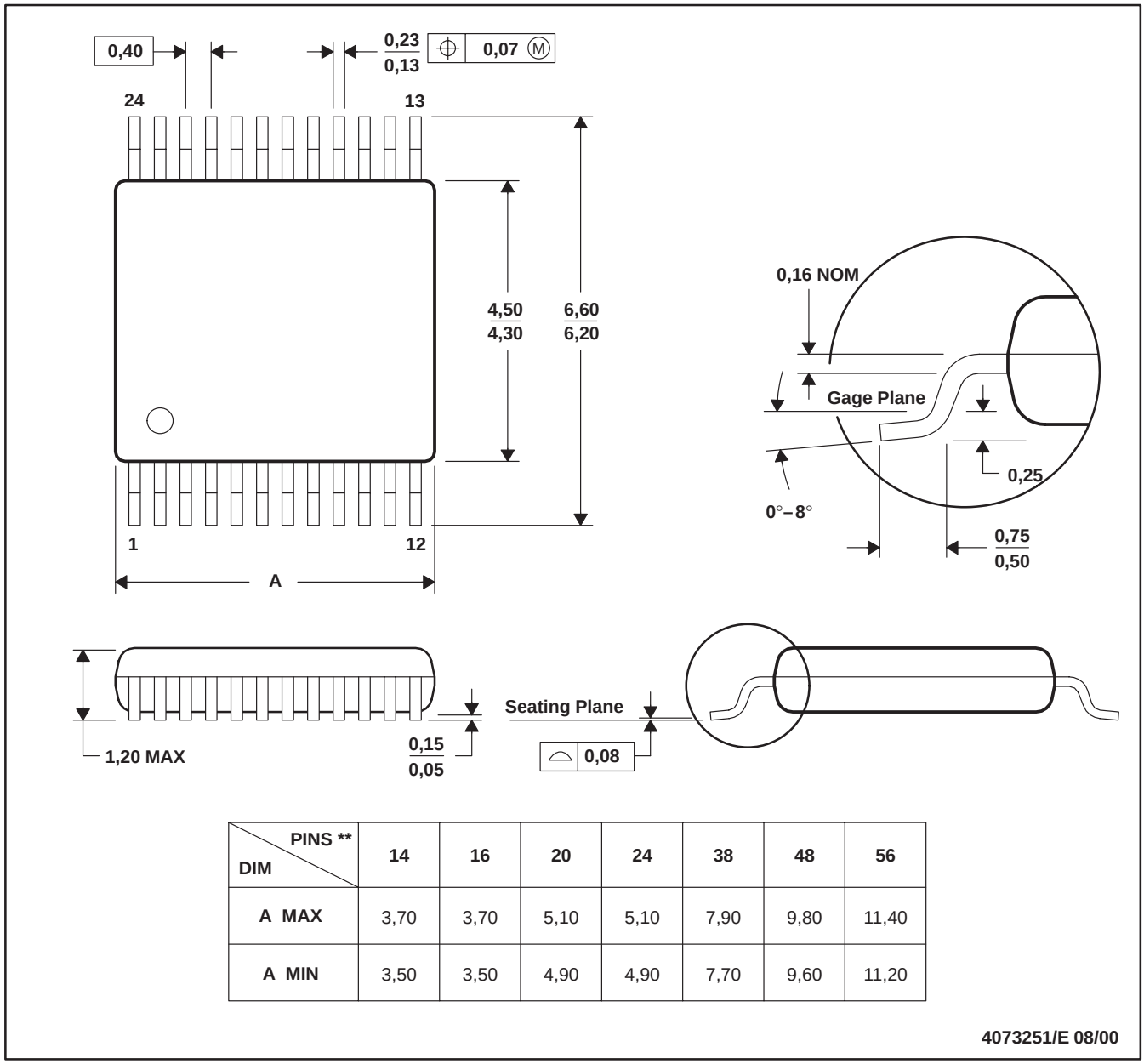
DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

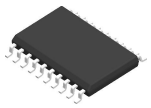
24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

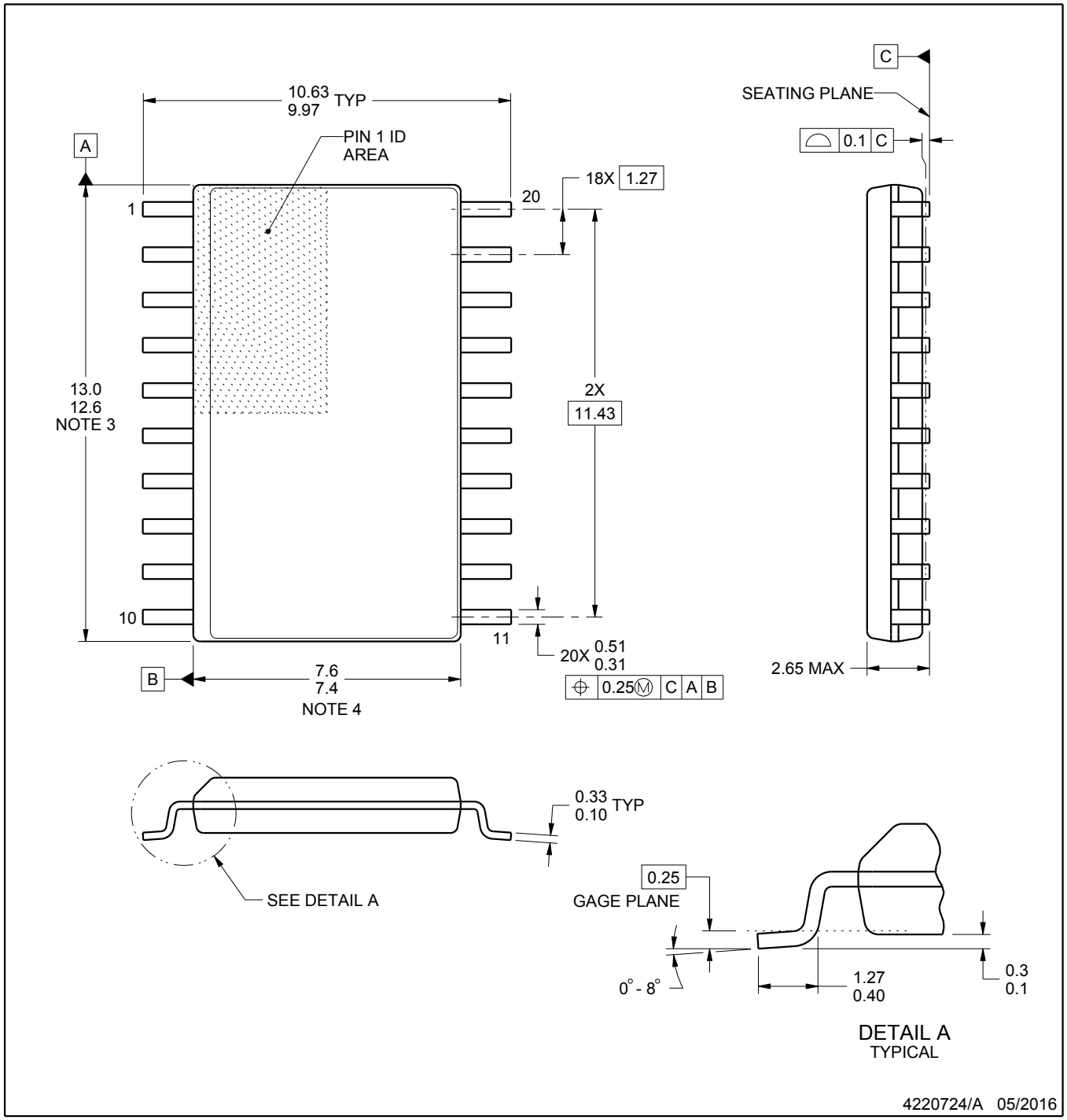


PACKAGE OUTLINE

DW0020A

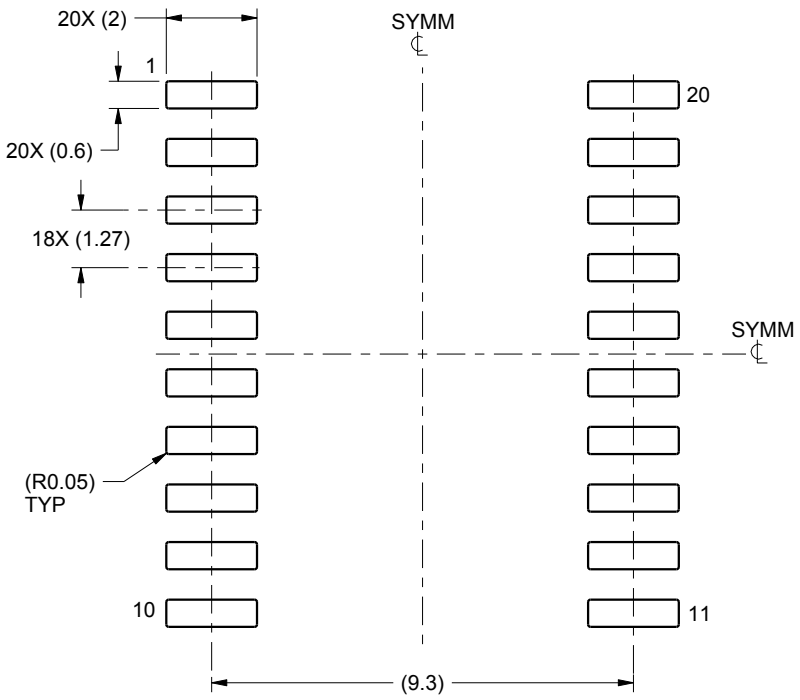
SOIC - 2.65 mm max height

SOIC

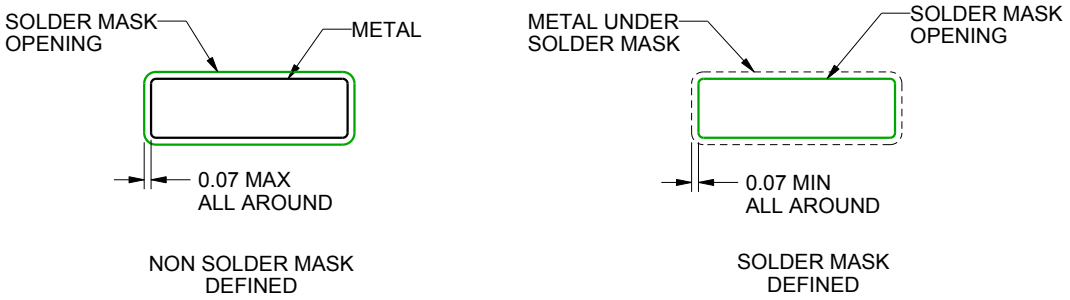


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

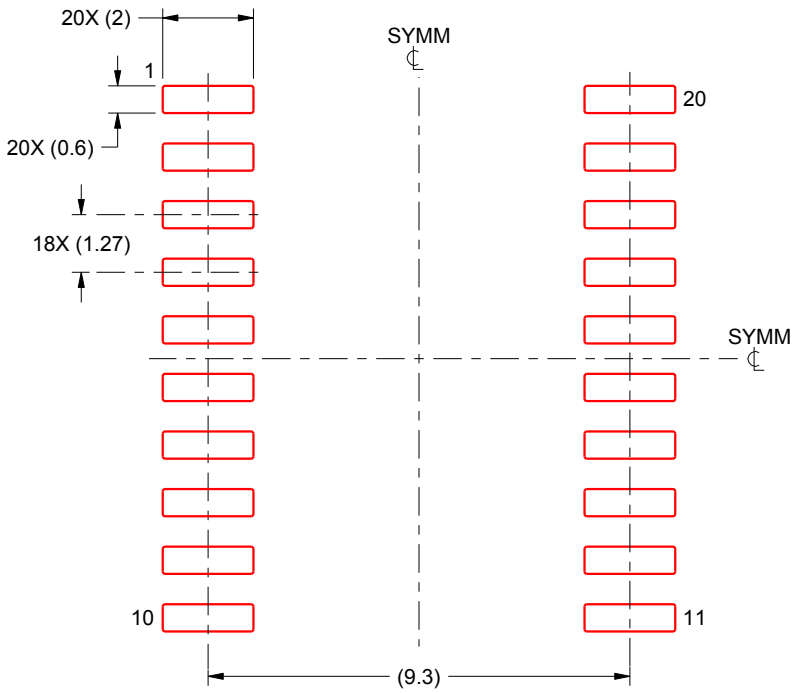


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

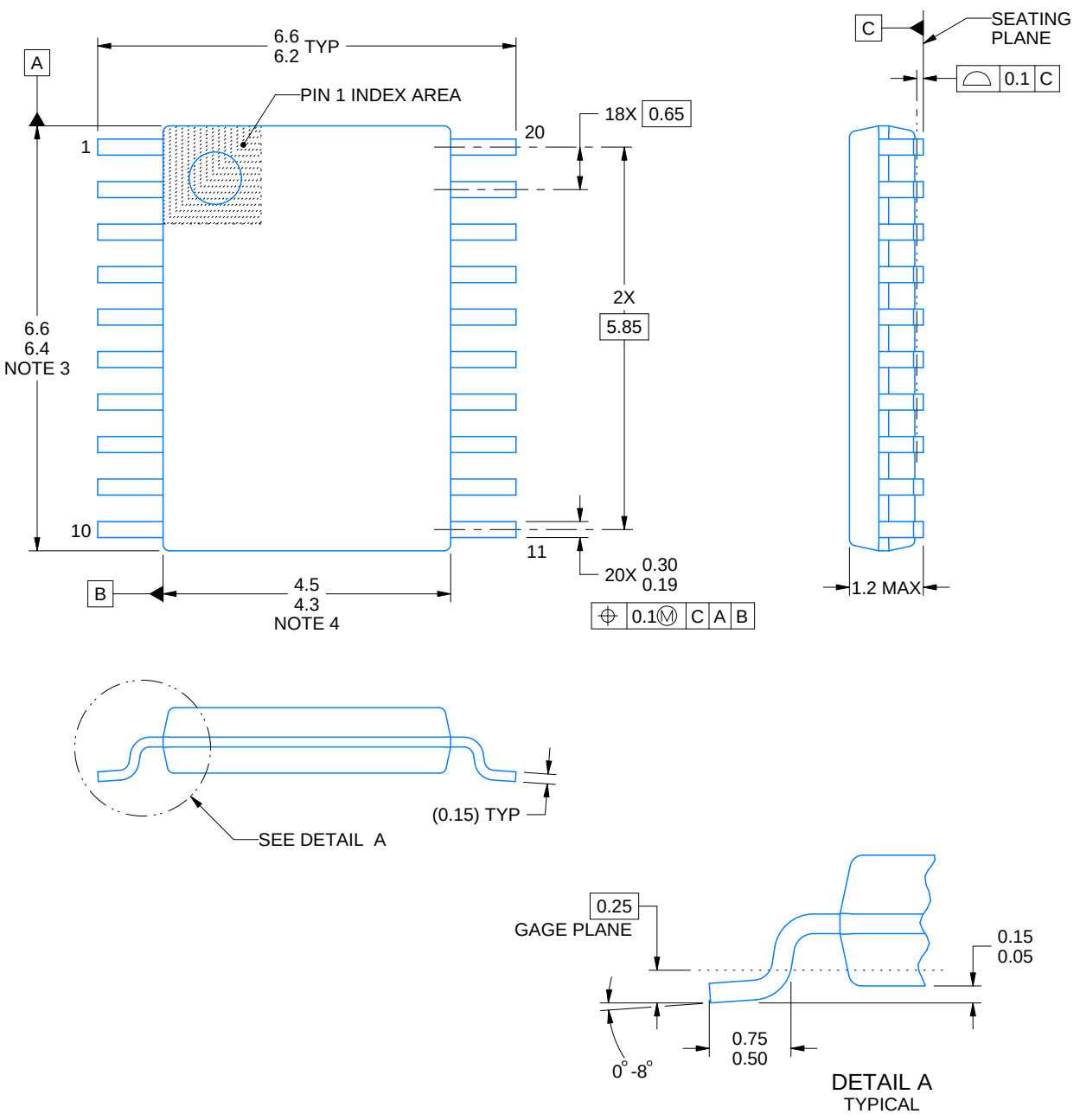
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

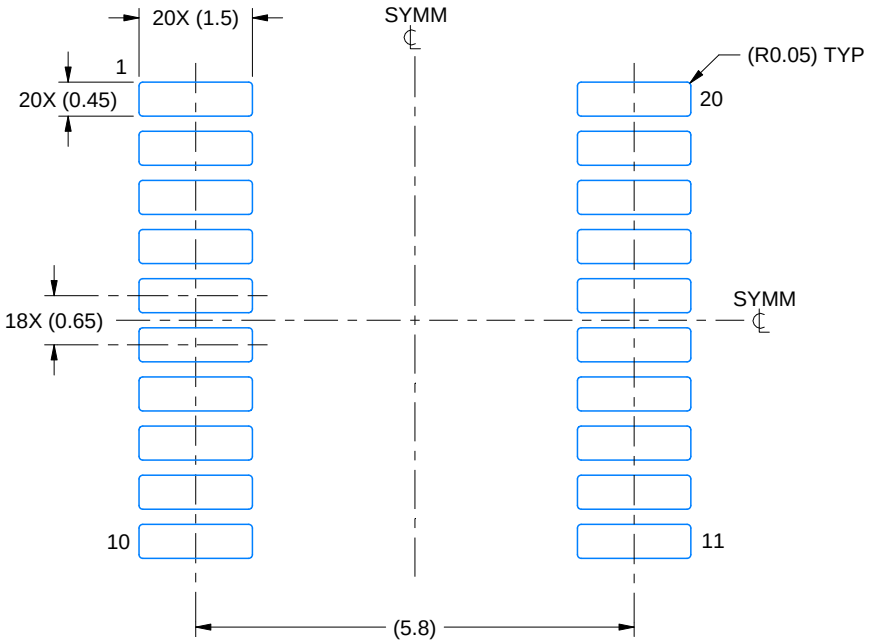
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



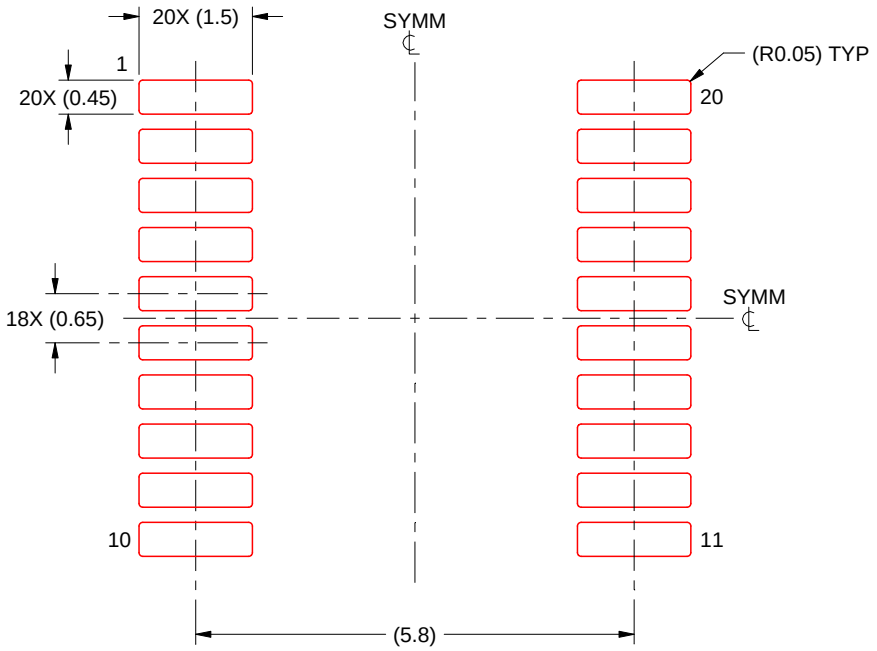
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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