

TIBPAL 16L8-15C, TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

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- **High-Performance Operation:**
Propagation Delay
C Suffix . . . 15 ns Max
M Suffix . . . 20 ns Max
- **Functionally Equivalent, but Faster Than**
PAL16L8A, PAL16R4A, PAL16R6A, and
PAL16R8A
- **Power-Up Clear on Registered Devices (All**
Register Outputs Are Set High, but Voltage
Levels at the Output Pins Go Low)
- **Package Options Include Both Plastic and**
Ceramic Chip Carriers in Addition to
Plastic and Ceramic DIPs
- **Dependable Texas Instruments Quality and**
Reliability

| DEVICE | I INPUTS | 3-STATE O OUTPUTS | REGISTERED Q OUTPUTS | I/O PORTS |
|---------|-------------|-------------------------|----------------------------|--------------|
| PAL16L8 | 10 | 2 | 0 | 6 |
| PAL16R4 | 8 | 0 | 4 (3-state buffers) | 4 |
| PAL16R6 | 8 | 0 | 6 (3-state buffers) | 2 |
| PAL16R8 | 8 | 0 | 8 (3-state buffers) | 0 |

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These *IMPACT*™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

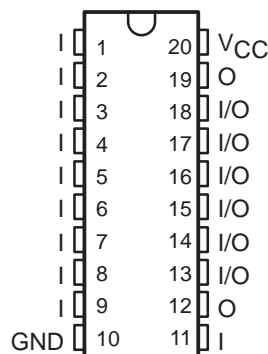
The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of -55°C to 125°C.



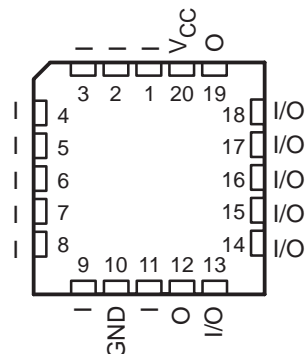
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments.
PAL is a registered trademark of Advanced Micro Devices Inc.

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



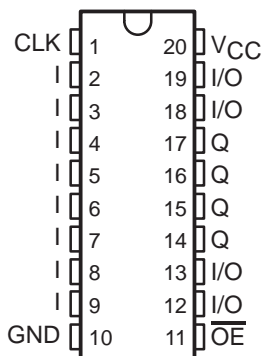
TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



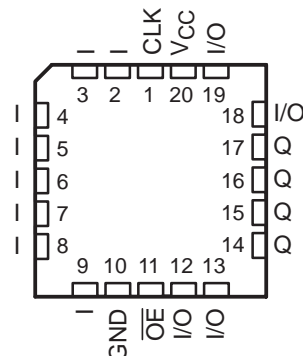
TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C
 TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
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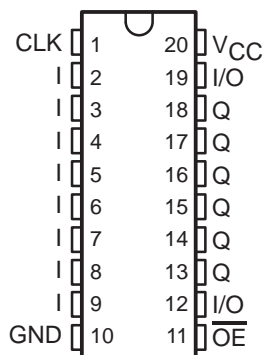
TIBPAL16R4'
 C SUFFIX ... J OR N PACKAGE
 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



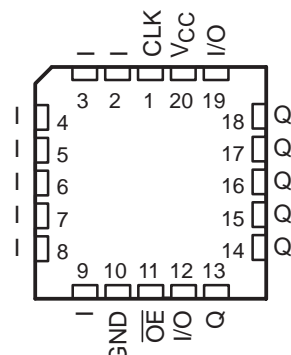
TIBPAL16R4'
 C SUFFIX ... FN PACKAGE
 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



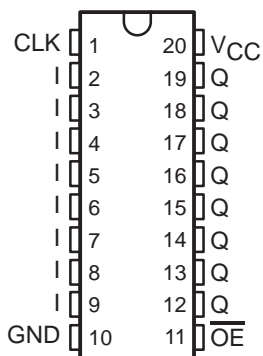
TIBPAL16R6'
 C SUFFIX ... J OR N PACKAGE
 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



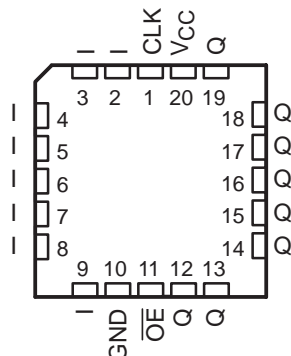
TIBPAL16R6'
 C SUFFIX ... FN PACKAGE
 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



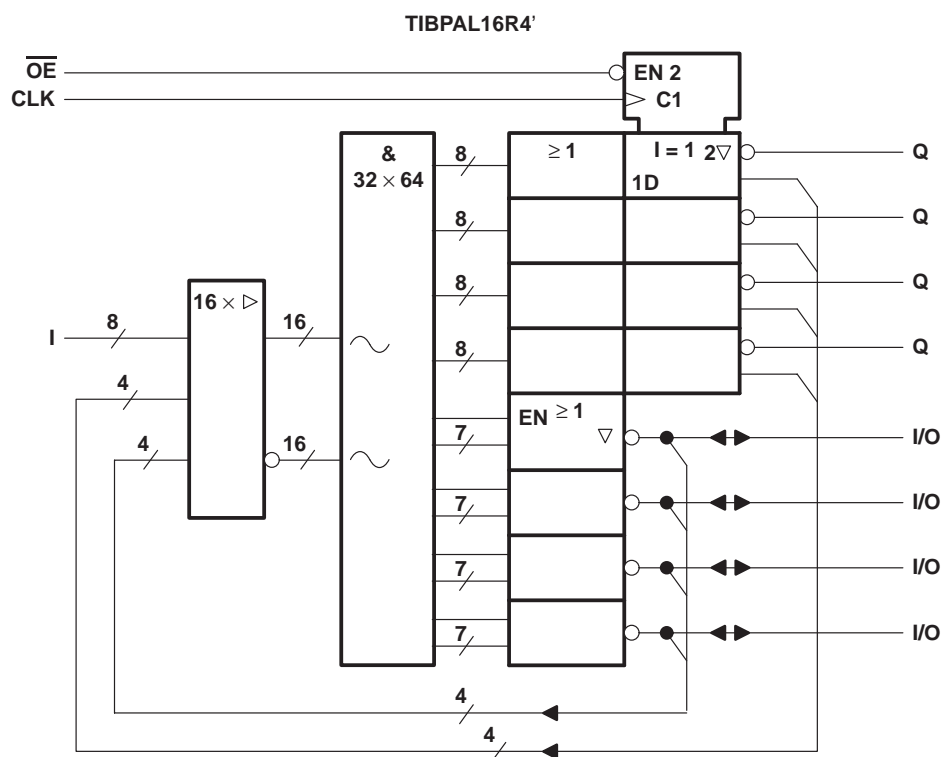
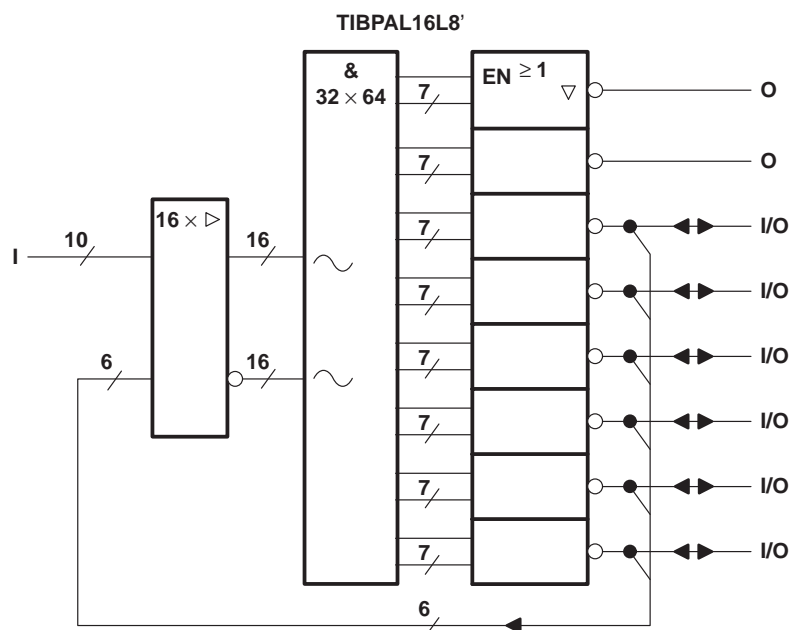
TIBPAL16R8'
 C SUFFIX ... J OR N PACKAGE
 M SUFFIX ... J OR W PACKAGE
 (TOP VIEW)



TIBPAL16R8'
 C SUFFIX ... FN PACKAGE
 M SUFFIX ... FK PACKAGE
 (TOP VIEW)



functional block diagrams (positive logic)

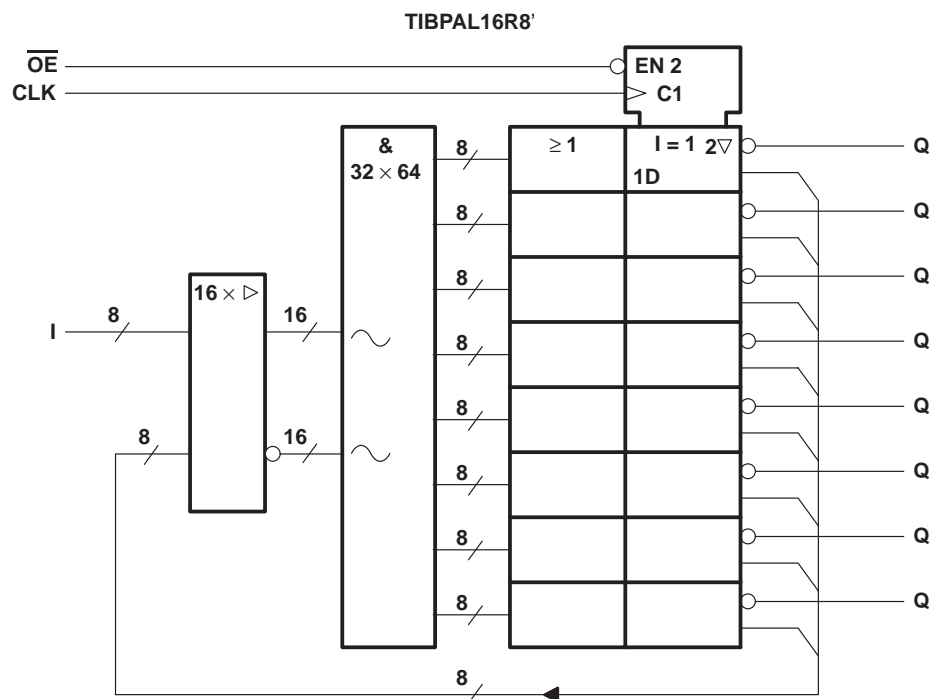
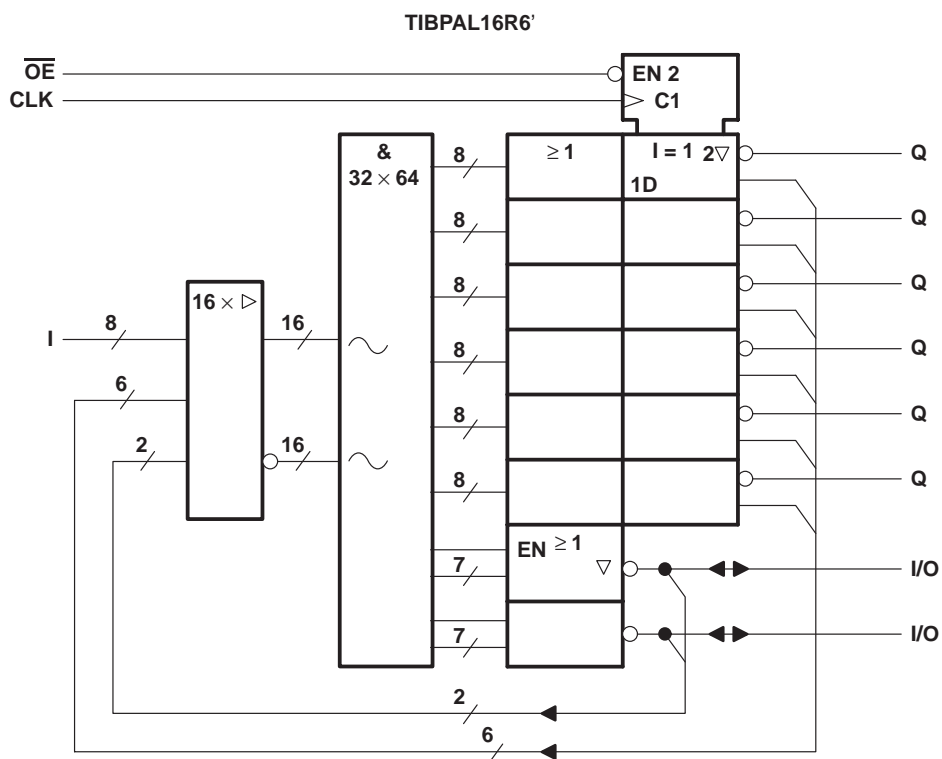


~ denotes fused inputs

TIBPAL 16R6-15C, TIBPAL 16R8-15C
 TIBPAL 16R6-20M, TIBPAL 16R8-20M
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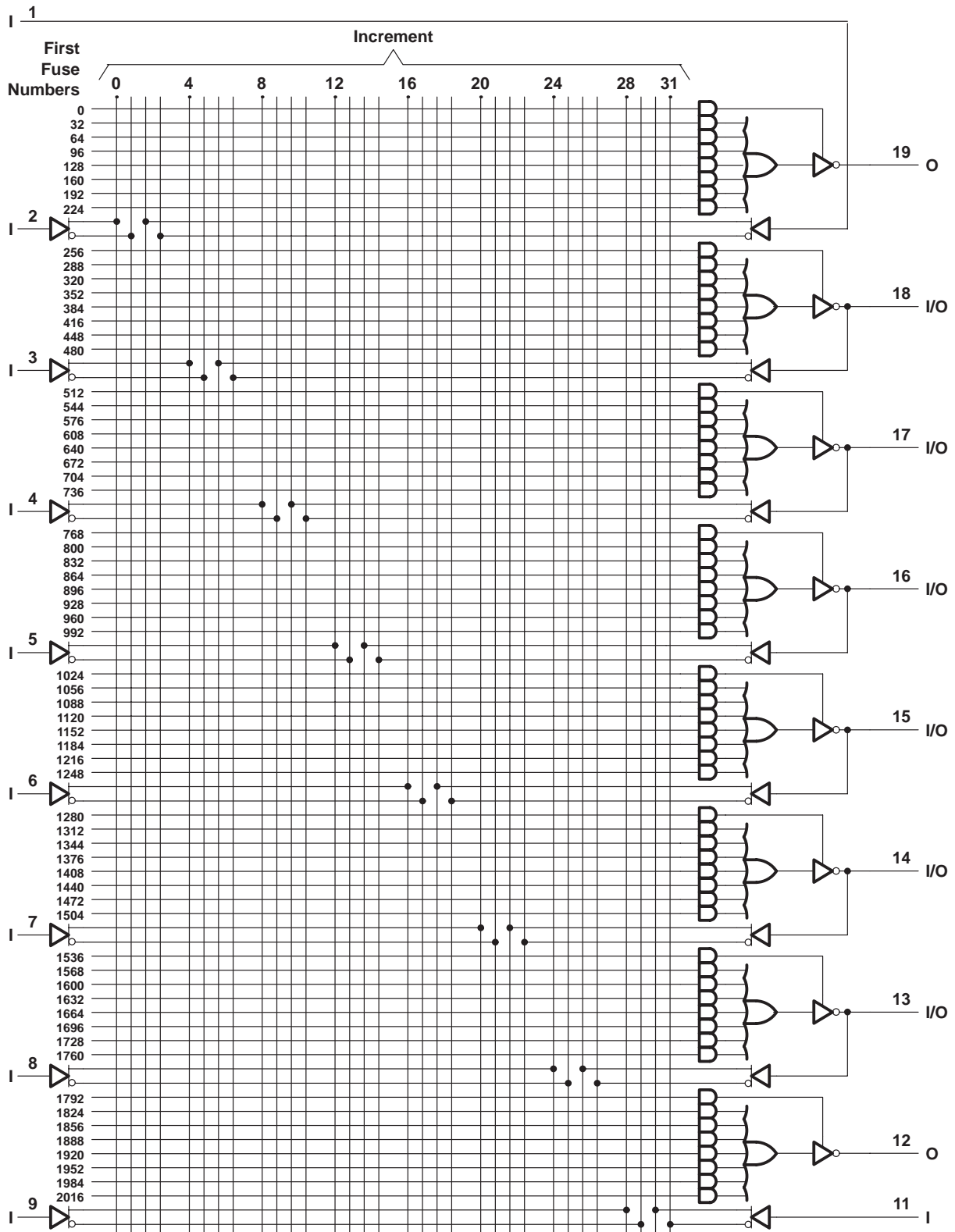
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functional block diagrams (positive logic)



⋯ denotes fused inputs

logic diagram (positive logic)



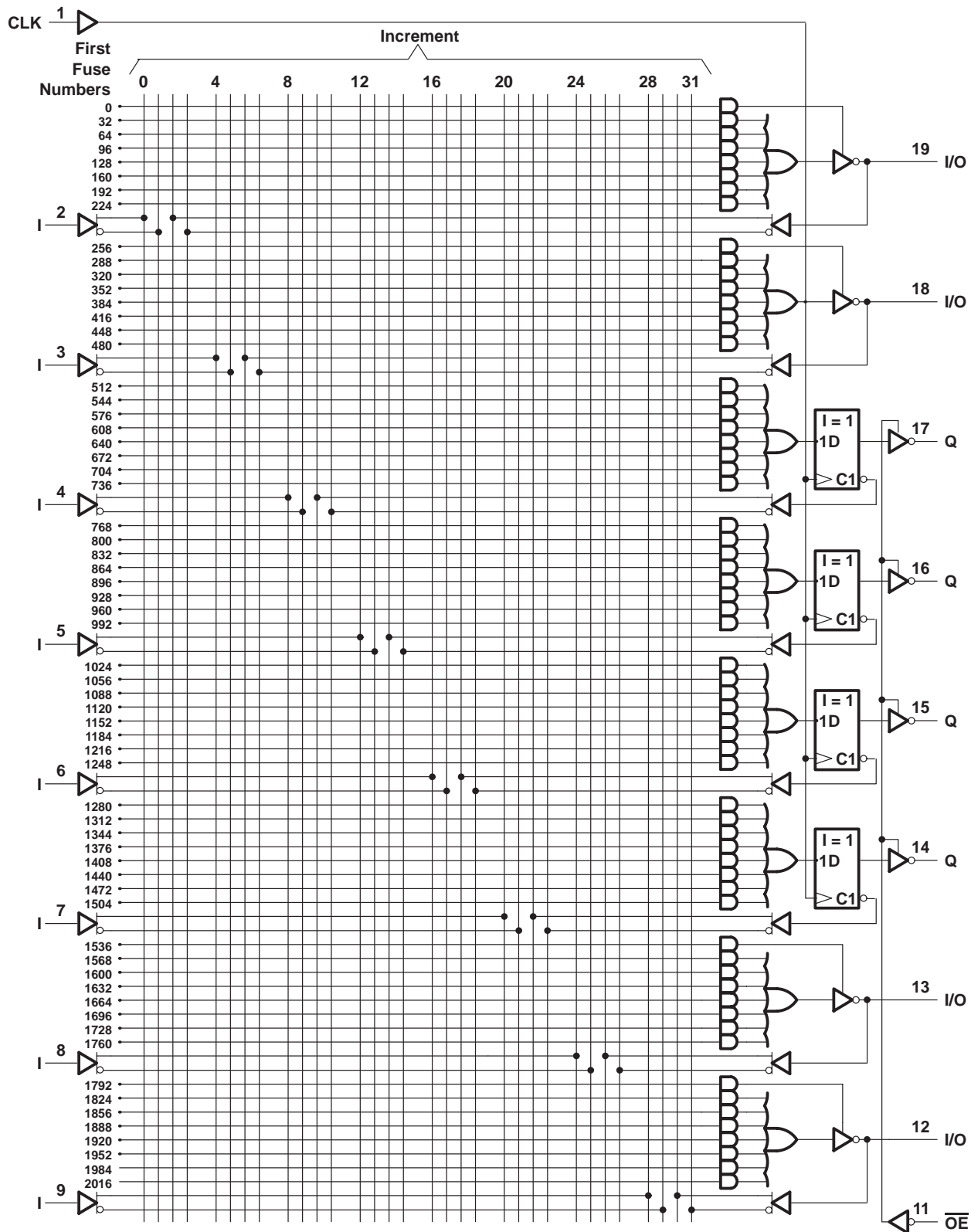
Fuse number = First fuse number + Increment



TIBPAL 16R4-15C TIBPAL 16R4-20M HIGH-PERFORMANCE *IMPACT*™ PAL® CIRCUITS

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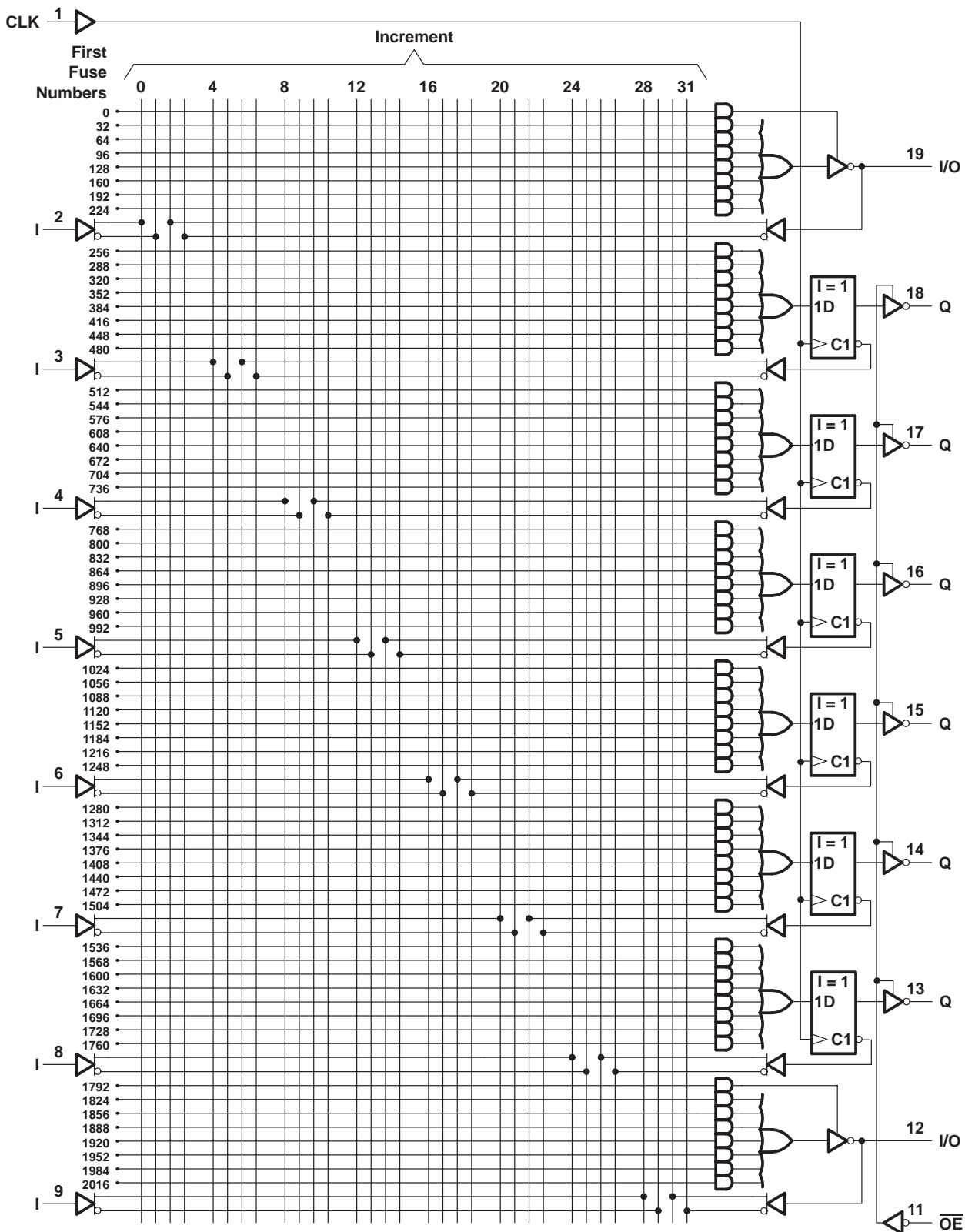
logic diagram (positive logic)



Fuse number = First fuse number + Increment



logic diagram (positive logic)



Fuse number = First fuse number + Increment

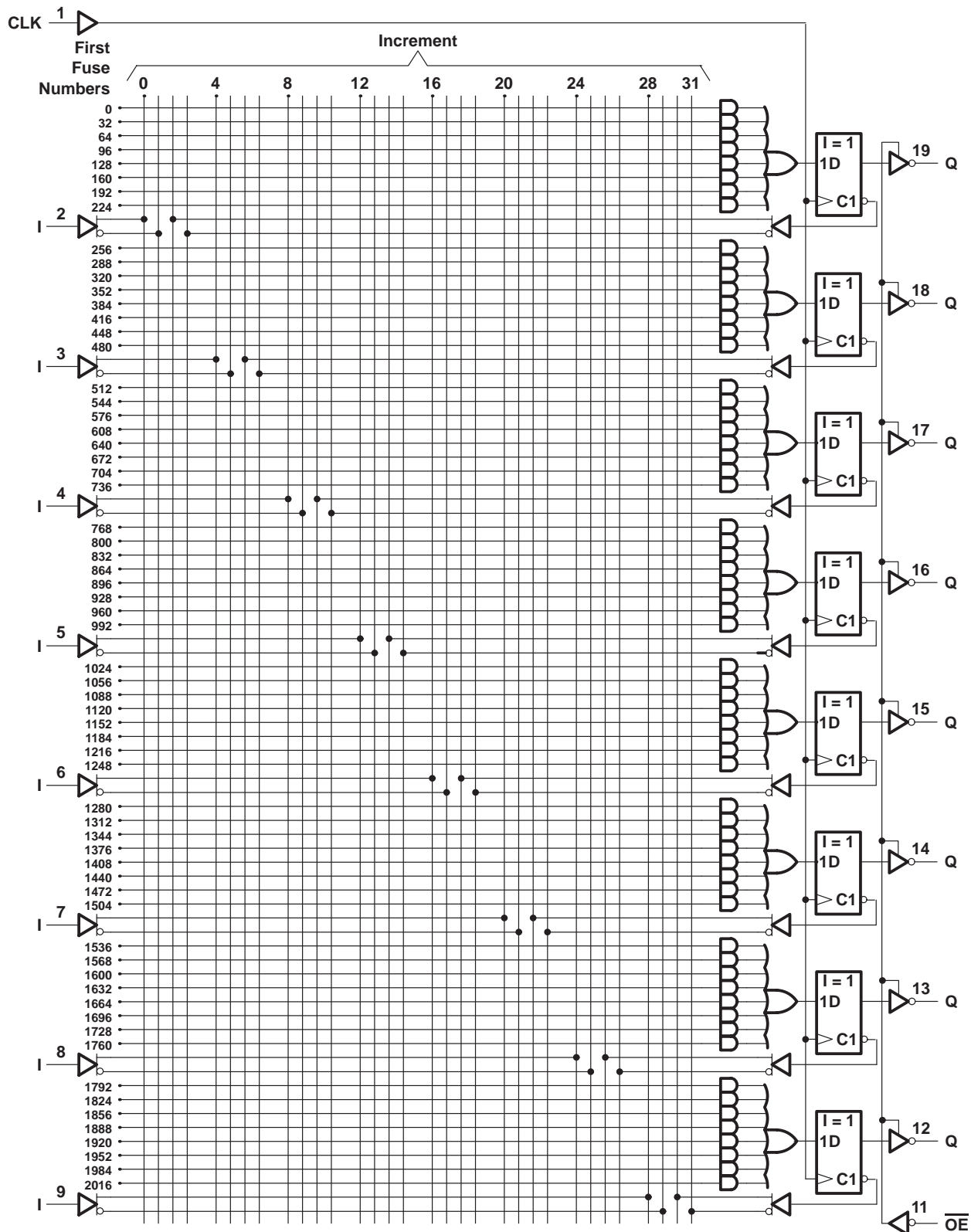


TIBPAL 16R8-15C TIBPAL 16R8-20M

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logic diagram (positive logic)



Fuse number = First fuse number + Increment



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage (see Note 1) | 5.5 V |
| Voltage applied to disabled output (see Note 1) | 5.5 V |
| Operating free-air temperature range | 0°C to 75°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-------------|---|------|-----|------|------|
| V_{CC} | Supply voltage | 4.75 | 5 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | 5.5 | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | -3.2 | mA |
| I_{OL} | Low-level output current | | | 24 | mA |
| f_{clock} | Clock frequency | 0 | | 50 | MHz |
| t_w | Pulse duration, clock (see Note 2) | High | 8 | | ns |
| | | Low | 9 | | |
| t_{su} | Setup time, input or feedback before clock \uparrow | 15 | | | ns |
| t_h | Hold time, input or feedback after clock \uparrow | 0 | | | ns |
| T_A | Operating free-air temperature | 0 | 25 | 75 | °C |

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

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electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT | |
|-----------------|-----------|-----------------------------|----------------------------|-----|------|------|---------------|----|
| V_{IK} | | $V_{CC} = 4.75 \text{ V}$, | $I_I = -18 \text{ mA}$ | | | -1.5 | V | |
| V_{OH} | | $V_{CC} = 4.75 \text{ V}$, | $I_{OH} = -3.2 \text{ mA}$ | 2.4 | 3.3 | | V | |
| V_{OL} | | $V_{CC} = 4.75 \text{ V}$, | $I_{OL} = 24 \text{ mA}$ | | 0.35 | 0.5 | V | |
| I_{OZH} | Outputs | $V_{CC} = 5.25 \text{ V}$, | $V_O = 2.7 \text{ V}$ | | | 20 | μA | |
| | I/O ports | | | | | 100 | | |
| I_{OZL} | Outputs | $V_{CC} = 5.25 \text{ V}$, | $V_O = 0.4 \text{ V}$ | | | -20 | μA | |
| | I/O ports | | | | | -250 | | |
| I_I | | $V_{CC} = 5.25 \text{ V}$, | $V_I = 5.5 \text{ V}$ | | | 0.1 | mA | |
| I_{IH} | | $V_{CC} = 5.25 \text{ V}$, | $V_I = 2.7 \text{ V}$ | | | 20 | μA | |
| I_{IL} | | $V_{CC} = 5.25 \text{ V}$, | $V_I = 0.4 \text{ V}$ | | | -0.2 | mA | |
| $I_{O\ddagger}$ | | $V_{CC} = 5.25 \text{ V}$, | $V_O = 2.25 \text{ V}$ | -30 | | -125 | mA | |
| I_{CC} | | $V_{CC} = 5.25 \text{ V}$, | $V_I = 0$, | | | 140 | 180 | mA |
| | | | Outputs open | | | | | |

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.‡ The output conditions have been chosen to produce a current that closely approximates one-half of the short-circuit output current, I_{OS} .

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|-----------|--------------|-------------|--|-----|------|-----|------|
| f_{max} | | | R1 = 500 Ω , R2 = 500 Ω , See Figure 3 | 50 | | | MHz |
| t_{pd} | I, I/O | O, I/O | | 10 | 15 | | ns |
| t_{pd} | CLK↑ | Q | | 8 | 12 | | ns |
| t_{en} | OE↓ | Q | | 8 | 12 | | ns |
| t_{dis} | OE↑ | Q | | 7 | 10 | | ns |
| t_{en} | I, I/O | O, I/O | | 10 | 15 | | ns |
| t_{dis} | I, I/O | O, I/O | | 10 | 15 | | ns |

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage (see Note 1) | 5.5 V |
| Voltage applied to disabled output (see Note 1) | 5.5 V |
| Operating free-air temperature range | –55°C to 125°C |
| Storage temperature range, T_{stg} | –65°C to 150°C |

NOTE 1: These ratings apply, except for programming pins, during a programming cycle.

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-------------|---|------|-----|------|------|
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 5.5 | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | –2 | mA |
| I_{OL} | Low-level output current | | | 12 | mA |
| f_{clock} | Clock frequency | 0 | | 41.6 | MHz |
| t_w | Pulse duration, clock (see Note 2) | High | 10 | | ns |
| | | Low | 11 | | |
| t_{su} | Setup time, input or feedback before clock↑ | 20 | | | ns |
| t_h | Hold time, input or feedback after clock↑ | 0 | | | ns |
| T_A | Operating free-air temperature | –55 | 25 | 125 | °C |

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock} . The minimum pulse durations specified are for clock high or low only, but not for both simultaneously.

TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M

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electrical characteristics over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-------------------|------------|---------------------------|-----------------------------|-----|------|-------|---------------|
| V_{IK} | | $V_{CC} = 4.5\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.5 | V |
| V_{OH} | | $V_{CC} = 4.5\text{ V}$, | $I_{OH} = -2\text{ mA}$ | 2.4 | 3.2 | | V |
| V_{OL} | | $V_{CC} = 4.5\text{ V}$, | $I_{OL} = 12\text{ mA}$ | | 0.25 | 0.4 | V |
| I_{OZH} | Outputs | $V_{CC} = 5.5\text{ V}$, | $V_O = 2.7\text{ V}$ | | | 20 | μA |
| | I/O ports | | | | | 100 | |
| I_{OZL} | Outputs | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.4\text{ V}$ | | | -20 | μA |
| | I/O ports | | | | | -250 | |
| I_I | Pin 1, 11 | $V_{CC} = 5.5\text{ V}$, | $V_I = 5.5\text{ V}$ | | | 0.2 | mA |
| | All others | | | | | 0.1 | |
| I_{IH} | Pin 1, 11 | $V_{CC} = 5.5\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 50 | μA |
| | I/O ports | | | | | 100 | |
| | All others | | | | | 20 | |
| I_{IL} | I/O ports | $V_{CC} = 5.5\text{ V}$, | $V_I = 0.4\text{ V}$ | | | -0.25 | mA |
| | All others | | | | | -0.2 | |
| I_{OS}^\ddagger | | $V_{CC} = 5.5\text{ V}$, | $V_O = 0.5\text{ V}$ | -30 | | -250 | mA |
| I_{CC} | | $V_{CC} = 5.5\text{ V}$, | $V_I = 0$, Outputs open | | 140 | 190 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test-equipment degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP† | MAX | UNIT | |
|-----------|-----------------|-------------|--|------|------|-----|------|----|
| f_{max} | | | R1 = 390 Ω , R2 = 750 Ω , See Figure 4 | 41.6 | | | MHz | |
| t_{pd} | I, I/O | O, I/O | | | | 10 | 20 | ns |
| t_{pd} | CLK \uparrow | Q | | | | 8 | 15 | ns |
| t_{en} | OE \downarrow | Q | | | | 8 | 15 | ns |
| t_{dis} | OE \uparrow | Q | | | | 7 | 15 | ns |
| t_{en} | I, I/O | O, I/O | | | | 10 | 20 | ns |
| t_{dis} | I, I/O | O, I/O | | | | 10 | 20 | ns |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

programming information

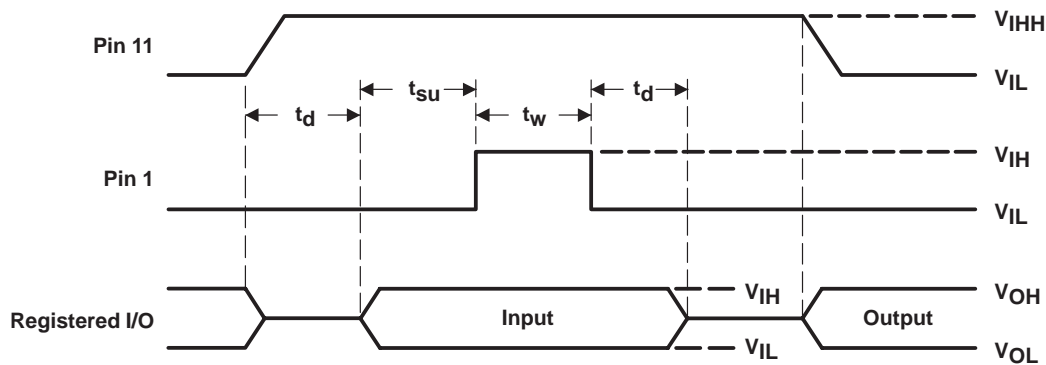
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic also is available, upon request, from the nearest TI field sales office or local authorized TI distributor, by calling Texas Instruments at +1 (972) 644-5580, or by visiting the TI Semiconductor Home Page at www.ti.com/sc.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With V_{CC} at 5 V and Pin 1 at V_{IL} , raise Pin 11 to V_{IHH} .
- Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
- Step 3. Pulse Pin 1, clocking in preload data.
- Step 4. Remove output voltage, then lower Pin 11 to V_{IL} . Preload can be verified by observing the voltage level at the output pin.



NOTE 3: $t_d = t_{su} = t_h = 100$ ns to 1000 ns $V_{IHH} = 10.25$ V to 10.75 V

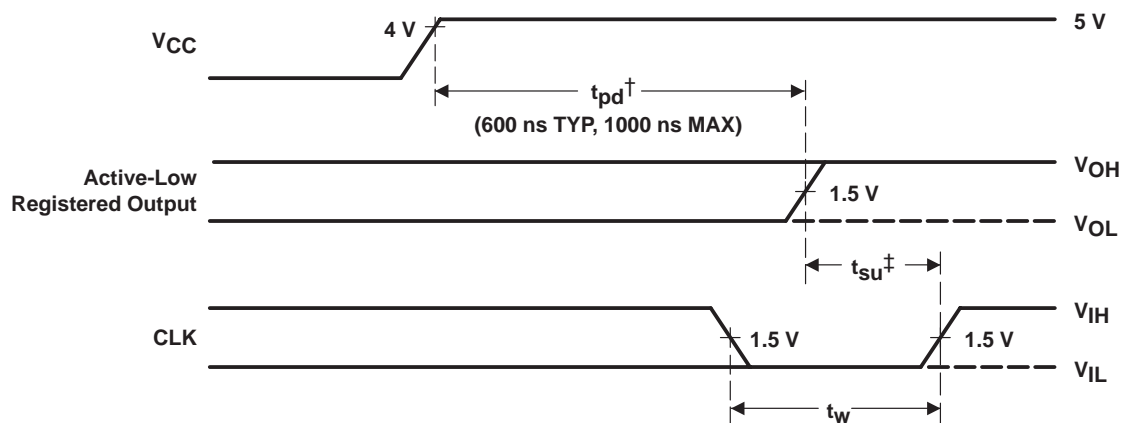
Figure 1. Preload Waveforms

TIBPAL 16L8-15C, TIBPAL 16R4-15C, TIBPAL 16R6-15C, TIBPAL 16R8-15C
 TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M
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power-up reset (see Figure 2)

Following power up, all registers are set high. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.

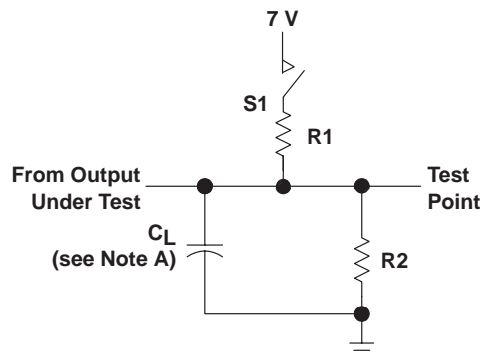


† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

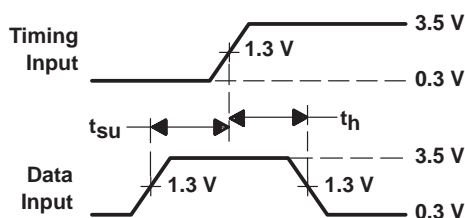
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

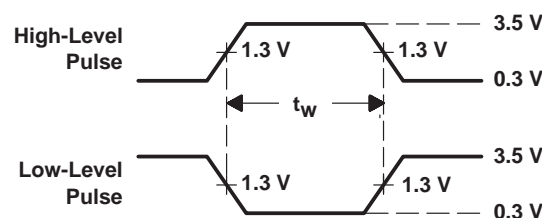
PARAMETER MEASUREMENT INFORMATION



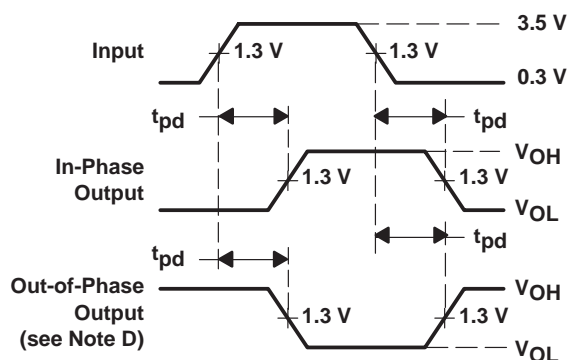
LOAD CIRCUIT FOR 3-STATE OUTPUTS



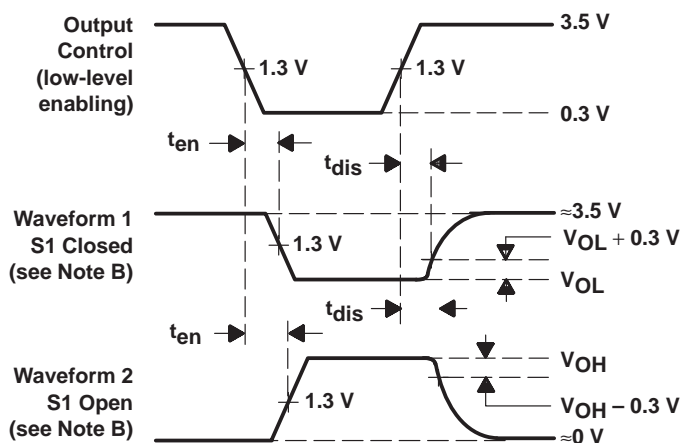
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

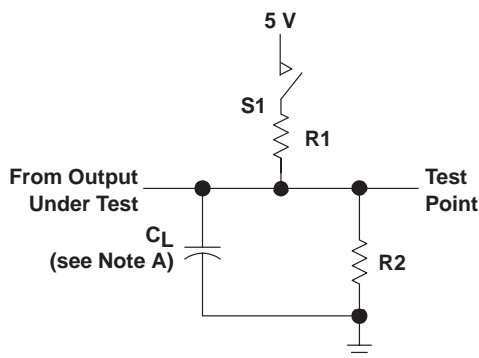
- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
 D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed. When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.
 E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

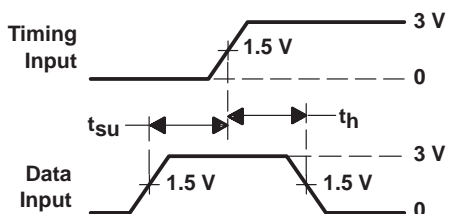
TIBPAL 16L8-20M, TIBPAL 16R4-20M, TIBPAL 16R6-20M, TIBPAL 16R8-20M HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

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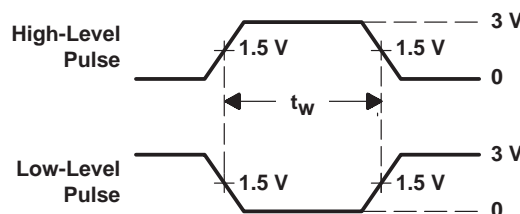
PARAMETER MEASUREMENT INFORMATION



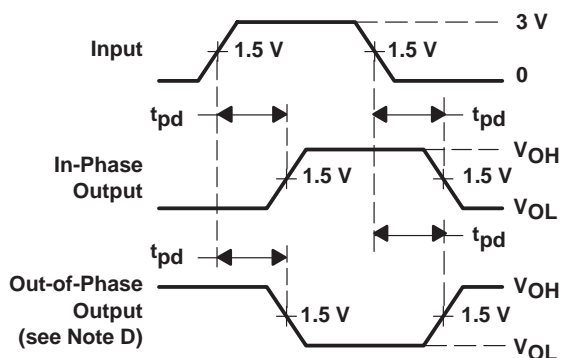
LOAD CIRCUIT FOR 3-STATE OUTPUTS



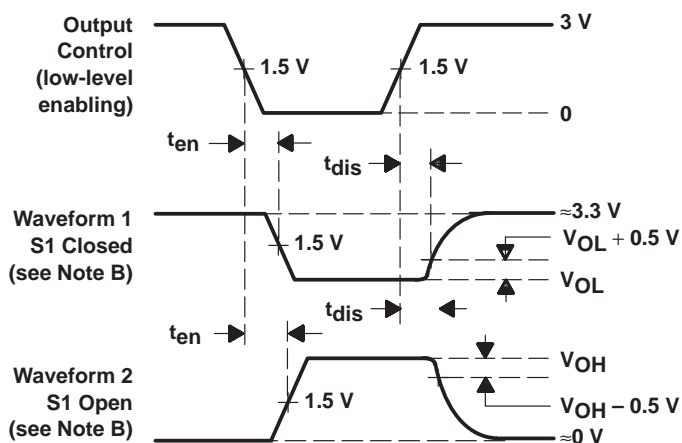
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} , 5 pF for t_{dis} .
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses have the following characteristics: $PRR \leq 10$ MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
 D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
 E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| 5962-85155012A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155012A TIBPAL16 L8-20MFKB |
| 5962-8515501RA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515501RA TIBPAL16L8-20M JB |
| 5962-8515501SA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515501SA TIBPAL16L8-20M WB |
| 5962-85155022A | NRND | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155022A TIBPAL16 R8-20MFKB |
| 5962-8515502RA | NRND | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515502RA TIBPAL16R8-20M JB |
| 5962-85155032A | NRND | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155032A TIBPAL16 R6-20MFKB |
| 5962-8515503RA | NRND | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515503RA TIBPAL16R6-20M JB |
| 5962-8515503SA | NRND | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515503SA TIBPAL16R6-20M WB |
| 5962-85155042A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155042A TIBPAL16 R4-20MFKB |
| 5962-8515504RA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515504RA TIBPAL16R4-20M JB |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| 5962-8515504SA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515504SA TIBPAL16R4-20M WB |
| JM38510/50601BRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 50601BRA |
| JM38510/50601BRA.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 50601BRA |
| JM38510/50604BRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 50604BRA |
| JM38510/50604BRA.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 50604BRA |
| M38510/50601BRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 50601BRA |
| M38510/50604BRA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 50604BRA |
| TIBPAL16L8-20MFKB | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155012A TIBPAL16 L8-20MFKB |
| TIBPAL16L8-20MFKB.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155012A TIBPAL16 L8-20MFKB |
| TIBPAL16L8-20MJ | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TIBPAL16L8-20M J |
| TIBPAL16L8-20MJ.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | TIBPAL16L8-20M J |
| TIBPAL16L8-20MJB | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515501RA TIBPAL16L8-20M JB |
| TIBPAL16L8-20MJB.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515501RA TIBPAL16L8-20M JB |
| TIBPAL16L8-20MWB | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515501SA TIBPAL16L8-20M WB |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| TIBPAL16L8-20MWB.A | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515501SA TIBPAL16L8-20M WB |
| TIBPAL16R4-20MFKB | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155042A TIBPAL16 R4-20MFKB |
| TIBPAL16R4-20MFKB.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155042A TIBPAL16 R4-20MFKB |
| TIBPAL16R4-20MJB | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515504RA TIBPAL16R4-20M JB |
| TIBPAL16R4-20MJB.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515504RA TIBPAL16R4-20M JB |
| TIBPAL16R4-20MWB | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515504SA TIBPAL16R4-20M WB |
| TIBPAL16R4-20MWB.A | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515504SA TIBPAL16R4-20M WB |
| TIBPAL16R6-20MFKB | NRND | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155032A TIBPAL16 R6-20MFKB |
| TIBPAL16R6-20MFKB.A | NRND | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155032A TIBPAL16 R6-20MFKB |
| TIBPAL16R6-20MJB | NRND | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515503RA TIBPAL16R6-20M JB |
| TIBPAL16R6-20MJB.A | NRND | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515503RA TIBPAL16R6-20M JB |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| TIBPAL16R6-20MWB | NRND | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515503SA TIBPAL16R6-20M WB |
| TIBPAL16R6-20MWB.A | NRND | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515503SA TIBPAL16R6-20M WB |
| TIBPAL16R8-20MFKB | NRND | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155022A TIBPAL16 R8-20MFKB |
| TIBPAL16R8-20MFKB.A | NRND | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 85155022A TIBPAL16 R8-20MFKB |
| TIBPAL16R8-20MJB | NRND | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515502RA TIBPAL16R8-20M JB |
| TIBPAL16R8-20MJB.A | NRND | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8515502RA TIBPAL16R8-20M JB |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

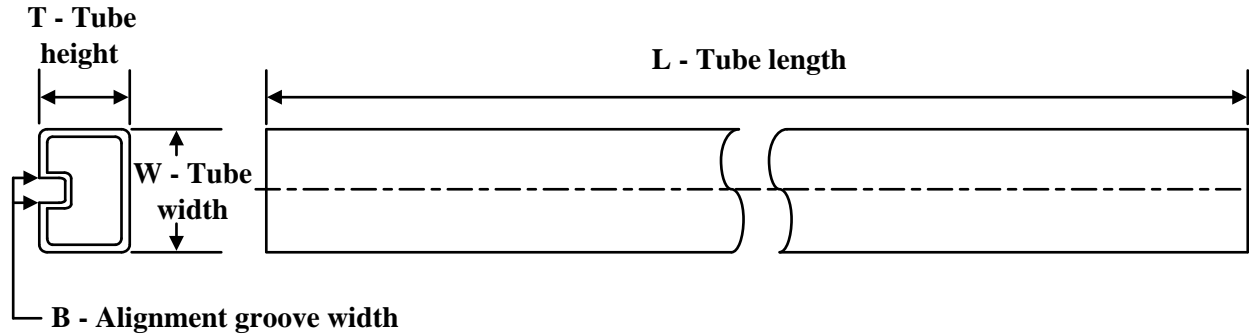
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-85155012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8515501SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-85155022A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-85155032A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8515503SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-85155042A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8515504SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16L8-20MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16L8-20MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16L8-20MWB | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16L8-20MWB.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16R4-20MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16R4-20MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16R4-20MWB | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16R4-20MWB.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16R6-20MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16R6-20MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16R6-20MWB | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16R6-20MWB.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| TIBPAL16R8-20MFKB | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| TIBPAL16R8-20MFKB.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

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