

## TPS783xx 500-nA $I_Q$ , 150-mA, Ultralow Quiescent Current Low-Dropout Linear Regulator

### 1 Features

- Input Voltage Range: 2.2 V to 5.5 V
- Low Quiescent Current ( $I_Q$ ): 500 nA
- 150-mA, Low-Dropout Regulator
- Low-Dropout at 25°C, 130 mV at 150 mA
- Low-Dropout at 85°C, 175 mV at 150 mA
- 3% Accuracy Over Load, Line, and Temperature
- Stable with a 1.0- $\mu$ F Ceramic Capacitor
- Thermal Shutdown and Overcurrent Protection
- CMOS Logic Level-Compatible Enable Pin
- DDC (SOT-5) Package

### 2 Applications

- TI [MSP430](#) Attach Applications
- Wireless Handsets and Smartphones
- MP3 Players
- Battery-Operated Handheld Products

### 3 Description

The TPS783 family of low-dropout regulators (LDOs) offers the benefits of ultralow power and miniaturized packaging.

This LDO family is designed specifically for battery-powered applications where ultralow quiescent current is a critical parameter. The TPS783, with ultralow  $I_Q$  (500 nA), is ideal for microprocessors, microcontrollers, and other battery-powered applications.

The absence of pulldown circuitry at the output of the LDO provides the flexibility to use the regulator output capacitor as a temporary backup power supply (for example, during battery replacement).

The ultralow power and miniaturized packaging allow designers to customize power consumption for specific applications. Consult with your local factory representative for exact voltage options and ordering information; minimum order quantities may apply.

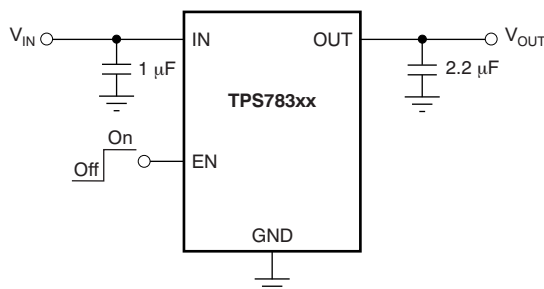
The TPS783 family is compatible with the TI [MSP430](#) and other similar products. The enable pin (EN) is compatible with standard CMOS logic. This device allows for minimal board space because of miniaturized packaging and a potentially small output capacitor. The TPS783 family also features thermal shutdown and current limit to protect the device during fault conditions. All packages have a specified operating temperature range of  $T_J = -40^\circ\text{C}$  to  $105^\circ\text{C}$ .

#### Device Information<sup>(1)</sup>

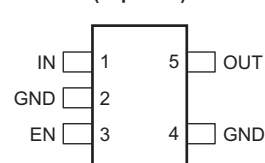
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS783xx	SOT (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the package option addendum at the end of the datasheet.

#### Simplified Schematic



TPS783xxDDC  
SOT-5  
(Top View)



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>10</b>
<b>2 Applications</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>11</b>
<b>3 Description</b> .....	<b>1</b>	8.1 Application Information.....	<b>11</b>
<b>4 Revision History</b> .....	<b>2</b>	8.2 Typical Application .....	<b>11</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.3 System Examples .....	<b>13</b>
<b>6 Specifications</b> .....	<b>4</b>	8.4 Do's and Don'ts.....	<b>15</b>
6.1 Absolute Maximum Ratings .....	<b>4</b>	<b>9 Power-Supply Recommendations</b> .....	<b>15</b>
6.2 Handling Ratings.....	<b>4</b>	<b>10 Layout</b> .....	<b>15</b>
6.3 Recommended Operating Conditions.....	<b>4</b>	10.1 Layout Guidelines .....	<b>15</b>
6.4 Thermal Information .....	<b>4</b>	10.2 Layout Example .....	<b>16</b>
6.5 Electrical Characteristics.....	<b>5</b>	<b>11 Device and Documentation Support</b> .....	<b>17</b>
6.6 Typical Characteristics .....	<b>6</b>	11.1 Device Support .....	<b>17</b>
<b>7 Detailed Description</b> .....	<b>9</b>	11.2 Trademarks .....	<b>17</b>
7.1 Overview .....	<b>9</b>	11.3 Electrostatic Discharge Caution.....	<b>17</b>
7.2 Functional Block Diagram .....	<b>9</b>	11.4 Glossary .....	<b>17</b>
7.3 Feature Description.....	<b>9</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>17</b>

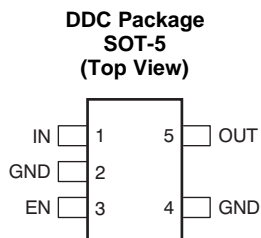
## 4 Revision History

### Changes from Original (February 2010) to Revision A

Page

• Changed document format to latest data sheet standards; added <i>Handling Ratings</i> , <i>Thermal Information</i> , <i>Recommended Operating Conditions</i> , <i>Power Supply Recommendations</i> , and <i>Device and Documentation Support</i> sections; moved existing sections .....	<b>1</b>
• Deleted factory programming feature bullet .....	<b>1</b>
• Added input voltage range feature bullet .....	<b>1</b>
• Deleted programmable mode application bullet .....	<b>1</b>
• Added simplified schematic to front page.....	<b>1</b>
• Changed <i>Pin Functions</i> table .....	<b>3</b>
• Changed operating junction temperature maximum value in <i>Absolute Maximum Ratings</i> table .....	<b>4</b>
• Deleted <i>Dissipation Ratings</i> table; see <i>Thermal Information</i> table.....	<b>4</b>
• Changed symbol and parameter names for clarity in <i>Electrical Characteristics</i> table .....	<b>5</b>
• Added footnote (2) to <i>Electrical Characteristics</i> table .....	<b>5</b>
• Changed <a href="#">Figure 7</a> y-axis title and measurement range .....	<b>7</b>
• Changed <a href="#">Figure 9</a> V <sub>EN</sub> labels to match <i>Electrical Characteristics</i> table .....	<b>7</b>
• Changed <a href="#">Figure 10</a> y-axis title to match <i>Electrical Characteristics</i> table .....	<b>7</b>
• Deleted <a href="#">Figure 14</a> I <sub>OUT</sub> condition .....	<b>7</b>
• Deleted <a href="#">Figure 15</a> I <sub>OUT</sub> condition .....	<b>7</b>
• Changed <a href="#">Functional Block Diagram</a> .....	<b>9</b>
• Changed <a href="#">Figure 18</a> .....	<b>10</b>
• Added reference for <a href="#">Table 1</a> in <i>Device Functional Modes</i> .....	<b>10</b>
• Changed <a href="#">Figure 19</a> .....	<b>11</b>
• Changed <a href="#">Table 2</a> format.....	<b>14</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Drive this pin over 1.2 V to turn on the regulator. Drive this pin below 0.4 V to put the regulator into shutdown mode, reducing operating current to 18 nA, typical.
GND	2, 4	—	Ground pin. Tie all ground pins to ground for proper operation.
IN	1	I	Input pin. For stable operation, place a small, 0.1- $\mu$ F capacitor from this pin to ground; typical input capacitor = 1.0 $\mu$ F. Tie back both input and output capacitor grounds to the IC ground, with no significant impedance between them.
OUT	5	O	Regulated output voltage pin. Connect a small (1- $\mu$ F or greater) ceramic capacitor from this pin to ground for stable operation. See the <a href="#">Input and Output Capacitor Requirements</a> in the <a href="#">Application and Implementation</a> section for more details.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

At  $T_J = -40^\circ\text{C}$  to  $105^\circ\text{C}$  (unless otherwise noted). All voltages are with respect to GND.<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	$V_{IN}$	-0.3	6.0	V
	EN pin	-0.3	$V_{IN} + 0.3$	V
	$V_{OUT}$	-0.3	$V_{IN} + 0.3$	V
Current	$I_{OUT}$	Internally limited		A
	Output short-circuit duration	Indefinite		
Temperature	Operating junction, $T_J$	-40	160	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 Handling Ratings

		MIN	MAX	UNIT	
$T_{stg}$	Storage temperature range	-55	150	$^\circ\text{C}$	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	-2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	-500	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	2.2		5.5	V
$V_{OUT}$	Output voltage	1.8		4.2	V
$V_{EN}$	Enable voltage	0		$V_{IN}$	V
$I_{OUT}$	Output current	0		150	mA
$T_J$	Junction temperature	-40		105	$^\circ\text{C}$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS783xx	UNIT
		DDC (SOT)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.0	$^\circ\text{C/W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.3	
$\Psi_{JT}$	Junction-to-top characterization parameter	0.9	
$\Psi_{JB}$	Junction-to-board characterization parameter	34.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

At  $T_J = -40^\circ\text{C}$  to  $105^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $I_{OUT} = 100\ \mu\text{A}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1.0\ \mu\text{F}$ , and fixed  $V_{OUT}$  test conditions (unless otherwise noted). Typical values at  $T_J = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{IN}$	Input voltage range		2.2		5.5	V	
$V_{OUT}$	DC output accuracy	Nominal	$T_J = 25^\circ\text{C}$		-2%	2%	
		Over $V_{IN}$ , $I_{OUT}$ , temperature	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ , $100\ \mu\text{A} \leq I_{OUT} \leq 150\text{ mA}$		-3.0%	$\pm 2.0\%$	3.0%
$\Delta V_{O(\Delta V)}$	Line regulation	$V_{OUT(nom)} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$			$\pm 1.0\%$		
$\Delta V_{O(\Delta I)}$	Load regulation	$100\ \mu\text{A} \leq I_{OUT} \leq 150\text{ mA}$			$\pm 1.0\%$		
$V_{DO}$	Dropout voltage <sup>(1)</sup>	$V_{IN} = 95\% V_{OUT(nom)}$ , $I_{OUT} = 150\text{ mA}$		130	250	mV	
$I_{LIM}$	Output current limit	$V_{OUT} = 0.90 \times V_{OUT(nom)}$	150	230	400	mA	
$I_{GND}$	GND pin current	$I_{OUT} = 0\text{ mA}$			420	800	nA
		$I_{OUT} = 150\text{ mA}$			8		$\mu\text{A}$
$I_{EN}$	EN pin current	$V_{IN} = V_{EN} = 5.5\text{ V}$			0.07	40	nA
$I_{SHDN(GND)}$	Shutdown current at GND pin	$V_{EN} \leq 0.4\text{ V}$ , $V_{IN(min)} \leq V_{IN} < 5.5\text{ V}^{(2)}$			18	150	nA
$I_{SHDN(OUT)}$	Shutdown current at OUT pin (leakage) <sup>(3)</sup>	$V_{IN} = \text{open}$ , $V_{EN} = 0.4\text{ V}$ , $V_{OUT} = V_{OUT(nom)}$			137	500	nA
$V_{EN(HI)}$	Enable high-level voltage	$V_{IN} = 5.5\text{ V}$	1.2		$V_{IN}$	V	
$V_{EN(LO)}$	Enable low-level voltage	$V_{IN} = 5.5\text{ V}$	0		0.4	V	
PSRR	Power-supply rejection ratio	$V_{IN} = 4.3\text{ V}$ , $V_{OUT} = 3.0\text{ V}$ , $I_{OUT} = 150\text{ mA}$	$f = 10\text{ Hz}$			40	dB
			$f = 100\text{ Hz}$			20	dB
			$f = 1\text{ kHz}$			15	dB
$V_n$	Output noise voltage	$BW = 100\text{ Hz to }100\text{ kHz}$ , $V_{IN} = 2.2\text{ V}$ , $V_{OUT} = 1.2\text{ V}$ , $I_{OUT} = 1\text{ mA}$			86	$\mu\text{V}_{RMS}$	
$t_{STR}$	Startup time <sup>(4)</sup>	$C_{OUT} = 1.0\ \mu\text{F}$ , $V_{OUT} = 10\% V_{OUT(nom)}$ to $V_{OUT} = 90\% V_{OUT(nom)}$			500	$\mu\text{s}$	
$T_{sd}$	Thermal shutdown temperature	Shutdown, temperature increasing			160	$^\circ\text{C}$	
		Reset, temperature decreasing			140	$^\circ\text{C}$	
$T_J$	Operating junction temperature		-40		125	$^\circ\text{C}$	

(1)  $V_{DO}$  is not measured for devices with  $V_{OUT(nom)} \leq 2.3\text{ V}$  because minimum  $V_{IN} = 2.2\text{ V}$ .

(2)  $V_{IN(min)} = (V_{OUT(nom)} + 0.5\text{ V})$  or  $2.2\text{ V}$ , whichever is greater.

(3) See [Shutdown](#) in the [Application and Implementation](#) section for more details.

(4) Time from  $V_{EN} = 1.2\text{ V}$  to  $V_{OUT} = 90\% (V_{OUT(nom)})$ .

### 6.6 Typical Characteristics

At  $T_J = -40^\circ\text{C}$  to  $105^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $I_{OUT} = 100\ \mu\text{A}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1\ \mu\text{F}$ , and  $C_{IN} = 1\ \mu\text{F}$  (unless otherwise noted).

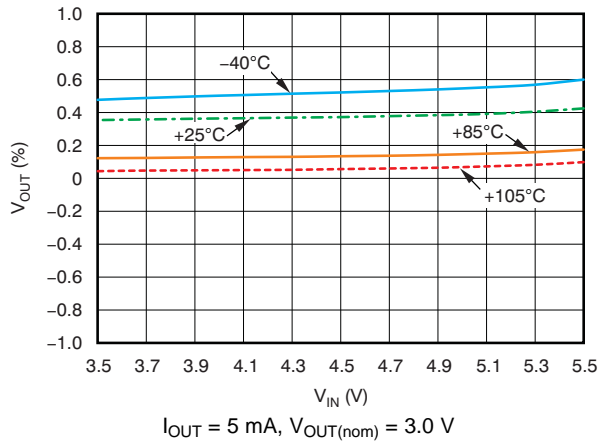


Figure 1. TPS78330 Line Regulation

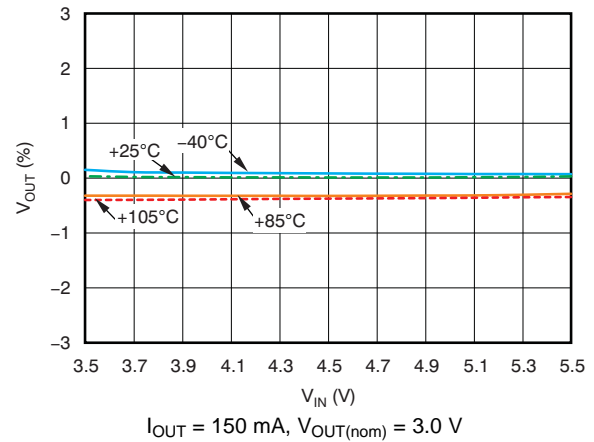


Figure 2. TPS78330 Line Regulation

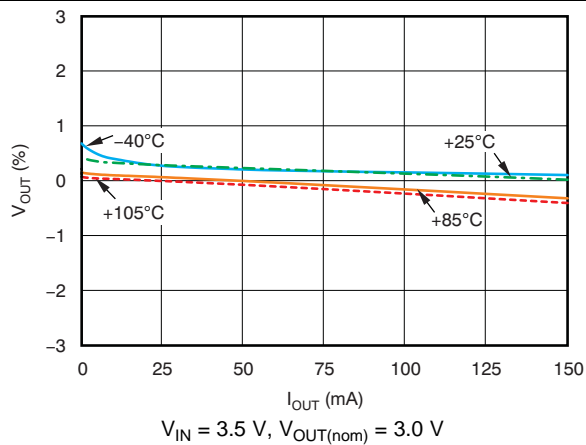


Figure 3. TPS78330 Load Regulation

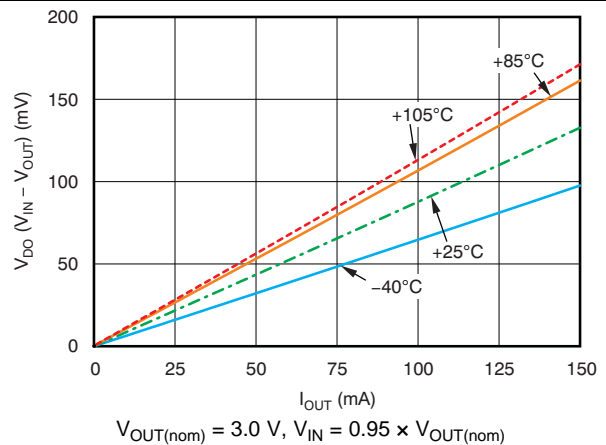


Figure 4. TPS78330 Dropout Voltage vs Output Current

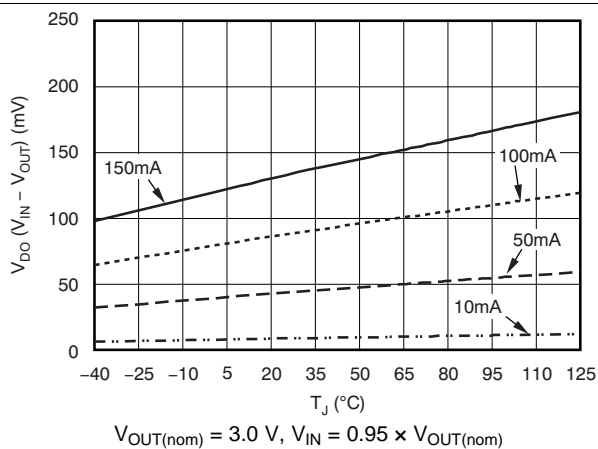


Figure 5. TPS78330 Dropout Voltage vs Junction Temperature

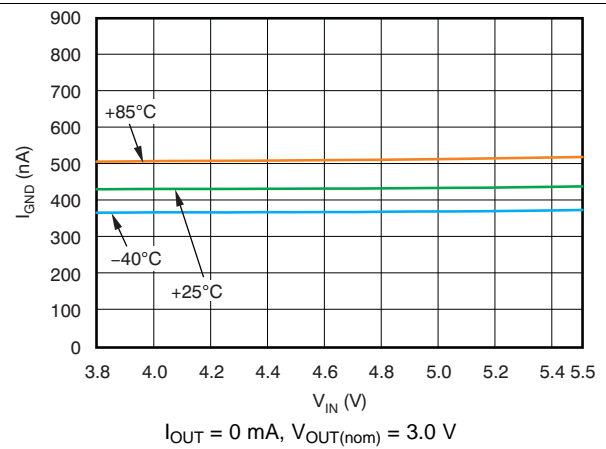


Figure 6. TPS78330 Ground Pin Current vs Input Voltage

Typical Characteristics (continued)

At  $T_J = -40^\circ\text{C}$  to  $105^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $I_{OUT} = 100\ \mu\text{A}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1\ \mu\text{F}$ , and  $C_{IN} = 1\ \mu\text{F}$  (unless otherwise noted).

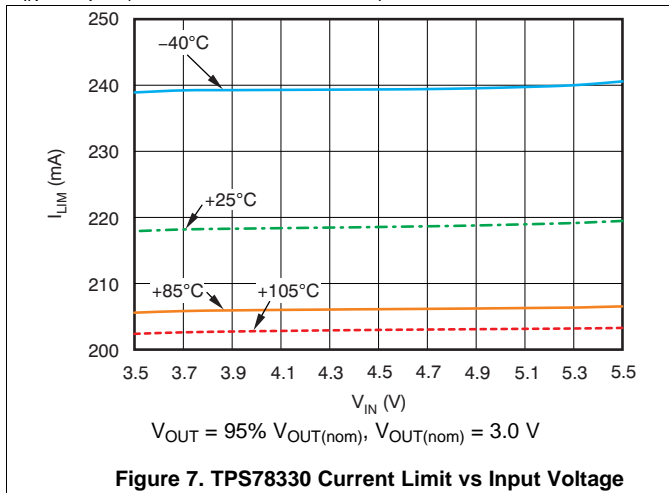


Figure 7. TPS78330 Current Limit vs Input Voltage

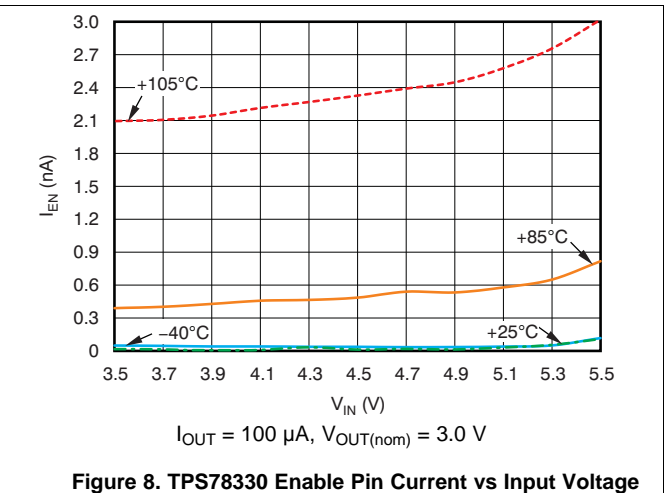


Figure 8. TPS78330 Enable Pin Current vs Input Voltage

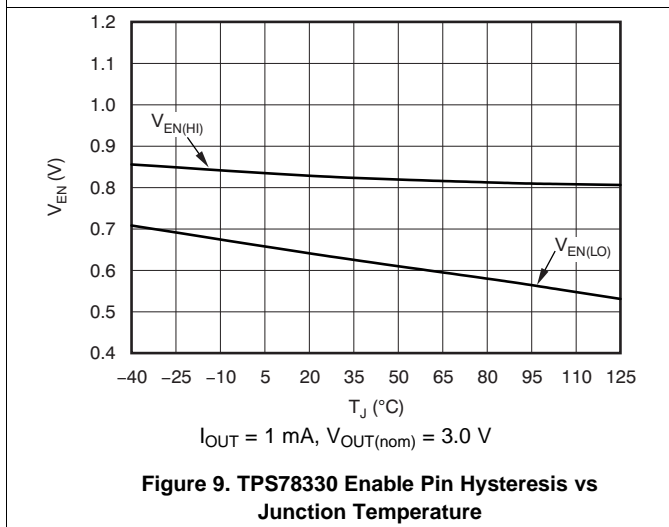


Figure 9. TPS78330 Enable Pin Hysteresis vs Junction Temperature

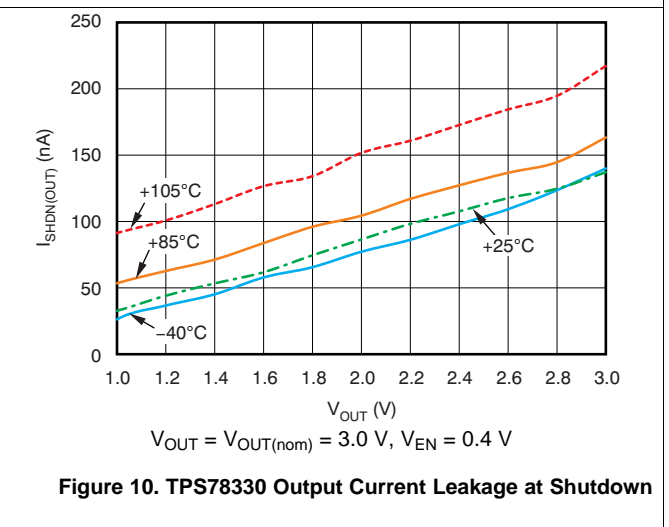


Figure 10. TPS78330 Output Current Leakage at Shutdown

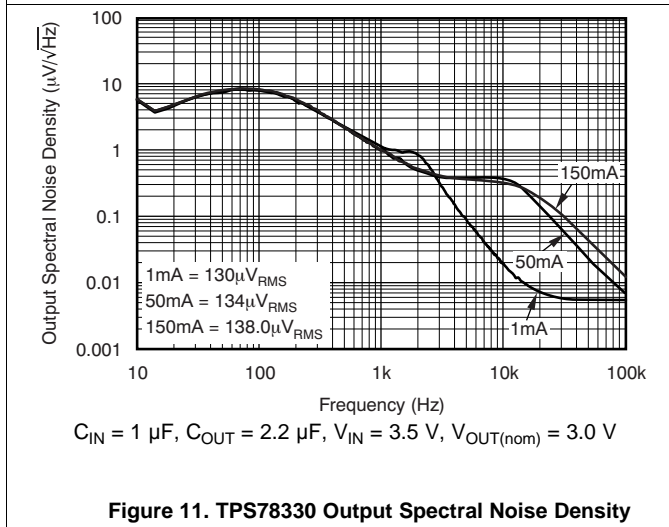


Figure 11. TPS78330 Output Spectral Noise Density

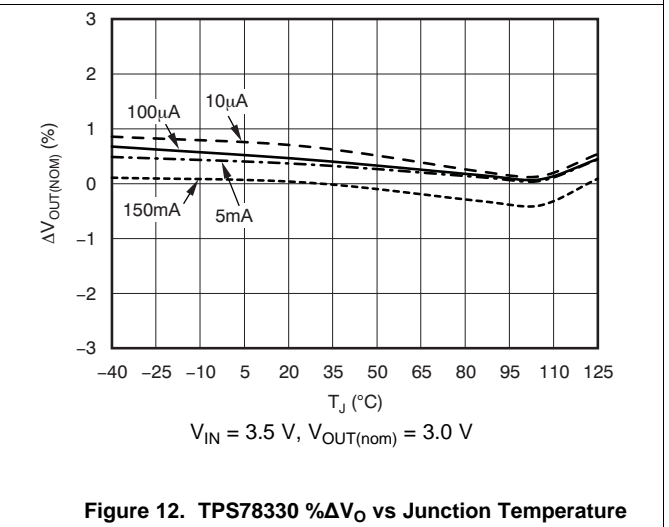


Figure 12. TPS78330  $\% \Delta V_O$  vs Junction Temperature

Typical Characteristics (continued)

At  $T_J = -40^\circ\text{C}$  to  $105^\circ\text{C}$ ,  $V_{IN} = V_{OUT(nom)} + 0.5\text{ V}$  or  $2.2\text{ V}$ , whichever is greater;  $I_{OUT} = 100\ \mu\text{A}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 1\ \mu\text{F}$ , and  $C_{IN} = 1\ \mu\text{F}$  (unless otherwise noted).

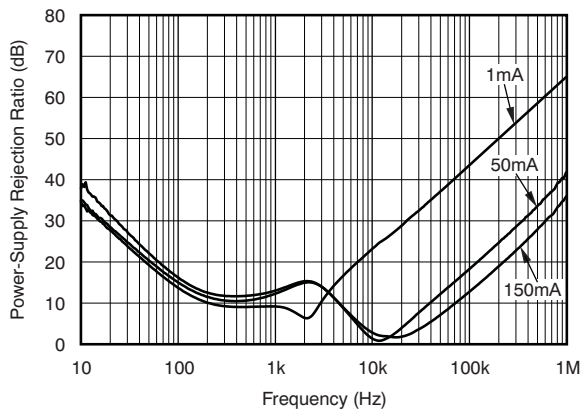


Figure 13. TPS78330 Ripple Rejection vs Frequency

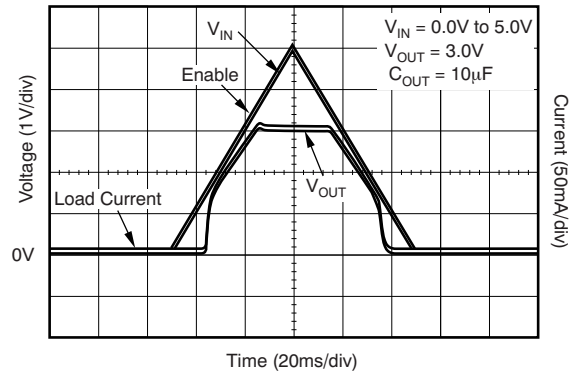


Figure 14. TPS78330 Input Voltage Ramp vs Output Voltage

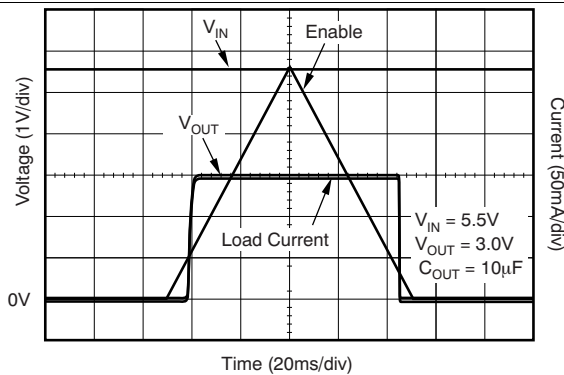


Figure 15. TPS78330 Output Voltage vs Enable (Slow Ramp)

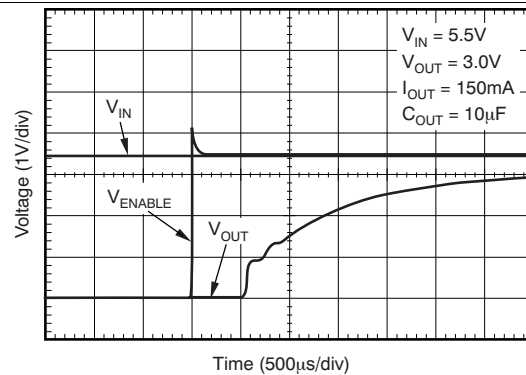


Figure 16. TPS78330 Input Voltage vs Delay to Output

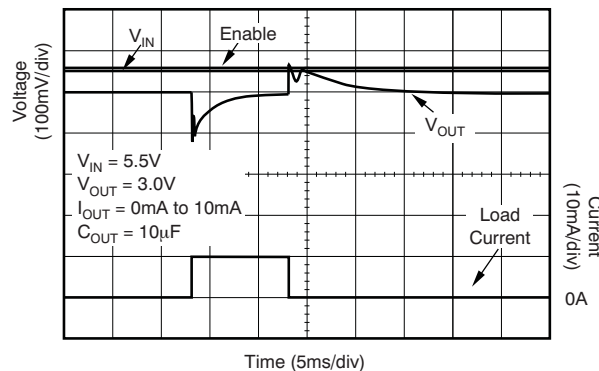


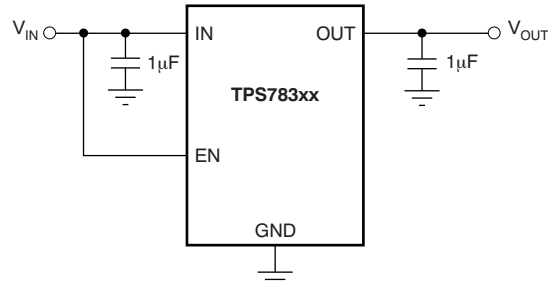
Figure 17. TPS78330 Load Transient Response



## Feature Description (continued)

### 7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage CMOS levels. When shutdown capability is not required, connect EN to the IN pin, as shown in [Figure 18](#).



**Figure 18. Circuit Showing EN Tied High When Shutdown Capability is Not Required**

## 7.4 Device Functional Modes

[Table 1](#) provides a quick comparison between the normal, dropout, and disabled modes of operation.

**Table 1. Device Functional Mode Comparison**

OPERATING MODE	PARAMETER			
	V <sub>IN</sub>	EN	I <sub>OUT</sub>	T <sub>J</sub>
Normal	V <sub>IN</sub> > V <sub>OUT(nom)</sub> + V <sub>DO</sub>	V <sub>EN</sub> > V <sub>EN(HI)</sub>	I <sub>OUT</sub> < I <sub>LIM</sub>	T <sub>J</sub> < 160°C
Dropout	V <sub>IN</sub> < V <sub>OUT(nom)</sub> + V <sub>DO</sub>	V <sub>EN</sub> > V <sub>EN(HI)</sub>	I <sub>OUT</sub> < I <sub>LIM</sub>	T <sub>J</sub> < 160°C
Disabled	—	V <sub>EN</sub> < V <sub>EN(LO)</sub>	—	T <sub>J</sub> > 160°C

### 7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage (V<sub>OUT(nom)</sub> + V<sub>DO</sub>).
- The enable voltage has previously exceeded the enable rising threshold voltage (V<sub>EN</sub> > V<sub>EN(HI)</sub>) and not yet decreased below the enable falling threshold.
- The output current is less than the current limit (I<sub>OUT</sub> < I<sub>LIM</sub>).
- The device junction temperature is less than the thermal shutdown temperature (T<sub>J</sub> < 160°C).

### 7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

### 7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage (V<sub>EN</sub> < V<sub>EN(LO)</sub>) or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature (T<sub>J</sub> > 160°C).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS783 family of LDOs is factory-programmable to have a fixed output. Note that during startup or steady-state conditions, do not allow the EN pin voltage to exceed  $V_{IN} + 0.3\text{ V}$ .

### 8.2 Typical Application

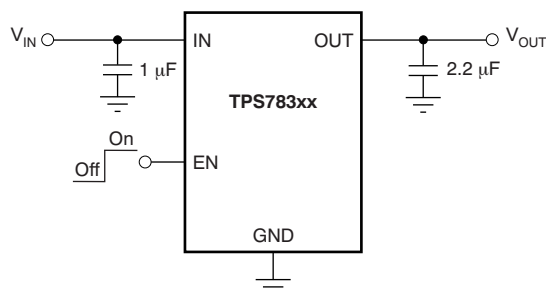


Figure 19. Providing a Low-Power Standby Rail

#### 8.2.1 Design Requirements

##### 8.2.1.1 Input and Output Capacitor Requirements

A 0.1- $\mu\text{F}$  input capacitor is necessary for stable operation. Good analog design practice is to connect a 0.1- $\mu\text{F}$  to 1.0- $\mu\text{F}$ , low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located near the power source.

The TPS783 family is designed to be stable with standard ceramic capacitors with values of 1.0  $\mu\text{F}$  or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1.0  $\Omega$ . With tolerance and dc bias effects, the minimum capacitance for stable operation is 1  $\mu\text{F}$ .

## Typical Application (continued)

### 8.2.1.2 Dropout Voltage

The TPS783 family uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  approximately scales with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as  $(V_{IN} - V_{OUT})$  approaches dropout. This effect is shown in the [Typical Characteristics](#) section. Refer to application report [SLVA207, Understanding LDO Dropout](#), available for download from [www.ti.com](#).

### 8.2.1.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response. For more information, see [Figure 17](#).

### 8.2.1.4 Minimum Load

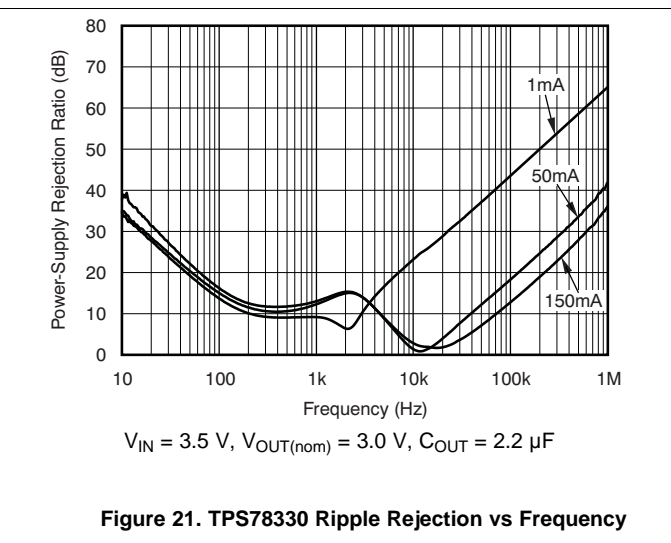
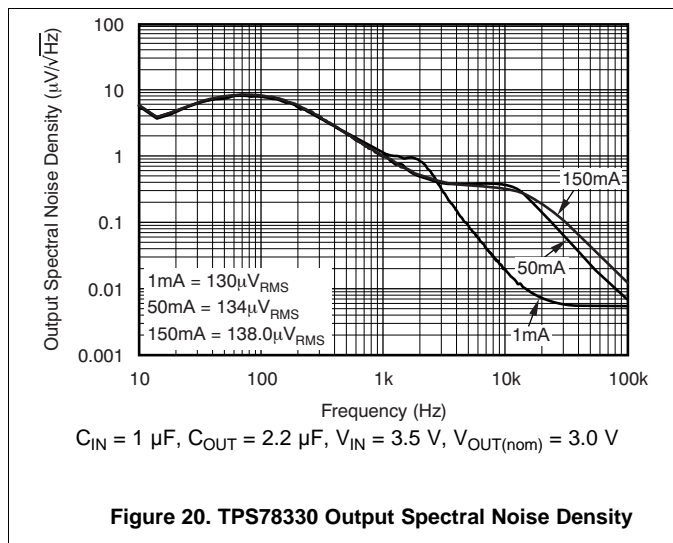
The TPS783 family is stable with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS783 employs an innovative, low-current circuit under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current. See [Figure 17](#) for the load transient response.

## 8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to account for dropout and output current to account for the GND pin current, and power the load. Select input and output capacitors based on application needs.

## 8.2.3 Application Curves



### 8.3 System Examples

The TPS783 family is designed to be compatible with low-power microprocessors and microcontrollers such as the TI MSP430. In particular, the ultralow quiescent current allows for the TPS783 family to be used in battery-powered applications.

When the system is active, a voltage supervisor enables the regulator and puts the MSP430 into active mode when there is a battery installed and its voltage is above a certain threshold, as shown in Figure 22. The dashed red line indicates the ground current.

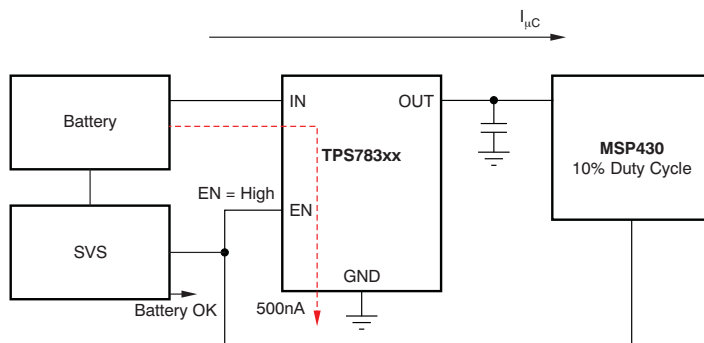


Figure 22. MSP430 Application in Active Mode

When the battery is depleted, the voltage supervisor signals to replace the system battery. After the battery is removed, the voltage supervisor disables the regulator and signals the MSP430 to go into low-power mode. At this moment, the output capacitor functions as a power supply for the MSP430 during the absence of the battery while it is being replaced, as Figure 23 illustrates. The dashed red line indicates the ground current.

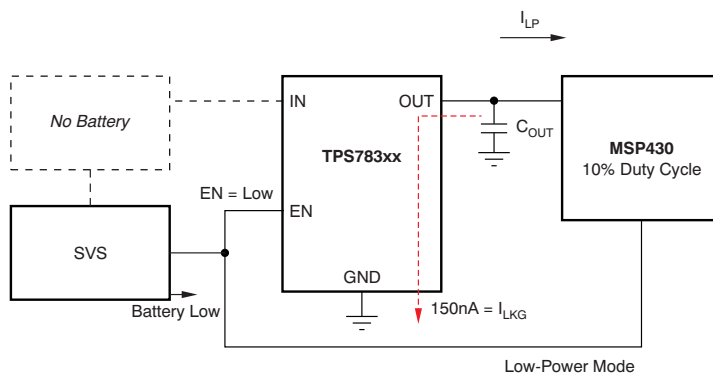


Figure 23. MSP430 Application While Battery is Replaced

Equation 1 shows how to find the required value of the output capacitor ( $C_{OUT}$ ) to provide an appropriate voltage level to the MSP430 for a given amount of time. This time varies from a few seconds to a few minutes, depending on several factors.

$$C_{OUT} = \frac{t_{MAX}}{\left[ \frac{V_{OUT(Nom)} - V_{MIN}}{I_{LKG} + I_{LP}} \right]}$$

where

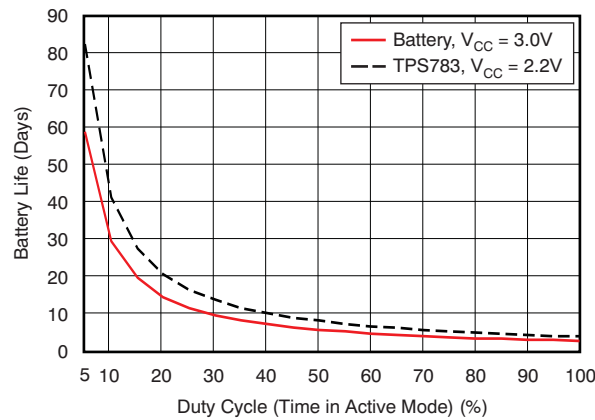
- $t_{MAX}$  = maximum time to replace depleted battery
- $V_{OUT(nom)}$  = nominal regulator output equal to initial voltage of capacitor when regulator is disabled
- $V_{MIN}$  = minimum voltage required by MSP430
- $I_{(LKG)}$  = leakage current into regulator output
- $I_{(LP)}$  = current demand from MSP430 in low-power mode

(1)

## System Examples (continued)

### 8.3.1 Extending Battery Life in *Keep-Alive* Circuitry Applications for MSP430 and Other Low-Power Microcontrollers

One of the primary advantages of a low quiescent current LDO is the extremely low energy requirement. Counter-intuitively, this requirement enables a longer battery life compared to using only the battery as an unregulated voltage supply for low-power microcontrollers, such as the MSP430. [Figure 24](#) illustrates the characteristic performance of an unregulated, 3.0-V battery supply versus a regulated TPS783 supply for a typical MSP430 application. [Table 2](#) summarizes this comparison.



Calculated with an MSP430F model, operating at 6 MHz.

**Figure 24. Battery Life Comparison vs Duty Cycle for MSP430 Application**

**Table 2. Battery Life Comparison vs Active Mode Time for MSP430 Application**

ACTIVE DUTY CYCLE	TPS783xx (NO. OF DAYS)	BATTERY ONLY (NO. OF DAYS)	1- $\mu$ A LDO (NO. OF DAYS)
Active mode, 1 sec/hour (0.028% duty cycle)	5742	6286	4373
Active mode, 10 sec/hour (0.28% duty cycle)	1320	998	1085
Active mode, 100 sec/hour (2.8% duty cycle)	151	106	148
Active mode, 1000 sec/hour (28% duty cycle)	15.4	10.7	15.4
Active mode, on all the time (100% duty cycle)	4.2	3.0	4.2
CONDITIONS			
Efficiency with V <sub>BAT</sub> = 3.0 V and V <sub>CC</sub> = 2.2 V (V <sub>OUT</sub> /V <sub>IN</sub> )	73%	100%	73%
LDO quiescent current (I <sub>Q</sub> )	0.5 $\mu$ A	0	1 $\mu$ A
MSP430 active current	2.19 mA	3.09 mA	2.19 mA
MSP430 low-power current	0.5 $\mu$ A	0.6 $\mu$ A	0.5 $\mu$ A

### 8.3.2 Supercapacitor-Based Backup Power

The very-low leakage current at the LDO output provides a system with the flexibility to use the device output capacitor, or supercapacitor, as a temporary backup power supply. The leakage current going into the regulator output from the output capacitor when the LDO is disabled is typically 170 nA; see [Figure 10](#).

## 8.4 Do's and Don'ts

Do place at least one 1- $\mu$ F ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

Do connect a 0.1- $\mu$ F to 1.0- $\mu$ F low equivalent series resistance (ESR) capacitor across the IN pin and GND of the regulator.

Do not exceed the absolute maximum ratings.

## 9 Power-Supply Recommendations

For best performance, connect a low-output impedance power supply directly to the IN pin of the TPS783. Inductive impedances between the input supply and the IN pin create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor.

## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), design the printed circuit board (PCB) with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with each ground plane connected only at the GND pin of the device. In addition, the output capacitor must be as close as possible to the ground pin of the device to provide a common reference for regulation purposes. High ESR capacitors may degrade PSRR.

#### 10.1.2 Package Mounting

Solder pad footprint recommendations for the TPS783 series are available from the Texas Instruments website at [www.ti.com](http://www.ti.com) through the [TPS783 family](#) product folders.

#### 10.1.3 Thermal Information

##### 10.1.3.1 Thermal Protection

Thermal protection disables the device output when the junction temperature rises to approximately 160°C, allowing the device to cool. After the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to 105°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TPS783 family is designed to protect against overload conditions. However, this circuitry is not intended to replace proper heatsinking. Continuously running the TPS783 series into thermal shutdown degrades device reliability.

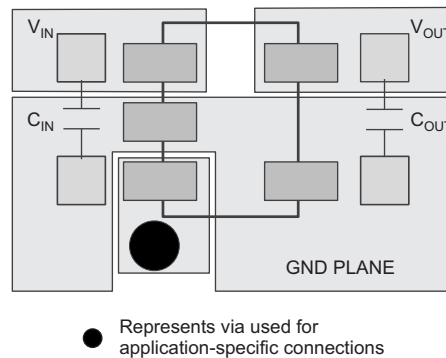
## Layout Guidelines (continued)

### 10.1.3.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current times the voltage drop across the output pass element ( $V_{IN}$  to  $V_{OUT}$ ), as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

## 10.2 Layout Example



**Figure 25. TPS783xx Layout Example**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS783. The [TPS782xxEVM evaluation modules](#) (and [related user guide](#)) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#).

##### 11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS783 is available through the product folders under *Simulation Models*.

#### 11.1.2 Device Nomenclature

**Table 3. Device Nomenclature<sup>(1)</sup>**

PRODUCT	V <sub>OUT</sub>
TPS783xxyyyz	XX is the nominal output voltage YYY is the package designator. Z is the tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### 11.2 Trademarks

All trademarks are the property of their respective owners.

### 11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS78318DDCR</a>	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO
TPS78318DDCR.A	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO
<a href="#">TPS78318DDCT</a>	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO
TPS78318DDCT.A	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO
TPS78318DDCTG4	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO
TPS78318DDCTG4.A	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIO
<a href="#">TPS78319DDCR</a>	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP
TPS78319DDCR.A	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP
<a href="#">TPS78319DDCT</a>	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP
TPS78319DDCT.A	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIP
<a href="#">TPS78326DDCR</a>	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB
TPS78326DDCR.A	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB
<a href="#">TPS78326DDCT</a>	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB
TPS78326DDCT.A	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIB
<a href="#">TPS78330DDCR</a>	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ
TPS78330DDCR.A	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS78330DDCRG4	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ
TPS78330DDCRG4.A	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ
<a href="#">TPS78330DDCT</a>	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ
TPS78330DDCT.A	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	DAZ
<a href="#">TPS78342DDCR</a>	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIQ
TPS78342DDCR.A	Active	Production	SOT-23-THIN (DDC)   5	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIQ
<a href="#">TPS78342DDCT</a>	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIQ
TPS78342DDCT.A	Active	Production	SOT-23-THIN (DDC)   5	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	SIQ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

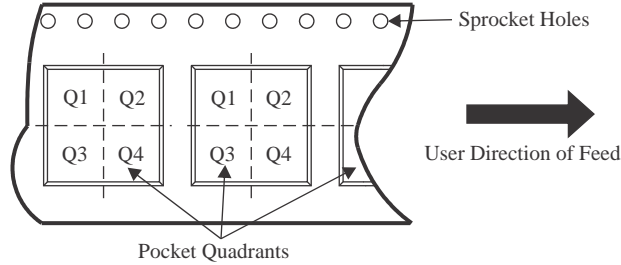
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

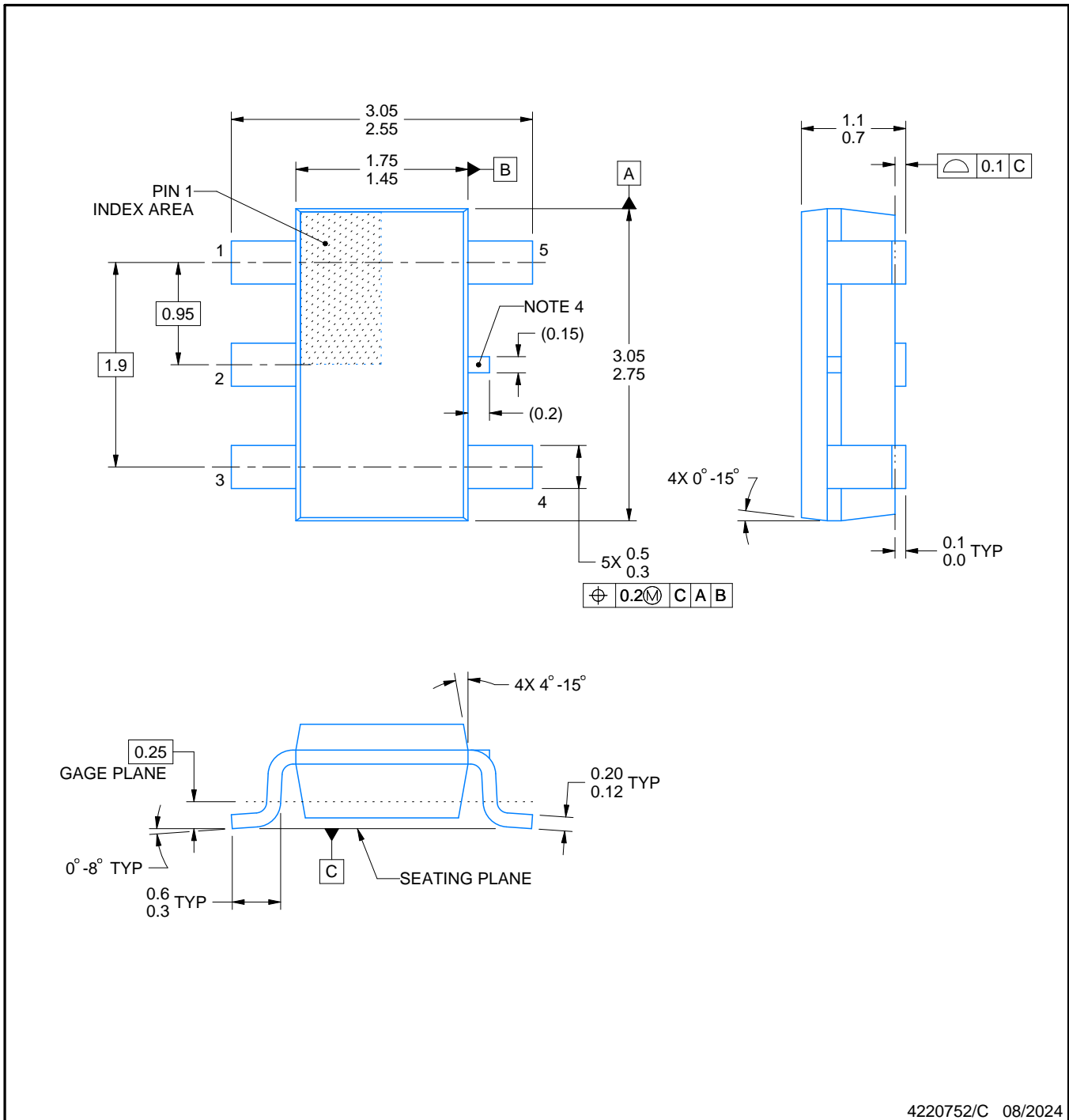
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78318DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78318DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78318DDCTG4	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78319DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78319DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78326DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78326DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78330DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78330DDCRG4	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS78330DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78342DDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS78342DDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS78318DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78318DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS78318DDCTG4	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS78319DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78319DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS78326DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78326DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS78330DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78330DDCRG4	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78330DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS78342DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS78342DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0



4220752/C 08/2024

NOTES:

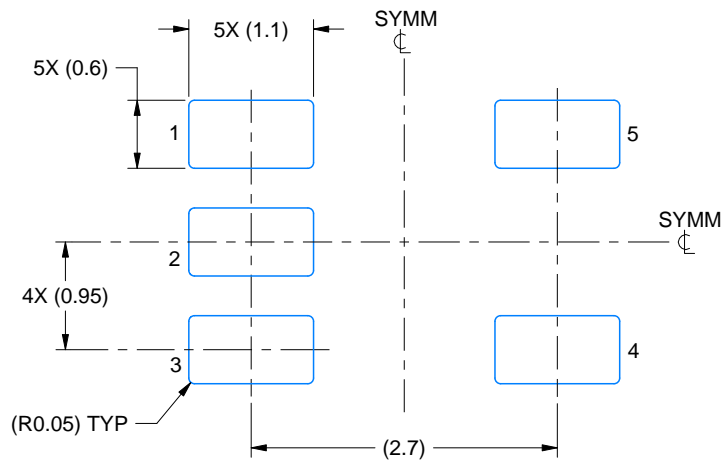
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

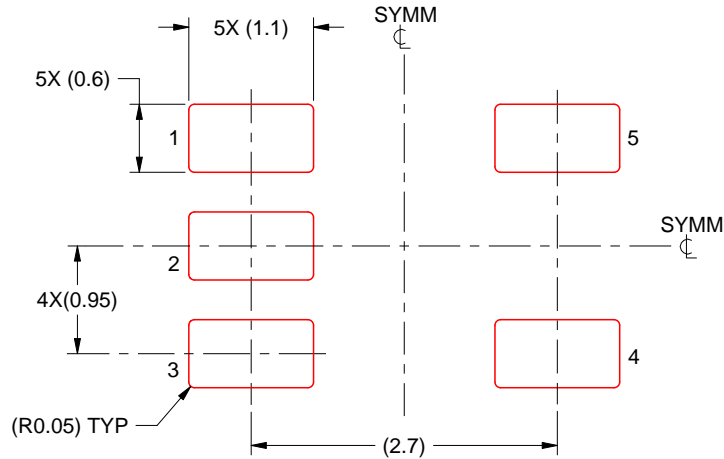
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated