AM261x Sitara™ Microcontrollers

1 Features

Processor Cores:

- Single and Dual Arm® Cortex® R5F CPU with each core running up to 500MHz
  - 16KB I-Cache with 64-bit ECC per CPU core
  - 16KB D-cache with 32-bit ECC per CPU core
  - 256KB Tightly Coupled Memory (TCM) with 32-bit ECC per core
  - Lockstep or Dual-core operation supported
- Trigonometric Math Unit (TMU) for accelerating trigonometric functions
  - Up to 2x, one per R5F MCU core

Memory:

- 1.5MB of On-Chip Shared RAM (OCSRAM):
  - 3 banks × 512KB
  - ECC error protection for full 1.5MB OCSRAM
  - Remote L2 Cache (RL2) for external memory, software programmable up to 256KB per CPU core
- 2x Octal Serial Peripheral Interface (OSPI) up to 133MHz SDR and DDR
  - 1x with eXecute In Place (XIP) support
  - RAM expansion/Flash over the Air (FOTA)
- General-Purpose Memory Controller (GPMC)
  - 16-bit parallel data bus with 22-bit address bus and 4 chip selects
  - Up to 4MB addressable memory space
  - Integrated Error Location Module (ELM) support for error checking

System on Chip (SoC) Services and Architecture:

- 1x EDMA to support data movement functions
- Device Boot supported from the following interfaces:
  - UART (Primary/Backup)
  - OSPI NOR and NAND Flash (50MHz SDR and 25MHz DDR) (Primary)
  - USB Peripheral boot
- Interprocessor communication modules
  - SPINLOCK module for synchronizing processes running on multiple cores
  - MAILBOX functionality implemented through CTRLMMR registers
- Central Platform Time Sync (CPTS) support with time-sync and compare-event interrupt routers
- Timer Modules:
  - 2x Windowed Watchdog Timer (WWDT)
  - 4x Real Time Interrupt (RTI) timer

USB 2.0

- Port configurable as USB host, USB device, or USB Dual-Role device
- USB 2.0 Host mode
  - High-Speed (HS, 480Mbps)
  - Full-Speed (FS, 12Mbps)
  - Low-Speed (LS, 1.5Mbps)
- USB 2.0 Device mode
  - High-Speed (HS, 480Mbps)
  - Full-Speed (FS, 12Mbps)

Industrial Connectivity:

- 2x Programmable Real-time Unit – Industrial Communication Subsystem (PRU-ICSS)
  - Dual core Programmable Realtime Unit Subsystem (PRU0 / PRU1) per PRU-ICSS for 4 cores total
    - Deterministic hardware
    - Dynamic firmware
  - 20-channel enhanced input (eGPI) per PRU
  - 20-channel enhanced output (eGPO) per PRU
  - Embedded Peripherals and Memory
    - 1x UART, 1x ECAP, 1x MDIO, 1x IEP
    - 1x 32KB Shared General Purpose RAM
    - 2x 8KB Shared Data RAM
    - 1x 12KB IRAM per PRU
    - ScratchPad (SPAD), MAC/CRC
  - Digital encoder and sigma-delta control loops
  - The PRU-ICSS enables advanced industrial protocols including:
    - EtherCAT®, Ethernet/IP™
    - PROFINET®, IO-Link®
  - Dedicated Interrupt Controller (INTC)
  - Dynamic CONTROLSS XBAR Integration

High Speed Interfaces

- Integrated 3-port Gigabit Ethernet Switch (CPSW) supporting up to two external ports
  - Selectable MII (10/100), RMII (10/100), or RGMII (10/100/1000)
  - IEEE 1588 (2008 Annex D, Annex E, Annex F) with 802.1AS PTP
  - Clause 45 MDIO PHY management
  - 512x ALE engine based packet classifiers
  - Priority flow control with up to 2KB packet size
  - Four CPU hardware interrupt pacing
  - IP/ UDP/ TCP checksum offload in hardware
  - Time Sensitive Network (TSN) Support
  - Cut-thru switching and Interexpress Traffic (IET) support

General Connectivity:

- 6x Universal Asynchronous RX-TX (UART)
- 4x Serial Peripheral Interface (SPI) controllers
- 3x Local Interconnect Network (LIN) ports
- 3x Inter-Integrated Circuit (I2C) ports
- 2x Modular Controller Area Network (MCAN) modules with CAN-FD support
- 1x Fast Serial Interface Transmitter (FSITX)
- 1x Fast Serial Interface Receiver (FSIRX)
- Up to 141x General Purpose I/O (GPIO) pins

Sensing and Actuation:

- Real-time Control Subsystem (CONTROLSS)
- Flexible Input/Output Crossbars (XBAR)
- 3x 12-bit Analog to Digital Converters (ADC) with 3 MSPS maximum sampling rate
  - Each ADC module with
    - 7x Single ended channels **OR**
    - 3x Differential channels
  - Highly configurable ADC digital logic
    - With selectable internal or external reference
    - 4x Post-Processing blocks for each ADC module
- 9x Analog Comparators with internal 12-bit DAC reference (CMPSSA)
- 1x 12 bit Digital to Analog Converter (DAC)
- 10x Enhanced High Resolution Pulse Width Modulation (eHRPWM) modules
  - Single or Dual PWM channels
  - Advanced PWM Configurations
  - Enhanced HRPWM time resolution
- 8x Enhanced Capture (ECAP) modules
- 2x Enhanced Quadrature Encoder Pulse (EQEP) modules
- 2x Sigma-Delta Filter Modules (SDFM)

Data Storage

- 1 × 4-bit Multi-Media Card/Secure Digital (MMC/SD) interface

Security:

- Hardware Security Module (HSM) with support for Auto SHE 1.1/EVITA
- Targeted for ISO 21434 compliance
- Secure boot support
  - Device Take Over Protection
  - Hardware enforced root-of-trust
  - Authenticated boot
  - SW Anti-rollback protection
- Debug security
  - Secure device debug only after proper authentication
  - Ability to disable device debug functionality
- Device ID and Key Management
  - Support for OTP Memory (FUSEROM)
    - Store root keys and other security fields
  - Separate EFUSE controllers and FUSE ROMs
  - Unique Device Public Identifiers
- Memory Protection Units (MPU)
  - Dedicated Arm® MPU per Cortex®-R5F core
  - System MPU - present at various interfaces in the SoC (MPU or Firewall)
  - 8 to 16 Programmable Regions
    - Enable/Privilege ID
    - Start/End Address
    - Read/Write/Cachable
    - Secure/Non-Secure
- Cryptographic acceleration
  - Cryptographic cores with DMA Support
  - AES - 128/192/256-bit key sizes
  - SHA2 - 256/384/512-bit support
  - DRBG with pseudo and true random number generator

Functional Safety:

- Enables design of systems with functional safety requirements
  - Error Signaling Module (ESM)
  - ECC or parity on calculation critical memories
  - Built-In Self-Test (BIST) on-chip RAM
  - Runtime internal diagnostic modules including voltage, temperature, and clock monitoring, windowed watchdog timers, CRC engines for memory integrity checks
- Functional Safety-Compliant targeted [Industrial]
  - Developed for functional safety applications
  - Documentation to be made available to aid IEC 61508 functional safety system design
  - Systematic capability up to SIL-3 targeted
  - Hardware integrity up to SIL-3 targeted
  - Safety-related certification
    - IEC 61508 planned
- Functional Safety-Compliant targeted [Automotive]
  - Developed for functional safety applications
  - Documentation to be made available to aid ISO 26262 functional safety system design
  - Systematic capability up to ASIL-D targeted
  - Hardware integrity up to ASIL-D targeted
  - Safety-related certification
    - ISO 26262 planned

Technology / Package:

- AEC-Q100 qualified for automotive applications
- ZCZ Package
  - 324-pin NFBGAs
  - 15.00mm × 15.00mm
  - 0.8mm pitch
- ZFG Package
  - 304-pin NFBGA
  - 13.25mm × 13.25mm
  - 0.65mm pitch
- ZEJ Package
  - 256-pin NFBGA
  - 13.00mm × 13.00mm
  - 0.8mm pitch
- ZNC Package
  - 293-pin NFBGA
  - 10.00mm × 10.00mm
  - 0.5mm pitch

2 Applications

- AC Inverter
- Automotive Digital Power Conversion/Control
  - Battery Management Systems (BMS)
  - On-board Chargers, DC/DC Converters
- Humanoid robot
- Industrial and collaborative robot
- Industrial Digital Power Control
  - Energy storage systems
  - EV charging
  - String Inverters
- Mobile robot
- PLC, DCS and PAC
  - Communication Module
  - Digital input module
  - Digital output module
  - Stand-alone remote IO
- Remote I/O
- Single and multiaxis servo drives
- Telematics Control Unit

3 Description

The AM261x Sitara Arm® Microcontrollers are part of Sitara AM26x real-time MCU families designed to meet the complex real-time processing needs of next generation industrial and automotive embedded products. With scalable Arm Cortex® R5F performance and an extensive set of peripherals, AM261x device is designed for a broad range of applications while offering safety features and optimized peripherals for real time control.

Key features and benefits:

- Peripherals supporting system level connectivity such as Gigabit Ethernet, USB, OSPI/QSPI, CAN, UARTs, SPI and GPIOs.
- Granular firewalls managed by Hardware Security Manager (HSM) enable developers to implement stringent security minded system design requirements.
- Up to two R5F cores in cluster with 256KB of shared Tightly Coupled Memory (TCM) per core along with 1.5MB of shared SRAM, greatly reducing the need for external memory.

Package Information

Part Number(1) (2)	Package	Package Size(3)
AM261...ZCZ	ZCZ (nFBGA, 324)	15.00mm × 15.00mm
AM261...ZFG	ZFG (nFBGA, 304)	13.25mm × 13.25mm
AM261...ZEJ	ZEJ (nFBGA, 256)	13.00mm × 13.00mm
AM261...ZNC	ZNC (nFBGA, 293)	10.00mm × 10.00mm
AM261...ZCZQ1	ZCZQ1 (nFBGA, 324)	15.00mm × 15.00mm
AM261...ZEJQ1	ZEJQ1 (nFBGA, 256)	13.00mm × 13.00mm

(1) For more information, see Section 11.
(2) All devices are available in both tray or tape and reel packaging.
(3) The package size (length x width) is a nominal value and includes pins, where applicable.

3.1 Functional Block Diagram

AM261x Functional Block Diagram is the functional block diagram for this device.

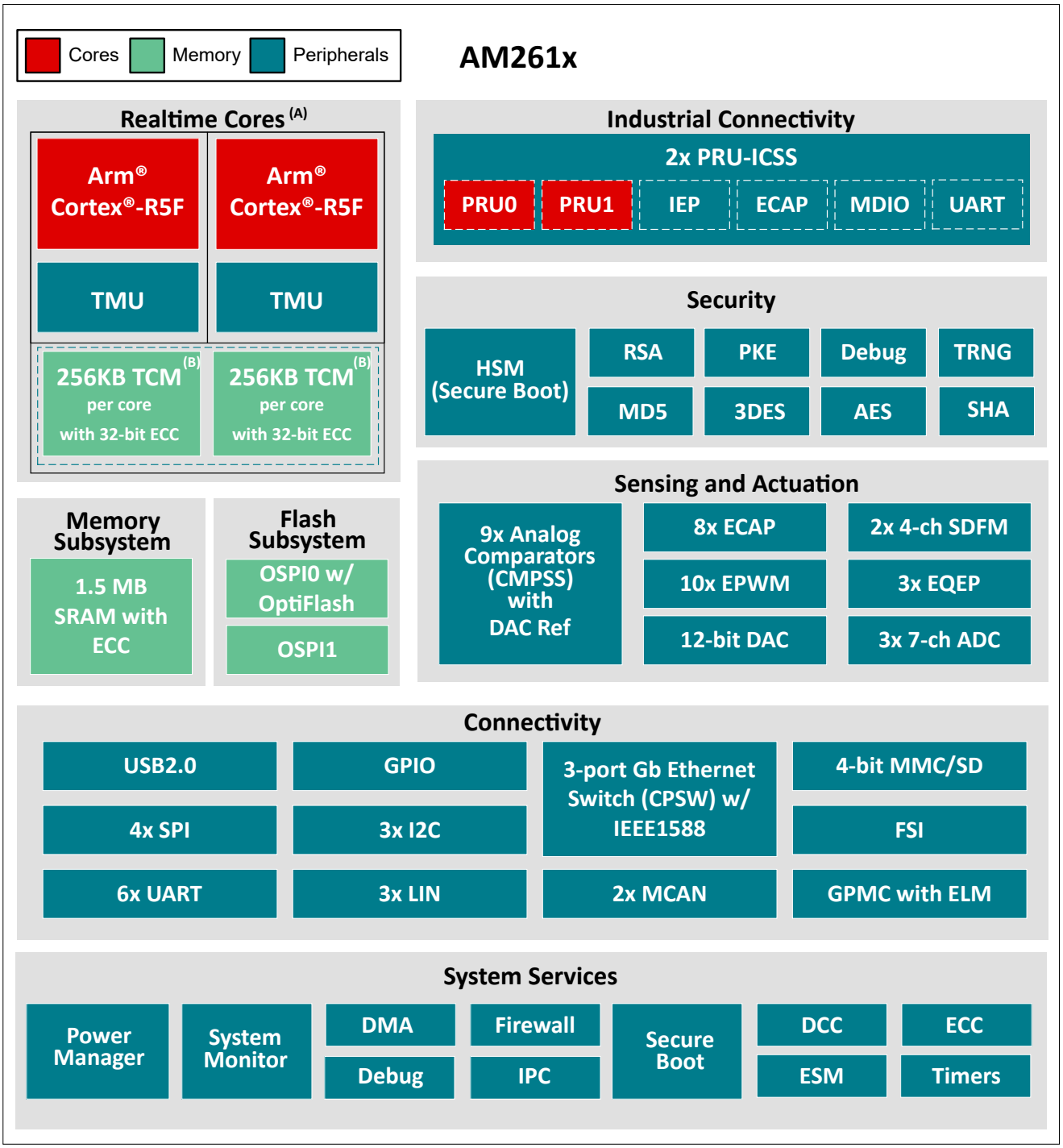


Figure 3-1. AM261x Functional Block Diagram

A. AM261x is available with two and one core options. Refer to the Package Comparison table for more peripheral specific details.
B. The R5F cluster supports 512KB of Tightly-Coupled Memory (TCM). When configured as Lockstep operating mode, individual cores can utilize all 512KB. While in Dual-Core mode, each core may only utilize its designated half (256KB TCM).

Table of Contents

4 Package Comparison

Table 4-1 shows a comparison between devices based on packages, highlighting the differences.

Table 4-1. Package Comparison

		Packages			
Features	**Reference Name**	**AM261...ZCZ AM261...ZCZ-Q1**	**AM261...ZFG**	**AM261...ZEJ AM261...ZEJ-Q1**	**AM261...ZNC**
PROCESSORS AND ACCELERATORS					
Speed Grade		Up to 500MHz, See Operating Performace Points for more details			
Arm® Cortex-R5F	R5FSS	AM261**2** and AM261**2**-Q1 : 2 cores (1× Dual Core with Lockstep option) AM261**1** and AM261**1**-Q1 : 1 core (Single Core)			
Trigonometric Math Unit	TMU	Yes			
Hardware Security Module	HSM	Yes			
Crypto Accelerators	Security	Yes			
PROGRAM AND DATA STORAGE					
On-Chip Shared Memory (RAM)	OCSRAM	Up to 1.5MB, See Operating Performace Points for more details			
R5F Tightly Coupled Memory (TCM)	TCM	Up to 512KB(1)			
PERIPHERALS					
Analog-to-Digital Converter	ADC	3x 6-ch	3x 7-ch		2x 7-ch
Comparator Modules	CMPSS	9			6
Gigabit Ethernet Interface	CPSW	Yes			
Digital-to-Analog Converter	DAC	1			
Enhanced Capture Module	ECAP	8			
Enhanced High Resolution Pulse Width Modulation	EHRPWM	10x 20-ch			
Enhanced Quadrature Encoder Pulse Module	EQEP	2			
Fast Serial Interface	FSI	1x FSI_RX + 1x FSI_TX			
General-Purpose I/O	GPIO	Up to 141 GPIOs		Up to 114 GPIOs	Up to 112 GPIOs
General-Purpose Memory Controller	GPMC	1		Not Available	
Inter-Integrated Circuit Interface	I2C	3			
Local Interconnect Network	LIN	3			
Modular Controller Area Network Iwith Full CAN_FD	MCAN	2			
Multi-Media Card/Secure Digital Interface	MMC-SD	1			Not Available
Octal SPI Flash Interface	OSPI	1x OSPI0 with OptiFlash and 1x OSPI1			
Programmable Real-Time Unit Subsystem	PRU	2(2)			
Industrial Communication Subsystem Support	PRU-ICSS	Optional			
Sigma Delta Filter Module	SDFM	2x 4-ch		1x 4-ch	3 channels total(3)
Serial Peripheral Interface	SPI	4			2(4)
Universal Asynchronous Receiver and Transmitter	UART	6			
Universal Serial Bus	USB 2.0	USB0 with external VBUS			
Miscellaneous					
Junction Temperature		Extended Automotive: –40°C to 150°C(5)			
		Extended Industrial: –40°C to 125°C(6)			
Automotive Qualification		AEC-Q100(7)			

(1) The R5FSS cluster supports 512KB of Tightly-Coupled Memory (TCM). When configured as Single-Core or Lockstep operating mode, individual cores can utilize the entire 512KB of TCM memory, while in Dual-Core mode, each core can only utilize its designated half (256KB TCM).
(2) AM261x supports 2 instances of the PRU Subsystem for a total of 4 real-time PRU cores.
(3) Instead of one or more full instances of the SDFM peripheral, the ZNC package devices have 3 SDFM channels: SDFM0_D2, SDFM1_D0, and SDFM1_D1.
(4) ZNC packages devices have SPI0 and SPI2 as useable SPI interfaces.
(5) Extended Automotive temperature is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the Nomenclature Description table.
(6) Extended Industrial temperature is applicable to select part number variants as indicated by the lack of the Automotive Designator (Q1) identifier in the Nomenclature Description table.

(7) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the Nomenclature Description table.

4.1 Device Identification

Device Identification below details the specific JTAG_USER_ID and feature sets available for AM261x devices across packages per OPN. Please see Device Nomenclature for more information.

Table 4-2. Device Identification

Orderable Part Number (OPN)[1]	JTAG_USER_ID	R5F	PRU-ICSS	EtherCAT	Integrated Stacks	Speed[2]
ZCZ, 15.00mm × 15.00mm						
AM2612AOFFHMZCZR	0x5908 DBFE	2	x	x	x	500MHz
AM2612ALDFHMZCZRQ1	0x5908 9B3E		x			400MHz
AM2612APDFHMZCZRQ1	0x5908 9C3E		x			200MHz
AM2611AOFFHIZCZR	0x5904 DBFE	1	x	x	x	500MHz
ZFG, 13.25mm × 13.25mm						
AM2612AOFFHIZFGR	0x5908 DBEA	2	x	x	x	500MHz
AM2612AOEFHIZFGR	0x5908 BBEA		x	x		
AM2612AODFHIZFGR	0x5908 9BEA		x			
AM2611AOFFHIZFGR	0x5904 DBEA	1	x	x	x	
AM2611AOEFHIZFGR	0x5904 BBEA		x	x		
AM2611AODFHIZFGR	0x5904 9BEA		x			
ZEJ, 13.00mm × 13.00mm						
AM2612AOFFHIZEJR	0x5908 DBEC	2	x	x	x	500MHz
AM2612AOEFHIZEJR	0x5908 BBEC		x	x		
AM2612AODFHIZEJR	0x5908 9BEC		x			
AM2612ALDFHMZEJRQ1	0x5908 9B3C		x			400MHz
AM2612APDFHMZEJRQ1	0x5908 9C3C		x			200MHz
AM2611AOFFHIZEJR	0x5904 9BEC	1	x	x	x	500MHz
AM2611AOEFHIZEJR	0x5904 9BEC		x	x		
AM2611AODFHIZEJR	0x5904 9BEC		x			
AM2611ALDFHMZEJRQ1	0x5904 9B3C		x			400MHz
AM2611APDFHMZEJRQ1	0x5904 9C3C		x			200MHz
ZNC, 10.00mm × 10.00mm						
AM2612AOFFHIZNCR	0x5908 DBE9	2	x	x	x	500MHz
AM2612AOEFHIZNCR	0x5908 BBE9		x	x		
AM2612AODFHIZNCR	0x5908 9BE9		x			
AM2611AOFFHIZNCR	0x5904 DBE9	1	x	x	x	
AM2611AOEFHIZNCR	0x5904 BBE9		x	x		
AM2611AODFHIZNCR	0x5904 9BE9		x			

(1) Planned values. Please see Mechanical, Packaging, and Orderable Information for released OPNs.
(2) See Operating Performace Points for more details

4.2 Related Products

Sitara™ Microcontrollers Family of Arm® Cortex®-R based high performance microcontrollers with advanced networking, real-time control, and signal processing accelerators to meet emerging MCU requirements for industrial and automotive applications.

Sitara™ Microcontrollers - Evaluation Modules TI provides device-specific Evaluation Module (EVM) designs to help kick-start product development. See the LP-AM261 and AM261-SOM-EVM for more information.

MCU-PLUS_SDK_AM261X The AM261x microcontroller (MCU) plus software development kit (SDK) is a unified software platform for embedded processors providing easy setup and fast out-of-the-box access to examples, benchmarks and demonstrations. This software accelerates application development schedules by eliminating creating basic system software functions from scratch.

Products to complete your design The following list of products are frequently purchased or used in conjunction with the AM261x device to meet your system design requirements.

- **TPS65036x-Q1** - Functional safety-compliant multi-rail power supply for safety MCUs applications.
- **TPS3704-Q1** - Automotive multichannel window supervisor with very-high accuracy and compact form factor.
- **DP83TG720S-Q1** - 1000BASE-T1 automotive Ethernet PHY with RGMII.
- **DP83826E** - Low latency 10/100Mbps Ethernet PHY with MII interface and enhanced mode.
- DP83869HM - Extended temperature, high-immunity gigabit Ethernet PHY transceiver with copper & fiber interface.
- **TCAN1042H-Q1** - Automotive 70V bus-fault-protected CAN transceiver with flexible data-rate.

5 Terminal Configuration and Functions

5.1 Pin Diagram

Note

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

The diagrams in this section are used in conjunction with the other Terminal Configuration and Functions tables to locate signal names and ball grid numbers.

5.1.1 AM261x ZCZ Pin Diagram

AM261x ZCZ Pin Diagram

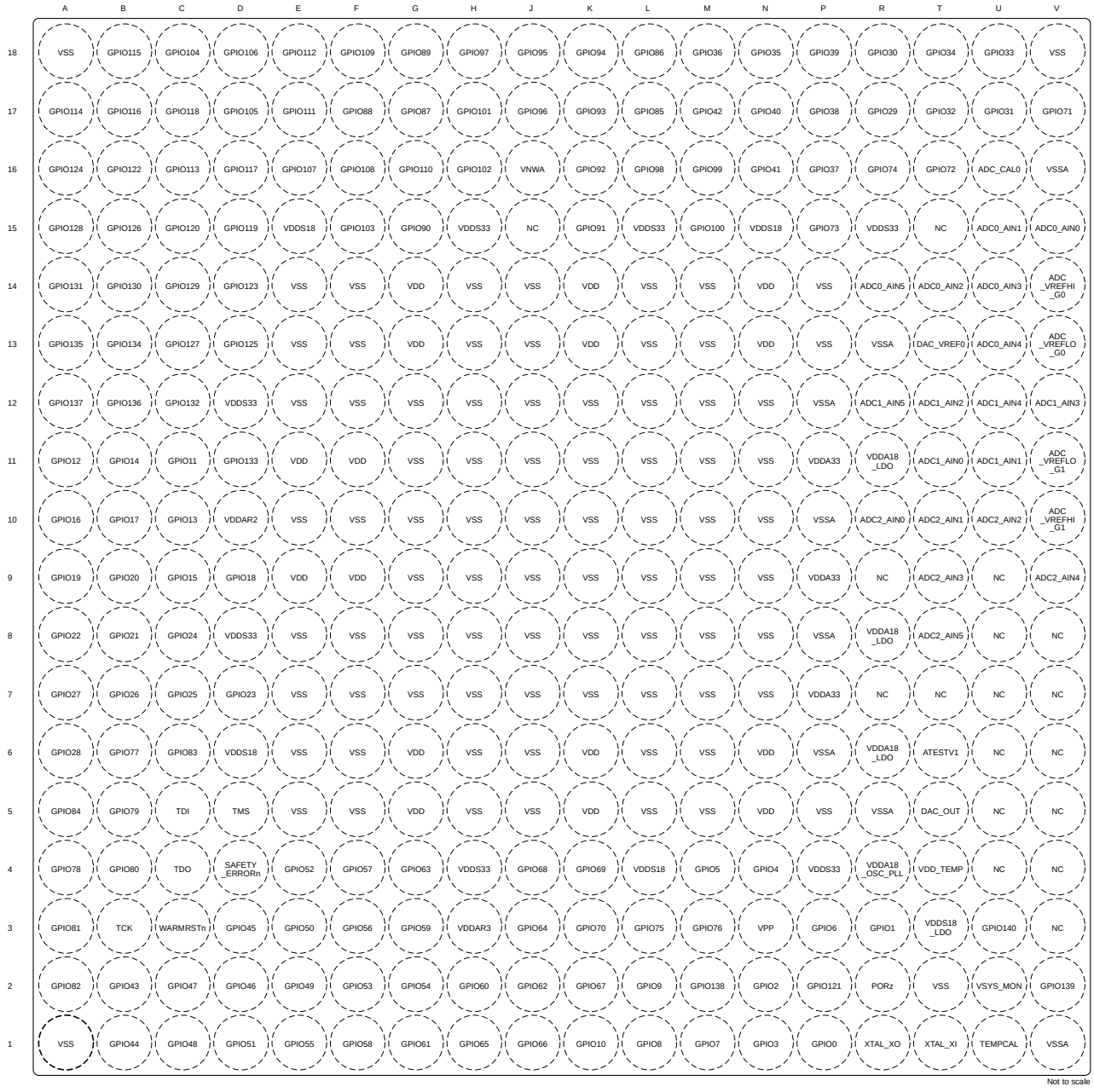


Figure 5-1. AM261x ZCZ Pin Diagram

5.1.2 AM261x ZFG Pin Diagram

AM261x ZFG Pin Diagram

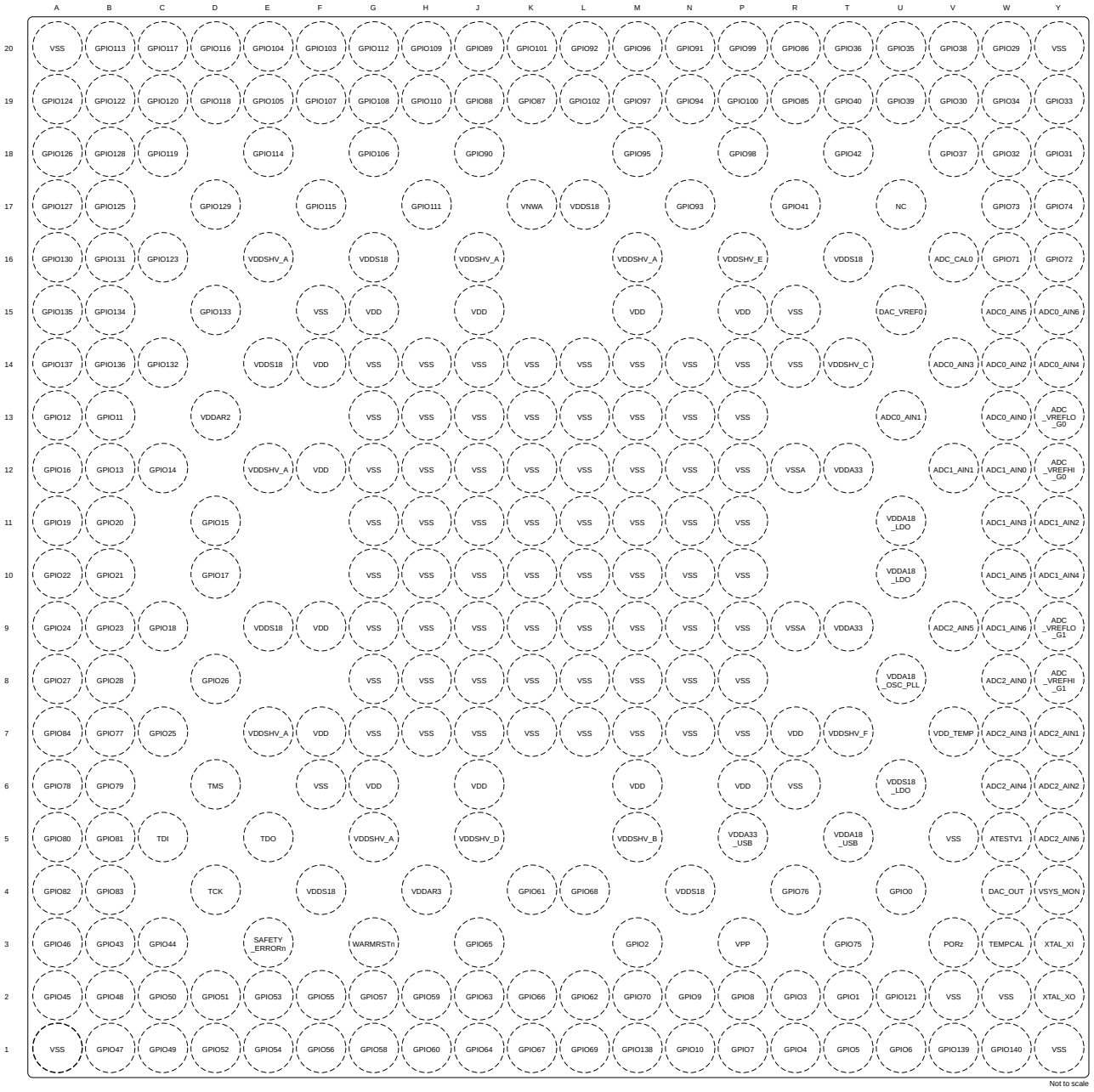


Figure 5-2. AM261x ZFG Pin Diagram

5.1.3 AM261x ZEJ Pin Diagram

AM261x ZEJ Pin Diagram

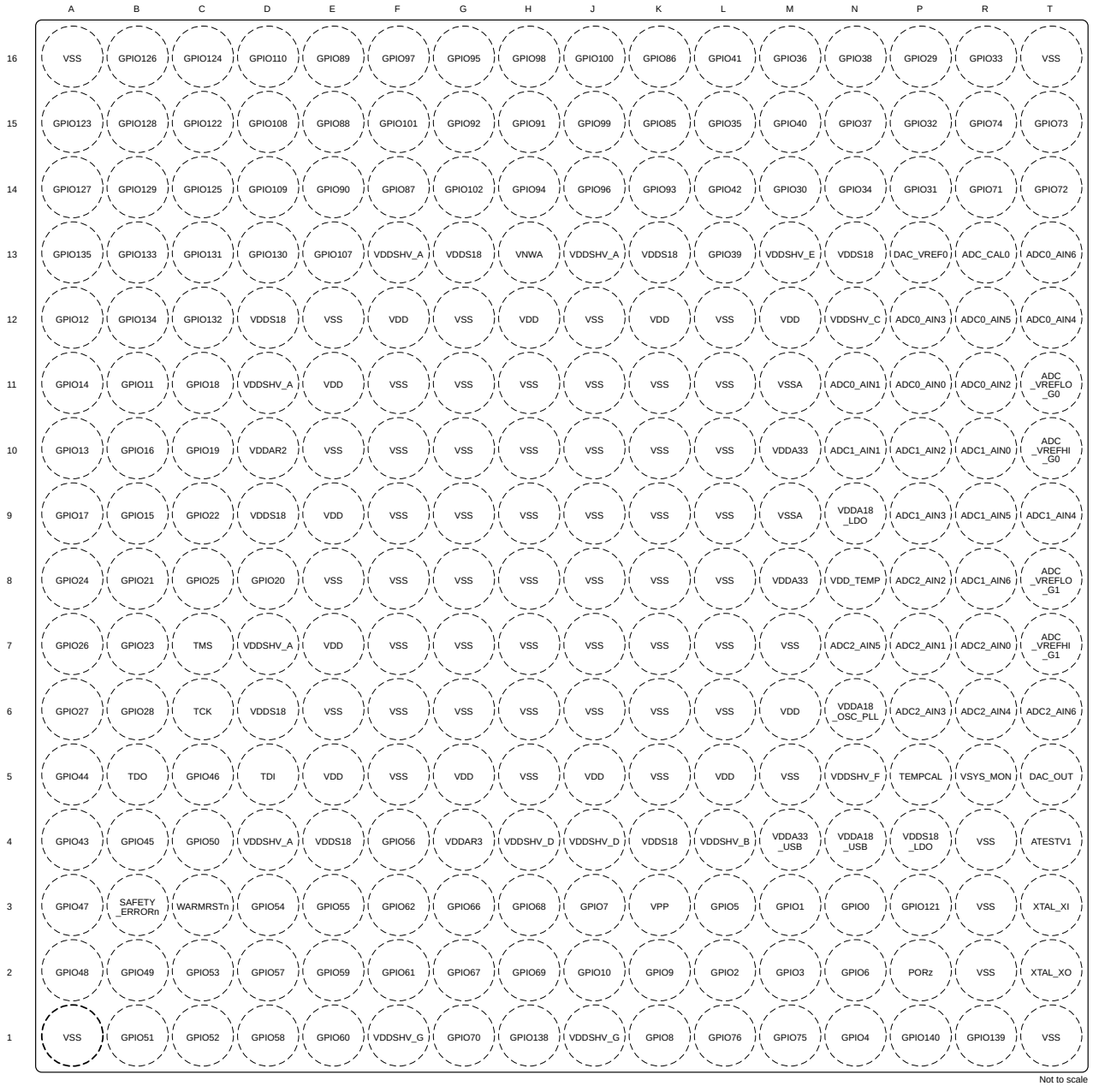


Figure 5-3. AM261x ZEJ Pin Diagram

5.1.4 AM261x ZNC Pin Diagram

AM261x ZNC Pin Diagram

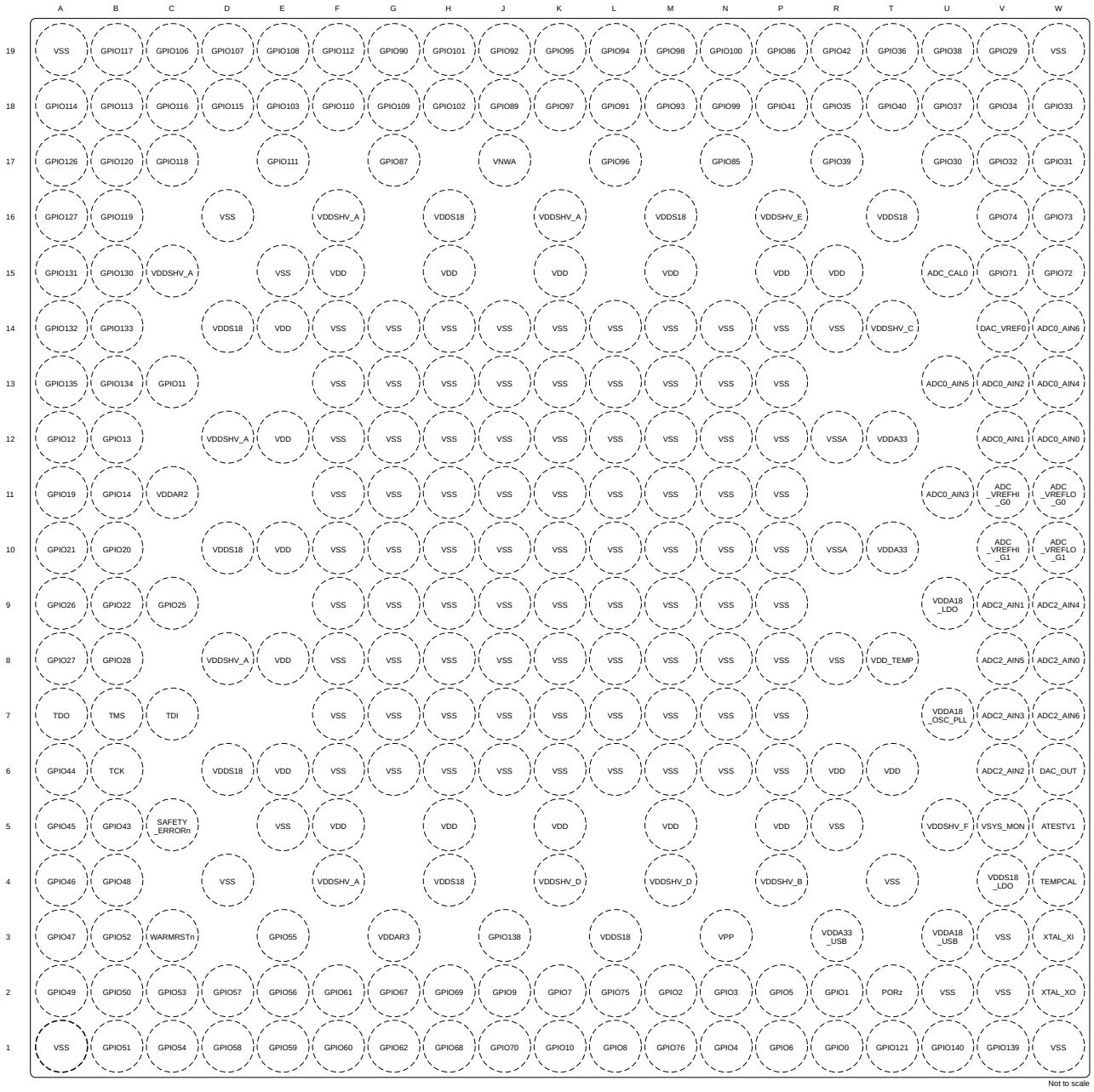


Figure 5-4. AM261x ZNC Pin Diagram

5.2 Pin Attributes

The following list describes the contents of each column in the *Pin Attributes* table:

1. **Ball Number:** Ball numbers assigned to each terminal of the Ball Grid Array package.
2. **Ball Name:** Ball name assigned to each terminal of the Ball Grid Array package (this name is typically taken from the primary MUXMODE 0 signal function).
3. **Signal Name:** Signal name of all dedicated and pin multiplexed signal functions associated with a ball.

Note

The *Pin Attributes* table, defines the SoC pin multiplexed signal function implemented at the pin and **does not** define secondary multiplexing of signal functions implemented in device subsystems. Secondary multiplexing of signal functions are not described in this table. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

4. **Mux Mode:** The MUXMODE value associated with each pin multiplexed signal function:
   - MUXMODE 7 is the primary pin multiplexed signal function. However, the primary pin multiplexed signal function is not necessarily the default pin multiplexed signal function.
   - MUXMODE values 1 through 15 are possible for pin multiplexed signal functions. However, not all MUXMODE values have been implemented. The only valid MUXMODE values are those defined as pin multiplexed signal functions within the Pin Attributes table. Only defined valid values of MUXMODE can be used.
   - Bootstrap defines SOC configuration pins, where the logic state applied to each pin is latched on the rising edge of PORz. These input signal functions are fixed to their respective pins and are not programmable via MUXMODE.
   - An empty box or "-" means Not Applicable.

Note

- The value found in the MUX MODE AFTER RESET column defines the default pin multiplexed signal function selected when PORz is deasserted.
- Configuring two pins to the same pin multiplexed signal function can yield unexpected results and is not supported. This can be prevented with proper software configuration.
- Configuring a pad to an undefined multiplexing mode results in undefined behavior and must be avoided.

5. **Type:** Signal type and direction:
   - I = Input
   - O = Output
   - ID = Input, with open-drain output function
   - OD = Output, with open-drain output function
   - IO = Input, Output, or simultaneously Input and Output
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
6. **Ball State During Reset (RX/TX/PULL):** State of the terminal while PORz is asserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.

  - On: The input buffer is **enabled**.
- TX (Output buffer)
  - Off: The output buffer is **disabled**.
  - Low: The output buffer is **enabled** and drives V_{OL}.
- PULL (Internal pull resistors)
  - Off: Internal pull resistors are turned **off.**
  - Up: Internal **pull-up** resistor is turned on.
  - Down: Internal **pull-down** resistor is turned on.
  - NA: No internal pull resistor.
- An empty box, or "-" means Not Applicable.

7. **Ball State After Reset (RX/TX/PULL):** State of the terminal after PORz is deasserted, where RX defines the state of the input buffer, TX defines the state of the output buffer, and PULL defines the state of internal pull resistors:
   - RX (Input buffer)
     - Off: The input buffer is **disabled**.
     - On: The input buffer is **enabled**.
   - TX (Output buffer)
     - Off: The output buffer is **disabled**.
     - SS: The subsystem selected with MUXMODE determines the output buffer state.
   - PULL (Internal pull resistors)
     - Off: Internal pull resistors are turned **off.**
     - Up: Internal **pull-up resistor** is turned on.
     - Down: Internal **pull-down resistor** is turned on.
     - NA: No internal pull resistor.
   - An empty box, NA, or "-" means Not Applicable.
8. **Mux Mode After Reset:** The value found in this column defines the **default** pin multiplexed signal function after PORz is deasserted.
   - An empty box, NA, or "-" means Not Applicable.
9. **I/O Voltage**: This column describes I/O **operating voltage** options of the respective power supply, when applicable.
   - An empty box, NA, or "-" means Not Applicable.

   For more information, see valid operating voltage range defined for each power supply in *Recommended Operating Conditions*.
10. **Power:** The power supply of the associated I/O, when applicable.
    - An empty box, NA, or "-" means Not Applicable.
11. **Hys:** Indicates if the input buffer associated with this I/O has hysteresis:
    - Yes: Hysteresis Support
    - No: **No** Hysteresis Support
    - An empty box, NA, or "-" means Not Applicable.

    For more information, see the hysteresis values in *Electrical Characteristics*.
12. **Pull Type:** Indicates the presence of an internal pull-up or pull-down resistor. Internal resistors can be enabled or disabled via software.
    - PU: Internal pull-up Only
    - PD: Internal pull-down Only
    - PU/PD: Internal pull-up and pull-down
    - An empty box, NA, or "-" means No internal pull.

Note

Configuring two pins to the same pin multiplexed signal function is not supported as this yields unexpected results. Issues can be easily prevented with the proper software configuration.

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This must be avoided.

13. **Buffer Type:** This column defines the buffer type associated with a terminal. This information can be used to determine the applicable Electrical Characteristics table.
    - An empty box, NA, or "-" means Not Applicable.

    For electrical characteristics, refer to the appropriate buffer type table in *Electrical Characteristics*.
14. **Pad Configuration Register Name:** This is the name of the device pad/pin configuration register.
15. **Pad Configuration Register Address:** This is the memory address of the device pad/pin configuration register.
16. **Pad Configuration Register Default Value**: This is the default value of the register device pad/pin configuration register after PORz is deasserted.

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
V15	W13	P11	W12	ADC0_AIN0	ADC0_AIN0		-				-		Analog	
U15	U13	N11	V12	ADC0_AIN1	ADC0_AIN1		-				-		Analog	
T14	W14	R11	V13	ADC0_AIN2	ADC0_AIN2		-				-		Analog	
U14	V14	P12	U11	ADC0_AIN3	ADC0_AIN3		-				-		Analog	
U13	Y14	T12	W13	ADC0_AIN4	ADC0_AIN4		-				-		Analog	
R14	W15	R12	U13	ADC0_AIN5	ADC0_AIN5		-				-		Analog	
	Y15	T13	W14	ADC0_AIN6	ADC0_AIN6		-				-		Analog	
T11	W12	R10		ADC1_AIN0	ADC1_AIN0		-				-		Analog	
U11	V12	N10		ADC1_AIN1	ADC1_AIN1		-				-		Analog	
T12	Y11	P10		ADC1_AIN2	ADC1_AIN2		-				-		Analog	
V12	W11	P9		ADC1_AIN3	ADC1_AIN3		-				-		Analog	
U12	Y10	T9		ADC1_AIN4	ADC1_AIN4		-				-		Analog	
R12	W10	R9		ADC1_AIN5	ADC1_AIN5		-				-		Analog	
	W9	R8		ADC1_AIN6	ADC1_AIN6		-				-		Analog	
R10	W8	R7	W8	ADC2_AIN0	ADC2_AIN0		-				-		Analog	
T10	Y7	P7	V9	ADC2_AIN1	ADC2_AIN1		-				-		Analog	
U10	Y6	P8	V6	ADC2_AIN2	ADC2_AIN2		-				-		Analog	
T9	W7	P6	V7	ADC2_AIN3	ADC2_AIN3		-				-		Analog	
V9	W6	R6	W9	ADC2_AIN4	ADC2_AIN4		-				-		Analog	
T8	V9	N7	V8	ADC2_AIN5	ADC2_AIN5		-				-		Analog	
	Y5	T6	W7	ADC2_AIN6	ADC2_AIN6		-				-		Analog	
U16	V16	R13	U15	ADC_CAL0	ADC_CAL0		-				-		Analog	
			V11	ADC_VREFHI_G0	ADC_VREFHI0		-				-		Analog	
V14	Y12	T10	V11	ADC_VREFHI_G0	ADC_VREFHI1		-				-		Analog	
V10	Y8	T7	V10	ADC_VREFHI_G1	ADC_VREFHI2		-				-		Analog	
			W11	ADC_VREFLO_G0	ADC_VREFLO0		-				-		Analog	
V13	Y13	T11	W11	ADC_VREFLO_G0	ADC_VREFLO1		-				-		Analog	
V11	Y9	T8	W10	ADC_VREFLO_G1	ADC_VREFLO2		-				-		Analog	
T6	W5	T4	W5	ATESTV1	ATESTV1		-				-		Analog	
T5	W4	T5	W6	DAC_OUT	DAC_OUT		-				-		Analog	
T13	U15	P13	V14	DAC_VREF0	DAC_VREF0		-				-		Analog	
P1	U4	N3	R1	GPIO0	OSPI0_CSn0	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
				GPIO0_CFG_REG 0x5310 0000 0x0000 05F7	SPI0_CS0	1	IO							
					UART3_RXD	2	I							
					OSPI0_D0	4	IO							
					GPIO0	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
R3	T2	M3	R2	GPIO1 GPIO1_CFG_REG 0x5310 0004 0x0000 05F7	OSPI0_CSn1	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					SPI0_CLK	1	IO							
					UART3_TXD	2	O							
					UART2_RTSn	5	O							
					GPIO1	7	IO							
					XBAROUT0	10	O							
N2	M3	L2	M2	GPIO2 GPIO2_CFG_REG 0x5310 0008 0x0000 05F7	OSPI0_CLK	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D0	1	IO							
					UART3_CTSn	4	I							
					OSPI1_D0	5	IO							
					GPIO2	7	IO							
N1	R2	M2	N2	GPIO3 GPIO3_CFG_REG 0x5310 000C 0x0000 05D7	OSPI0_D0	0	IO	On / Off / Off	On / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					EPWM9_A	1	O							
					PR1_PRU1_GPIO11	2	IO							
					UART1_DCDn	3	I							
					GPMC0_AD11	6	O							
					GPIO3	7	IO							
					SOP0	Bootstrap								
N4	R1	N1	N1	GPIO4 GPIO4_CFG_REG 0x5310 0010 0x0000 05D7	OSPI0_D1	0	IO	On / Off / Off	On / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					EPWM9_B	1	O							
					PR1_PRU1_GPIO12	2	IO							
					UART1_RIn	3	I							
					GPMC0_AD12	6	O							
					GPIO4	7	IO							
					SOP1	Bootstrap								
M4	T1	L3	P2	GPIO5 GPIO5_CFG_REG 0x5310 0014 0x0000 05F7	OSPI0_D2	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					SPI0_D0	1	IO							
					OSPI0_D6	2	IO							
					GPIO5	7	IO							
P3	U1	N2	P1	GPIO6 GPIO6_CFG_REG 0x5310 0018 0x0000 05F7	OSPI0_D3	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					SPI0_D1	1	IO							
					OSPI0_D4	2	IO							
					GPIO6	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
M1	P1	J3	K2	GPIO7 GPIO7_CFG_REG 0x5310 001C 0x0000 05F7	MCAN0_RX	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D4	1	IO							
					OSPI0_D2	2	IO							
					OSPI0_DQS	5	I							
					GPIO7	7	IO							
L1	P2	K1	L1	GPIO8 GPIO8_CFG_REG 0x5310 0020 0x0000 05F7	MCAN0_TX	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D5	1	IO							
					OSPI0_D6	2	IO							
					OSPI0_D2	5	IO							
					GPIO8	7	IO							
L2	N2	K2	J2	GPIO9 GPIO9_CFG_REG 0x5310 0024 0x0000 05F7	MCAN1_RX	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D6	1	IO							
					OSPI0_DQS	2	I							
					LIN1_TXD	3	IO							
					UART1_TXD	4	O							
					OSPI0_CLK	5	O							
					GPIO9	7	IO							
K1	N1	J2	K1	GPIO10 GPIO10_CFG_REG 0x5310 0028 0x0000 05F7	MCAN1_TX	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D7	1	IO							
					OSPI0_CLK	2	O							
					UART1_DTRn	3	O							
					UART3_CTSn	4	I							
					OSPI1_CLK	5	O							
					GPIO10	7	IO							
C11	B13	B11	C13	GPIO11 GPIO11_CFG_REG 0x5310 002C 0x0000 05F7	SPI0_CS0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO2	1	IO							
					MMC0_CLK	2	IO							
					UART3_RXD	3	I							
					GPMC0_A0	6	O							
					GPIO11	7	IO							
					ADC_EXTCH_XBAROUT0	9	O							
					XBAROUT0	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
A11	A13	A12	A12	GPIO12 GPIO12_CFG_REG 0x5310 0030 0x0000 05D7	SPI0_CLK	0	IO	On / Off / Off	On / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO9	1	IO							
					MMC0_CMD	2	IO							
					UART3_TXD	3	O							
					FSITX0_CLK	5	O							
					GPMC0_A7	6	O							
					GPIO12	7	IO							
					ADC_EXTCH_XBAROUT1	9	O							
					XBAROUT1	10	O							
					SOP2	Bootstrap								
C10	B12	A10	B12	GPIO13 GPIO13_CFG_REG 0x5310 0034 0x0000 05D7	SPI0_D0	0	IO	On / Off / Off	On / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO0	1	IO							
					MMC0_D0	2	IO							
					UART3_CTSn	3	I							
					FSITX0_DATA0	5	O							
					GPMC0_A16	6	O							
					GPIO13	7	IO							
					ADC_EXTCH_XBAROUT2	9	O							
					XBAROUT2	10	O							
					SOP3	Bootstrap								
B11	C12	A11	B11	GPIO14 GPIO14_CFG_REG 0x5310 0038 0x0000 05F7	SPI0_D1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO1	1	IO							
					MMC0_D1	2	IO							
					UART3_RTSn	3	O							
					FSITX0_DATA1	5	O							
					GPMC0_BE1n	6	O							
					GPIO14	7	IO							
					ADC_EXTCH_XBAROUT3	9	O							
					XBAROUT3	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
C9	D11	B9		GPIO15 GPIO15_CFG_REG 0x5310 003C 0x0000 05F7	SPI1_CS0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					EPWM7_A	1	O							
					MMC0_D2	2	IO							
					UART4_TXD	3	O							
					PR1_PRU1_GPIO4	5	IO							
					GPIO15	7	IO							
					GPMC0_WAIT0	8	I							
					ADC_EXTCH_XBAROUT4	9	O							
					XBAROUT1	10	O							
A10	A12	B10		GPIO16 GPIO16_CFG_REG 0x5310 0040 0x0000 05F7	SPI1_CLK	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					EPWM7_B	1	O							
					MMC0_D3	2	IO							
					UART4_RXD	3	I							
					PR1_PRU1_GPIO3	5	IO							
					FSIRX0_CLK	6	I							
					GPIO16	7	IO							
					GPMC0_OEn_REn	8	O							
					ADC_EXTCH_XBAROUT5	9	O							
					XBAROUT2	10	O							
B10	D10	A9		GPIO17 GPIO17_CFG_REG 0x5310 0044 0x0000 05F7	SPI1_D0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					EPWM8_A	1	O							
					MMC0_WP	2	I							
					UART5_TXD	3	O							
					OSPI0_ECC_FAIL	4	I							
					PR1_PRU1_GPIO16	5	IO							
					FSIRX0_DATA0	6	I							
					GPIO17	7	IO							
					GPMC0_DIR	8	O							
					ADC_EXTCH_XBAROUT6	9	O							
					XBAROUT3	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
D9	C9	C11		GPIO18 GPIO18_CFG_REG 0x5310 0048 0x0000 05F7	SPI1_D1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					EPWM8_B	1	O							
					MMC0_CD	2	I							
					UART5_RXD	3	I							
					OSPI0_RESET_OUT0	4	O							
					PR1_PRU1_GPIO15	5	IO							
					FSIRX0_DATA1	6	I							
					GPIO18	7	IO							
					GPMC0_WPn	8	O							
					ADC_EXTCH_XBAROUT7	9	O							
					XBAROUT4	10	O							
A9	A11	C10	A11	GPIO19 GPIO19_CFG_REG 0x5310 004C 0x0000 05F7	LIN1_RXD	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					OSPI0_ECC_FAIL	1	I							
					SPI2_CS0	2	IO							
					PR1_PRU1_GPIO6	3	IO							
					OSPI1_ECC_FAIL	4	I							
					UART1_RXD	5	I							
					GPMC0_AD6	6	IO							
					GPIO19	7	IO							
					OSPI0_RESET_OUT1	8	O							
					XBAROUT5	10	O							
					EPWM6_B	11	O							
M15	P19	J16	N19	GPIO100 GPIO100_CFG_REG 0x5310 0190 0x0000 05F7	PR0_PRU0_GPIO12	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RMII2_TXD1	2	O							
					RGMII2_TD1	3	O							
					MII2_TXD1	4	O							
					GPIO100	7	IO							
H17	K20	F15	H19	GPIO101 GPIO101_CFG_REG 0x5310 0194 0x0000 05F7	PR0_PRU0_GPIO13	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII2_TD2	3	O							
					MII2_TXD2	4	O							
					GPIO101	7	IO							
H16	L19	G14	H18	GPIO102 GPIO102_CFG_REG 0x5310 0198 0x0000 05F7	PR0_PRU0_GPIO14	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII2_TD3	3	O							
					MII2_TXD3	4	O							
					GPIO102	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
F15	F20		E18	GPIO103 GPIO103_CFG_REG 0x5310 019C 0x0000 05F7	PR0_PRU1_GPIO5	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RMII1_RX_ER	2	I							
					MII1_RX_ER	4	I							
					GPIO103	7	IO							
					TRC_DATA0	8	O							
					ADC_EXTCH_XBAROUT6	9	O							
C18	E20			GPIO104 GPIO104_CFG_REG 0x5310 01A0 0x0000 05F7	PR0_PRU1_GPIO9	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR0_UART0_RXD	1	I							
					PR0_IEP0_EDIO_DATA_IN_OUT31	3	IO							
					MII1_COL	4	I							
					GPMC0_A21	6	O							
					GPIO104	7	IO							
					TRC_DATA1	8	O							
					ADC_EXTCH_XBAROUT7	9	O							
D17	E19			GPIO105 GPIO105_CFG_REG 0x5310 01A4 0x0000 05F7	PR0_PRU1_GPIO10	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR0_UART0_TXD	1	O							
					RMII1_CRS_DV	2	I							
					PR0_IEP0_EDIO_DATA_IN_OUT30	3	IO							
					MII1_CRS	4	I							
					GPMC0_A20	6	O							
					GPIO105	7	IO							
					TRC_DATA2	8	O							
D18	G18		C19	GPIO106 GPIO106_CFG_REG 0x5310 01A8 0x0000 05F7	PR0_PRU1_GPIO8	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					GPIO106	7	IO							
					TRC_DATA3	8	O							
E16	F19	E13	D19	GPIO107 GPIO107_CFG_REG 0x5310 01AC 0x0000 05F7	PR0_PRU1_GPIO6	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MCAN0_RX	1	I							
					RMII1_REF_CLK	2	IO							
					RGMII1_RXC	3	I							
					MII1_RXCLK	4	I							
					GPIO107	7	IO							
					TRC_DATA4	8	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
F16	G19	D15	E19	GPIO108 GPIO108_CFG_REG 0x5310 01B0 0x0000 05F7	PR0_PRU1_GPIO4	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MCAN0_TX	1	O							
					RGMII1_RX_CTL	3	I							
					MII1_RXDV	4	I							
					GPIO108	7	IO							
					TRC_DATA5	8	O							
F18	H20	D14	G18	GPIO109 GPIO109_CFG_REG 0x5310 01B4 0x0000 05F7	PR0_PRU1_GPIO0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MCAN1_RX	1	I							
					RMII1_RXD0	2	I							
					RGMII1_RD0	3	I							
					MII1_RXD0	4	I							
					GPIO109	7	IO							
					TRC_DATA6	8	O							
G16	H19	D16	F18	GPIO110 GPIO110_CFG_REG 0x5310 01B8 0x0000 05F7	PR0_PRU1_GPIO1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MCAN1_TX	1	O							
					RMII1_RXD1	2	I							
					RGMII1_RD1	3	I							
					MII1_RXD1	4	I							
					GPIO110	7	IO							
					TRC_DATA7	8	O							
E17	H17		E17	GPIO111 GPIO111_CFG_REG 0x5310 01BC 0x0000 05F7	PR0_PRU1_GPIO2	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII1_RD2	3	I							
					MII1_RXD2	4	I							
					GPIO111	7	IO							
					TRC_DATA8	8	O							
E18	G20		F19	GPIO112 GPIO112_CFG_REG 0x5310 01C0 0x0000 05F7	PR0_PRU1_GPIO3	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII1_RD3	3	I							
					MII1_RXD3	4	I							
					GPIO112	7	IO							
					TRC_DATA9	8	O							
C16	B20		B18	GPIO113 GPIO113_CFG_REG 0x5310 01C4 0x0000 05F7	PR0_PRU1_GPIO16	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII1_TXC	3	O							
					MII1_TXCLK	4	I							
					GPIO113	7	IO							
					TRC_DATA10	8	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
A17	E18		A18	GPIO114 GPIO114_CFG_REG 0x5310 01C8 0x0000 05F7	PR0_PRU1_GPIO15	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RMII1_TX_EN	2	O							
					RGMII1_TX_CTL	3	O							
					MII1_TX_EN	4	O							
					GPIO114	7	IO							
					TRC_DATA11	8	O							
B18	F17		D18	GPIO115 GPIO115_CFG_REG 0x5310 01CC 0x0000 05F7	PR0_PRU1_GPIO11	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RMII1_TXD0	2	O							
					RGMII1_TD0	3	O							
					MII1_TXD0	4	O							
					GPIO115	7	IO							
					TRC_DATA12	8	O							
B17	D20		C18	GPIO116 GPIO116_CFG_REG 0x5310 01D0 0x0000 05F7	PR0_PRU1_GPIO12	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RMII1_TXD1	2	O							
					RGMII1_TD1	3	O							
					MII1_TXD1	4	O							
					GPIO116	7	IO							
					TRC_DATA13	8	O							
D16	C20		B19	GPIO117 GPIO117_CFG_REG 0x5310 01D4 0x0000 05F7	PR0_PRU1_GPIO13	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII1_TD2	3	O							
					MII1_TXD2	4	O							
					GPIO117	7	IO							
					TRC_DATA14	8	O							
					XBAROUT11	10	O							
C17	D19		C17	GPIO118 GPIO118_CFG_REG 0x5310 01D8 0x0000 05F7	PR0_PRU1_GPIO14	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII1_TD3	3	O							
					MII1_TXD3	4	O							
					GPIO118	7	IO							
					TRC_DATA15	8	O							
					XBAROUT12	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
D15	C18		B16	GPIO119 GPIO119_CFG_REG 0x5310 01DC 0x0000 05F7	PR0_PRU1_GPIO19	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART3_RXD	2	I							
					PR0_IEP0_EDC_SYNC_OUT0	3	O							
					GPMC0_A19	6	O							
					GPIO119	7	IO							
					TRC_CLK	8	O							
					EQEP1_A	9	I							
					XBAROUT13	10	O							
C15	C19		B17	GPIO120 GPIO120_CFG_REG 0x5310 01E0 0x0000 05F7	PR0_PRU1_GPIO18	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART3_TXD	2	O							
					PR0_IEP0_EDIO_DATA_IN_OUT31	3	IO							
					GPMC0_A17	6	O							
					GPIO120	7	IO							
					TRC_CTL	8	O							
					EQEP1_B	9	I							
					XBAROUT14	10	O							
P2	U2	P3	T1	GPIO121 GPIO121_CFG_REG 0x5310 01E4 0x0000 05F7	EXT_REFCLK0	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					SAFETY_ERRORn	1	IO							
					USB0_DRVVBUS	2	O							
					PR0_IEP0_EDIO_DATA_IN_OUT30	3	IO							
					GPMC0_A18	6	O							
					GPIO121	7	IO							
					EQEP1_INDEX	9	IO							
					XBAROUT15	10	O							
B16	B19	C15		GPIO122 GPIO122_CFG_REG 0x5310 01E8 0x0000 05F7	CLKOUT1	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO7	1	IO							
					UART2_RTSn	2	O							
					PR1_UART0_CTSn	4	I							
					GPMC0_A5	6	O							
					GPIO122	7	IO							
					SDFM0_CLK0	8	I							
					EQEP1_STROBE	9	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
D14	C16	A15		GPIO123 GPIO123_CFG_REG 0x5310 01EC 0x0000 05F7	PR0_ECAP0_APWM_OUT	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO10	1	IO							
					UART2_CTSn	2	I							
					PR1_ECAP0_APWM_OUT	3	O							
					PR1_UART0_RTSn	4	O							
					GPMC0_AD10	6	IO							
					GPIO123	7	IO							
					SDFM0_D0	8	I							
A16	A19	C16		GPIO124 GPIO124_CFG_REG 0x5310 01F0 0x0000 05F7	PR0_PRU1_GPIO7	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					CPTS0_TS_SYNC	1	O							
					PR1_PRU0_GPIO10	2	IO							
					PR0_IEP0_EDC_SYNC_OUT1	3	O							
					PR1_UART0_RXD	4	I							
					GPMC0_A8	6	O							
					GPIO124	7	IO							
					SDFM0_CLK1	8	I							
					SDFM1_D0	9	I							
					UART2_TXD	10	O							
					UART5_RTSn	11	O							
D13	B17	C14		GPIO125 GPIO125_CFG_REG 0x5310 01F4 0x0000 05F7	PR0_PRU1_GPIO17	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO13	1	IO							
					UART2_RXD	2	I							
					PR0_IEP0_EDIO_DATA_IN_OUT30	3	IO							
					PR1_UART0_TXD	4	O							
					UART5_CTSn	5	I							
					GPMC0_AD13	6	IO							
					GPIO125	7	IO							
					SDFM0_D1	8	I							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
B15	A18	B16	A17	GPIO126 GPIO126_CFG_REG 0x5310 01F8 0x0000 05F7	UART1_CTSn	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_MDIO0_MDIO	1	IO							
					SPI2_CS1	2	IO							
					PR1_IEP0_EDC_SYNC_OUT1	3	O							
					UART5_CTSn	4	I							
					UART5_TXD	5	O							
					GPMC0_CLKLB	6	IO							
					GPIO126	7	IO							
					SDFM0_CLK2	8	I							
					SDFM1_D1	9	I							
					ADC_EXTCH_XBAROUT8	10	O							
C13	A17	A14	A16	GPIO127 GPIO127_CFG_REG 0x5310 01FC 0x0000 05F7	UART2_CTSn	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_MDIO0_MDC	1	O							
					SPI3_CS1	2	IO							
					UART5_RXD	5	I							
					GPMC0_BE0n_CLE	6	O							
					GPIO127	7	IO							
					SDFM0_D2	8	I							
					ADC_EXTCH_XBAROUT0	10	O							
A15	B18	B15		GPIO128 GPIO128_CFG_REG 0x5310 0200 0x0000 05F7	SPI2_D1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO14	1	IO							
					UART5_RXD	5	I							
					GPMC0_AD14	6	IO							
					GPIO128	7	IO							
					SDFM0_CLK3	8	I							
					SDFM1_D2	9	I							
					ADC_EXTCH_XBAROUT9	10	O							
C14	D17	B14		GPIO129 GPIO129_CFG_REG 0x5310 0204 0x0000 05F7	SPI2_CLK	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO17	1	IO							
					UART5_TXD	5	O							
					GPMC0_WEn	6	O							
					GPIO129	7	IO							
					SDFM0_D3	8	I							
					ADC_EXTCH_XBAROUT1	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
B14	A16	D13	B15	GPIO130 GPIO130_CFG_REG 0x5310 0208 0x0000 05F7	SPI2_D0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO18	1	IO							
					UART4_RTSn	2	O							
					PR1_IEP0_EDC_SYNC_OUT0	3	O							
					I2C1_SDA	4	IO							
					MCAN1_RX	5	I							
					GPMC0_OEn_REn	6	O							
					GPIO130	7	IO							
					EQEP0_A	8	I							
					SDFM1_CLK0	9	I							
A14	B16	C13	A15	GPIO131 GPIO131_CFG_REG 0x5310 020C 0x0000 05F7	SPI2_CS0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO19	1	IO							
					UART4_CTSn	2	I							
					PR1_IEP0_EDIO_DATA_IN_OUT31	3	IO							
					I2C1_SCL	4	IO							
					MCAN1_TX	5	O							
					GPMC0_CSn0	6	O							
					GPIO131	7	IO							
					EQEP0_B	8	I							
					SDFM1_D0	9	I							
C12	C14	C12	A14	GPIO132 GPIO132_CFG_REG 0x5310 0210 0x0000 05F7	I2C2_SDA	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO20	1	IO							
					UART4_TXD	2	O							
					PR1_IEP0_EDIO_DATA_IN_OUT30	3	IO							
					GPMC0_A15	6	O							
					GPIO132	7	IO							
					EQEP0_STROBE	8	IO							
					SDFM1_CLK1	9	I							
					ADC_EXTCH_XBAROUT2	10	O							
D11	D15	B13	B14	GPIO133 GPIO133_CFG_REG 0x5310 0214 0x0000 05F7	I2C2_SCL	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO7	1	IO							
					UART4_RXD	2	I							
					GPMC0_AD7	6	IO							
					GPIO133	7	IO							
					EQEP0_INDEX	8	IO							
					SDFM1_D1	9	I							
					ADC_EXTCH_XBAROUT3	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
B13	B15	B12	B13	GPIO134 GPIO134_CFG_REG 0x5310 0218 0x0000 05F7	I2C0_SDA	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	I2C OPEN DRAIN	
					GPIO134	7	IO							
					SDFM1_CLK2	9	I							
A13	A15	A13	A13	GPIO135 GPIO135_CFG_REG 0x5310 021C 0x0000 05F7	I2C0_SCL	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	I2C OPEN DRAIN	
					GPIO135	7	IO							
					SDFM1_CLK3	9	I							
B12	B14			GPIO136 GPIO136_CFG_REG 0x5310 0220 0x0000 05F7	UART1_RTSn	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					SPI0_CS1	1	IO							
					LIN0_RXD	2	IO							
					UART3_RXD	3	I							
					GPIO136	7	IO							
					SDFM1_D2	9	I							
A12	A14			GPIO137 GPIO137_CFG_REG 0x5310 0224 0x0000 05F7	UART2_RTSn	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					EQEP1_INDEX	1	IO							
					LIN0_TXD	2	IO							
					UART3_TXD	3	O							
					GPIO137	7	IO							
					SDFM1_D3	9	I							
M2	M1	H1	J3	GPIO138 GPIO138_CFG_REG 0x5310 0228 0x0000 0570	CLKOUT0	0	O	Off / Off / Off	Off / SS / Off	Mode0	1.8V/3.3V	Yes	LVCMOS	PU/PD
					LIN1_RXD	1	IO							
					OSPI0_ECC_FAIL	2	I							
					UART1_RXD	3	I							
					SPI2_CS0	4	IO							
					OSPI1_ECC_FAIL	5	I							
					USB0_DRVVBUS	6	O							
					GPIO138	7	IO							
					SAFETY_ERRORn	8	IO							
V2	V1	R1	V1	GPIO139 GPIO139_CFG_REG 0x5310 022C 0x00 0060	USB0_DP	0	IO	Off / Off / Off	Off / SS / Off	Mode0	3.3V	0	Analog	0
					UART5_RXD	1	I							
					GPIO139	7	IO							
U3	W1	P1	U1	GPIO140 GPIO140_CFG_REG 0x5310 0230 0x00 0060	USB0_DM	0	IO	Off / Off / Off	Off / SS / Off	Mode0	3.3V	0	Analog	0
					UART5_TXD	1	O							
					GPIO140	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
B9	B11	D8	B10	GPIO20 GPIO20_CFG_REG 0x5310 0050 0x0000 05F7	LIN1_TXD	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					OSPI0_RESET_OUT0	1	O							
					SPI2_CLK	2	IO							
					PR1_PRU1_GPIO8	3	IO							
					OSPI1_RESET_OUT0	4	O							
					UART1_TXD	5	O							
					GPMC0_AD8	6	IO							
					GPIO20	7	IO							
					XBAROUT6	10	O							
					EPWM6_A	11	O							
B8	B10	B8	A10	GPIO21 GPIO21_CFG_REG 0x5310 0054 0x0000 05F7	LIN2_RXD	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART2_RXD	1	I							
					SPI2_D0	2	IO							
					USB0_DRVVBUS	3	O							
					OSPI1_RESET_OUT1	4	O							
					OSPI0_RESET_OUT1	5	O							
					GPIO21	7	IO							
					GPMC0_CSn0	8	O							
A8	A10	C9	B9	GPIO22 GPIO22_CFG_REG 0x5310 0058 0x0000 05F7	LIN2_TXD	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART2_TXD	1	O							
					SPI2_D1	2	IO							
					GPIO22	7	IO							
					GPMC0_ADVn_ALE	8	O							
D7	B9	B7		GPIO23 GPIO23_CFG_REG 0x5310 005C 0x0000 05F7	I2C1_SCL	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					SPI3_CS0	2	IO							
					PR1_PRU0_GPIO17	3	IO							
					GPMC0_WEn	6	O							
					GPIO23	7	IO							
					XBAROUT7	10	O							
C8	A9	A8		GPIO24 GPIO24_CFG_REG 0x5310 0060 0x0000 05F7	I2C1_SDA	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					SPI3_CLK	2	IO							
					PR1_PRU0_GPIO18	3	IO							
					GPMC0_OEn_REn	6	O							
					GPIO24	7	IO							
					XBAROUT8	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
C7	C7	C8	C9	GPIO25 GPIO25_CFG_REG 0x5310 0064 0x0000 05F7	UART0_RTSn	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					I2C2_SCL	1	IO							
					SPI3_D0	2	IO							
					PR1_PRU1_GPIO19	3	IO							
					PR1_PRU0_GPIO17	4	IO							
					UART3_RXD	5	I							
					GPMC0_WAIT1	6	I							
					GPIO25	7	IO							
					XBAROUT9	10	O							
B7	D8	A7	A9	GPIO26 GPIO26_CFG_REG 0x5310 0068 0x0000 05F7	UART0_CTSn	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					I2C2_SDA	1	IO							
					SPI3_D1	2	IO							
					SPI0_CS1	3	IO							
					PR1_PRU0_GPIO7	4	IO							
					UART3_TXD	5	O							
					GPIO26	7	IO							
					XBAROUT10	10	O							
A7	A8	A6	A8	GPIO27 GPIO27_CFG_REG 0x5310 006C 0x0000 05F7	UART0_RXD	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					LIN0_RXD	1	IO							
					GPIO27	7	IO							
					XBAROUT4	10	O							
A6	B8	B6	B8	GPIO28 GPIO28_CFG_REG 0x5310 0070 0x0000 05F7	UART0_TXD	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					LIN0_TXD	1	IO							
					GPIO28	7	IO							
					XBAROUT5	10	O							
R17	W20	P16	V19	GPIO29 GPIO29_CFG_REG 0x5310 0074 0x0000 05F7	RGMII1_RXC	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_REF_CLK	1	IO							
					MII1_RXCLK	2	I							
					OSPI1_CLK	3	O							
					FSITX0_CLK	6	O							
					GPIO29	7	IO							
R18	V19	M14	U17	GPIO30 GPIO30_CFG_REG 0x5310 0078 0x0000 05F7	RGMII1_RX_CTL	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_RX_ER	1	I							
					MII1_RXDV	2	I							
					OSPI1_D0	3	IO							
					FSITX0_DATA0	6	O							
					GPIO30	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
U17	Y18	P14	W17	GPIO31 GPIO31_CFG_REG 0x5310 007C 0x0000 05F7	RGMII1_RD0	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_RXD0	1	I							
					MII1_RXD0	2	I							
					OSPI1_D1	3	IO							
					FSITX0_DATA1	6	O							
					GPIO31	7	IO							
T17	W18	P15	V17	GPIO32 GPIO32_CFG_REG 0x5310 0080 0x0000 05F7	RGMII1_RD1	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_RXD1	1	I							
					MII1_RXD1	2	I							
					OSPI1_D2	3	IO							
					FSIRX0_CLK	6	I							
					GPIO32	7	IO							
U18	Y19	R16	W18	GPIO33 GPIO33_CFG_REG 0x5310 0084 0x0000 05F7	RGMII1_RD2	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR1_IEP0_EDC_SYNC_OUT0	1	O							
					MII1_RXD2	2	I							
					OSPI1_D3	3	IO							
					UART1_RXD	4	I							
					FSIRX0_DATA0	6	I							
					GPIO33	7	IO							
					EQEP0_A	8	I							
					GPMC0_CSn2	9	O							
T18	W19	N14	V18	GPIO34 GPIO34_CFG_REG 0x5310 0088 0x0000 05F7	RGMII1_RD3	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR1_IEP0_EDIO_DATA_IN_OUT31	1	IO							
					MII1_RXD3	2	I							
					OSPI1_D4	3	IO							
					UART1_TXD	4	O							
					FSIRX0_DATA1	6	I							
					GPIO34	7	IO							
					EQEP0_B	8	I							
					GPMC0_CSn3	9	O							
N18	U20	L15	R18	GPIO35 GPIO35_CFG_REG 0x5310 008C 0x0000 05F7	RGMII1_TXC	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR1_IEP0_EDIO_DATA_IN_OUT30	1	IO							
					MII1_TXCLK	2	I							
					OSPI1_D5	3	IO							
					UART4_RXD	4	I							
					GPIO35	7	IO							
					EQEP0_INDEX	8	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
M18	T20	M16	T19	GPIO36 GPIO36_CFG_REG 0x5310 0090 0x0000 05F7	RGMII1_TX_CTL	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_TX_EN	1	O							
					MII1_TX_EN	2	O							
					OSPI1_D6	3	IO							
					GPIO36	7	IO							
					EQEP0_STROBE	8	IO							
P16	V18	N15	U18	GPIO37 GPIO37_CFG_REG 0x5310 0094 0x0000 05F7	RGMII1_TD0	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_TXD0	1	O							
					MII1_TXD0	2	O							
					OSPI1_D7	3	IO							
					GPIO37	7	IO							
					EQEP1_A	8	I							
P17	V20	N16	U19	GPIO38 GPIO38_CFG_REG 0x5310 0098 0x0000 05F7	RGMII1_TD1	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_TXD1	1	O							
					MII1_TXD1	2	O							
					OSPI1_CSn0	3	O							
					GPIO38	7	IO							
					EQEP1_B	8	I							
P18	U19	L13	R17	GPIO39 GPIO39_CFG_REG 0x5310 009C 0x0000 05F7	RGMII1_TD2	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					RMII1_CRS_DV	1	I							
					MII1_TXD2	2	O							
					OSPI1_DQS	3	I							
					GPIO39	7	IO							
					EQEP1_STROBE	8	IO							
N17	T19	M15	T18	GPIO40 GPIO40_CFG_REG 0x5310 00A0 0x0000 05F7	RGMII1_TD3	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR0_PRU0_GPIO7	1	IO							
					MII1_TXD3	2	O							
					OSPI1_ECC_FAIL	3	I							
					UART4_TXD	4	O							
					PR0_IEP0_EDC_SYNC_OUT1	5	O							
					PR1_IEP0_EDC_SYNC_OUT1	6	O							
					GPIO40	7	IO							
					EQEP1_INDEX	8	IO							
N16	R17	L16	P18	GPIO41 GPIO41_CFG_REG 0x5310 00A4 0x0000 05F7	MDIO0_MDIO	0	IO	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					MCAN1_RX	1	I							
					OSPI1_RESET_OUT0	3	O							
					GPIO41	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
M17	T18	L14	R19	GPIO42 GPIO42_CFG_REG 0x5310 00A8 0x0000 05F7	MDIO0_MDC	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MCAN1_TX	1	O							
					GPIO42	7	IO							
B2	B3	A4	B5	GPIO43 GPIO43_CFG_REG 0x5310 00AC 0x0000 05F7	EPWM0_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO5	2	IO							
					GPMC0_A3	6	O							
					GPIO43	7	IO							
					EPWM0_A	10	O							
B1	C3	A5	A6	GPIO44 GPIO44_CFG_REG 0x5310 00B0 0x0000 05F7	EPWM0_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO8	2	IO							
					GPMC0_A6	6	O							
					GPIO44	7	IO							
					EPWM0_B	10	O							
D3	A2	B4	A5	GPIO45 GPIO45_CFG_REG 0x5310 00B4 0x0000 05F7	EPWM1_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO6	2	IO							
					GPMC0_A4	6	O							
					GPIO45	7	IO							
					EPWM1_A	10	O							
D2	A3	C5	A4	GPIO46 GPIO46_CFG_REG 0x5310 00B8 0x0000 05F7	EPWM1_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO4	2	IO							
					GPMC0_A2	6	O							
					GPIO46	7	IO							
					EPWM4_B	10	O							
C2	B1	A3	A3	GPIO47 GPIO47_CFG_REG 0x5310 00BC 0x0000 05F7	EPWM2_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO3	2	IO							
					GPMC0_A1	6	O							
					GPIO47	7	IO							
					EPWM2_A	10	O							
C1	B2	A2	B4	GPIO48 GPIO48_CFG_REG 0x5310 00C0 0x0000 05F7	EPWM2_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO16	2	IO							
					PR1_PRU0_GPIO7	4	IO							
					GPMC0_A14	6	O							
					GPIO48	7	IO							
					EPWM2_B	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
E2	C1	B2	A2	GPIO49 GPIO49_CFG_REG 0x5310 00C4 0x0000 05F7	EPWM3_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO15	2	IO							
					GPMC0_A13	6	O							
					GPIO49	7	IO							
					EPWM3_A	10	O							
E3	C2	C4	B2	GPIO50 GPIO50_CFG_REG 0x5310 00C8 0x0000 05F7	EPWM3_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO11	2	IO							
					GPMC0_A9	6	O							
					GPIO50	7	IO							
					EPWM6_A	10	O							
D1	D2	B1	B1	GPIO51 GPIO51_CFG_REG 0x5310 00CC 0x0000 05F7	EPWM4_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO12	2	IO							
					GPMC0_A10	6	O							
					GPIO51	7	IO							
					EPWM4_A	10	O							
E4	D1	C1	B3	GPIO52 GPIO52_CFG_REG 0x5310 00D0 0x0000 05F7	EPWM4_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO13	2	IO							
					GPMC0_A11	6	O							
					GPIO52	7	IO							
					EPWM1_B	10	O							
F2	E2	C2	C2	GPIO53 GPIO53_CFG_REG 0x5310 00D4 0x0000 05F7	EPWM5_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO14	2	IO							
					GPMC0_A12	6	O							
					GPIO53	7	IO							
					EPWM5_A	10	O							
G2	E1	D3	C1	GPIO54 GPIO54_CFG_REG 0x5310 00D8 0x0000 05F7	EPWM5_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO5	2	IO							
					OSPI0_RESET_OUT0	3	O							
					GPMC0_AD5	6	IO							
					GPIO54	7	IO							
					EPWM8_B	10	O							
E1	F2	E3	E3	GPIO55 GPIO55_CFG_REG 0x5310 00DC 0x0000 05F7	EPWM6_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO8	1	IO							
					CLKOUT0	2	O							
					GPMC0_AD8	6	IO							
					GPIO55	7	IO							
					EPWM3_B	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
F3	F1	F4	E2	GPIO56 GPIO56_CFG_REG 0x5310 00E0 0x0000 05F7	EPWM6_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO6	1	IO							
					UART2_RTSn	3	O							
					GPMC0_A20	6	O							
					GPIO56	7	IO							
					EPWM6_B	10	O							
F4	G2	D2	D2	GPIO57 GPIO57_CFG_REG 0x5310 00E4 0x0000 05F7	EPWM7_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO4	1	IO							
					OSPI0_CSn1	2	O							
					OSPI1_CSn1	5	O							
					GPMC0_AD4	6	IO							
					GPIO57	7	IO							
					EPWM7_A	10	O							
F1	G1	D1	D1	GPIO58 GPIO58_CFG_REG 0x5310 00E8 0x0000 05F7	EPWM7_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO3	1	IO							
					OSPI1_D1	2	IO							
					OSPI0_D1	5	IO							
					GPMC0_AD3	6	IO							
					GPIO58	7	IO							
					EPWM5_B	10	O							
G3	H2	E2	E1	GPIO59 GPIO59_CFG_REG 0x5310 00EC 0x0000 05F7	EPWM8_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO16	1	IO							
					OSPI1_D0	2	IO							
					MCAN0_RX	3	I							
					PR0_PRU1_GPIO7	4	IO							
					OSPI0_D0	5	IO							
					GPMC0_CSn1	6	O							
					GPIO59	7	IO							
					UART4_TXD	8	O							
					EPWM8_A	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
H2	H1	E1	F1	GPIO60 GPIO60_CFG_REG 0x5310 00F0 0x0000 05F7	EPWM8_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU1_GPIO15	1	IO							
					OSPI1_CLK	2	O							
					MCAN0_TX	3	O							
					OSPI0_CLK	5	O							
					GPMC0_AD15	6	IO							
					GPIO60	7	IO							
					UART4_RXD	8	I							
					EPWM9_B	10	O							
G1	K4	F2	F2	GPIO61 GPIO61_CFG_REG 0x5310 00F4 0x0000 05F7	EPWM9_A	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					LIN1_TXD	1	IO							
					OSPI0_RESET_OUT0	2	O							
					SPI2_CLK	3	IO							
					UART1_TXD	4	O							
					OSPI1_RESET_OUT0	5	O							
					GPIO61	7	IO							
					EPWM9_A	10	O							
J2	L2	F3	G1	GPIO62 GPIO62_CFG_REG 0x5310 00F8 0x0000 05F7	EPWM9_B	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					LIN1_RXD	1	IO							
					OSPI0_CSn0	2	O							
					UART1_RTSn	3	O							
					OSPI1_CSn0	5	O							
					GPIO62	7	IO							
G4	J2			GPIO63 GPIO63_CFG_REG 0x5310 00FC 0x0000 05F7	LIN0_RXD	0	IO	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					UART1_CTSn	1	I							
					I2C0_SDA	3	IO							
					UART2_TXD	4	O							
					GPIO63	7	IO							
					EPWM7_B	10	O							
J3	J1			GPIO64 GPIO64_CFG_REG 0x5310 0100 0x0000 05F7	LIN0_TXD	0	IO	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					UART2_RTSn	1	O							
					OSPI0_RESET_OUT0	2	O							
					I2C0_SCL	3	IO							
					UART4_TXD	4	O							
					GPIO64	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
H1	J3			GPIO65 GPIO65_CFG_REG 0x5310 0104 0x0000 05F7	OSPI0_ECC_FAIL	0	I	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					UART2_CTSn	1	I							
					OSPI0_RESET_OUT1	2	O							
					I2C1_SDA	3	IO							
					UART4_RXD	4	I							
					OSPI0_CSn0	6	O							
					GPIO65	7	IO							
J1	K2	G3		GPIO66 GPIO66_CFG_REG 0x5310 0108 0x0000 05F7	OSPI0_RESET_OUT0	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					UART3_RTSn	1	O							
					I2C1_SCL	3	IO							
					UART2_RXD	4	I							
					OSPI0_D1	6	IO							
					GPIO66	7	IO							
K2	K1	G2	G2	GPIO67 GPIO67_CFG_REG 0x5310 010C 0x0000 05F7	PR1_PRU0_GPIO0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D5	2	IO							
					UART3_CTSn	3	I							
					GPIO67	7	IO							
J4	L4	H3	H1	GPIO68 GPIO68_CFG_REG 0x5310 0110 0x0000 05F7	PR1_PRU0_GPIO1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D7	2	IO							
					UART1_DCDn	3	I							
					GPIO68	7	IO							
K4	L1	H2	H2	GPIO69 GPIO69_CFG_REG 0x5310 0114 0x0000 05F7	PR1_PRU0_GPIO2	0	IO	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D3	2	IO							
					UART1_RIn	3	I							
					GPIO69	7	IO							
K3	M2	G1	J1	GPIO70 GPIO70_CFG_REG 0x5310 0118 0x0000 05F7	PR1_PRU0_GPIO9	0	IO	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_D1	2	IO							
					UART1_DTRn	3	O							
					UART3_CTSn	4	I							
					OSPI1_D1	5	IO							
					OSPI0_ECC_FAIL	6	I							
					GPIO70	7	IO							
V17	W16	R14	V15	GPIO71 GPIO71_CFG_REG 0x5310 011C 0x0000 05F7	PR1_PRU1_GPIO0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART1_DSRn	1	I							
					UART4_RTSn	3	O							
					GPMC0_AD0	6	IO							
					GPIO71	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
T16	Y16	T14	W15	GPIO72 GPIO72_CFG_REG 0x5310 0120 0x0000 05F7	PR1_PRU1_GPIO1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MII1_RX_ER	2	I							
					UART4_CTSn	3	I							
					GPMC0_AD1	6	IO							
					GPIO72	7	IO							
P15	W17	T15	W16	GPIO73 GPIO73_CFG_REG 0x5310 0124 0x0000 05F7	PR1_PRU1_GPIO2	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MII1_COL	2	I							
					UART5_TXD	3	O							
					GPMC0_AD2	6	IO							
					GPIO73	7	IO							
					ADC_EXTCH_XBAROUT4	9	O							
R16	Y17	R15	V16	GPIO74 GPIO74_CFG_REG 0x5310 0128 0x0000 05F7	PR1_PRU1_GPIO9	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MII1_CRS	2	I							
					UART5_RXD	3	I							
					GPMC0_AD9	6	IO							
					GPIO74	7	IO							
					ADC_EXTCH_XBAROUT5	9	O							
L3	T3	M1	L2	GPIO75 GPIO75_CFG_REG 0x5310 012C 0x0000 05F7	UART1_RXD	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					OSPI0_LBCLKO	1	O							
					LIN1_RXD	4	IO							
					OSPI1_LBCLKO	5	O							
					GPMC0_CLK	6	IO							
					GPIO75	7	IO							
M3	R4	L1	M1	GPIO76 GPIO76_CFG_REG 0x5310 0130 0x0000 05F7	UART1_TXD	0	O	Off / Off / Off	Off / Off / Off	Mode7	1.8V/3.3V	Yes	LVCMOS	PU/PD
					OSPI0_DQS	1	I							
					OSPI0_D4	2	IO							
					LIN1_TXD	4	IO							
					GPIO76	7	IO							
B6	B7			GPIO77 GPIO77_CFG_REG 0x5310 0134 0x0000 05F7	MMC0_CLK	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART0_RXD	1	I							
					LIN0_RXD	2	IO							
					MCAN0_RX	3	I							
					PR1_MDIO0_MDIO	4	IO							
					GPIO77	7	IO							
					SDFM1_CLK0	8	I							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
A4	A6			GPIO78 GPIO78_CFG_REG 0x5310 0138 0x0000 05F7	MMC0_CMD	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART0_TXD	1	O							
					LIN0_TXD	2	IO							
					MCAN0_TX	3	O							
					PR1_MDIO0_MDC	4	O							
					GPIO78	7	IO							
					SDFM1_D0	8	I							
B5	B6			GPIO79 GPIO79_CFG_REG 0x5310 013C 0x0000 05F7	MMC0_D0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART2_RXD	1	I							
					I2C1_SCL	2	IO							
					MCAN1_RX	3	I							
					PR1_PRU0_GPIO10	4	IO							
					GPIO79	7	IO							
					SDFM1_CLK1	8	I							
B4	A5			GPIO80 GPIO80_CFG_REG 0x5310 0140 0x0000 05F7	MMC0_D1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					MCAN1_TX	3	O							
					PR1_PRU0_GPIO9	4	IO							
					GPIO80	7	IO							
					SDFM1_D1	8	I							
A3	B5			GPIO81 GPIO81_CFG_REG 0x5310 0144 0x0000 05F7	MMC0_D2	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART2_TXD	1	O							
					I2C1_SDA	2	IO							
					PR1_PRU0_GPIO0	4	IO							
					GPIO81	7	IO							
					SDFM1_CLK2	8	I							
A2	A4			GPIO82 GPIO82_CFG_REG 0x5310 0148 0x0000 05F7	MMC0_D3	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART3_RTSn	1	O							
					PR1_PRU0_GPIO1	4	IO							
					GPIO82	7	IO							
					SDFM1_D2	8	I							
C6	B4			GPIO83 GPIO83_CFG_REG 0x5310 014C 0x0000 05F7	MMC0_WP	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART0_RTSn	1	O							
					I2C2_SCL	2	IO							
					PR1_PRU0_GPIO2	4	IO							
					GPIO83	7	IO							
					SDFM1_CLK3	8	I							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
A5	A7			GPIO84 GPIO84_CFG_REG 0x5310 0150 0x0000 05F7	MMC0_CD	0	I	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART0_CTSn	1	I							
					I2C2_SDA	2	IO							
					GPIO84	7	IO							
					SDFM1_D3	8	I							
L17	R19	K15	N17	GPIO85 GPIO85_CFG_REG 0x5310 0154 0x0000 05F7	PR0_MDIO0_MDIO	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					LIN0_RXD	1	IO							
					MCAN0_RX	2	I							
					GPIO85	7	IO							
					XBAROUT14	10	O							
L18	R20	K16	P19	GPIO86 GPIO86_CFG_REG 0x5310 0158 0x0000 05F7	PR0_MDIO0_MDC	0	O	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					LIN0_TXD	1	IO							
					MCAN0_TX	2	O							
					GPIO86	7	IO							
					XBAROUT15	10	O							
G17	K19	F14	G17	GPIO87 GPIO87_CFG_REG 0x5310 015C 0x0000 05F7	PR0_PRU0_GPIO5	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART3_RTSn	1	O							
					RMII2_RX_ER	2	I							
					MII2_RX_ER	4	I							
					GPIO87	7	IO							
					TRC_CTL	8	O							
					ADC_EXTCH_XBAROUT4	9	O							
					XBAROUT6	10	O							
F17	J19	E15		GPIO88 GPIO88_CFG_REG 0x5310 0160 0x0000 05F7	PR0_PRU0_GPIO9	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO9	1	IO							
					PR0_IEP0_EDC_SYNC_OUT1	2	O							
					PR0_UART0_CTSn	3	I							
					MII2_COL	4	I							
					GPIO88	7	IO							
G18	J20	E16	J18	GPIO89 GPIO89_CFG_REG 0x5310 0164 0x0000 05F7	PR0_PRU0_GPIO10	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART3_CTSn	1	I							
					RMII2_CRS_DV	2	I							
					PR0_UART0_RTSn	3	O							
					MII2_CRS	4	I							
					GPIO89	7	IO							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
G15	J18	E14	G19	GPIO90 GPIO90_CFG_REG 0x5310 0168 0x0000 05F7	PR0_PRU0_GPIO8	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					I2C0_SDA	1	IO							
					GPIO90	7	IO							
K15	N20	H15	L18	GPIO91 GPIO91_CFG_REG 0x5310 016C 0x0000 05F7	PR0_PRU0_GPIO6	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					I2C0_SCL	1	IO							
					RMII2_REF_CLK	2	IO							
					RGMII2_RXC	3	I							
					MII2_RXCLK	4	I							
					GPIO91	7	IO							
K16	L20	G15	J19	GPIO92 GPIO92_CFG_REG 0x5310 0170 0x0000 05F7	PR0_PRU0_GPIO4	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART3_RXD	1	I							
					RGMII2_RX_CTL	3	I							
					MII2_RXDV	4	I							
					GPIO92	7	IO							
					TRC_CLK	8	O							
					ADC_EXTCH_XBAROUT5	9	O							
					XBAROUT7	10	O							
K17	N17	K14	M18	GPIO93 GPIO93_CFG_REG 0x5310 0174 0x0000 05F7	PR0_PRU0_GPIO0	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO0	1	IO							
					RMII2_RXD0	2	I							
					RGMII2_RD0	3	I							
					MII2_RXD0	4	I							
					GPIO93	7	IO							
					TRC_DATA0	8	O							
					ADC_EXTCH_XBAROUT6	9	O							
					XBAROUT8	10	O							
K18	N19	H14	L19	GPIO94 GPIO94_CFG_REG 0x5310 0178 0x0000 05F7	PR0_PRU0_GPIO1	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO1	1	IO							
					RMII2_RXD1	2	I							
					RGMII2_RD1	3	I							
					MII2_RXD1	4	I							
					GPIO94	7	IO							
					TRC_DATA1	8	O							
					ADC_EXTCH_XBAROUT7	9	O							
					XBAROUT11	10	O							

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
J18	M18	G16	K19	GPIO95 GPIO95_CFG_REG 0x5310 017C 0x0000 05F7	PR0_PRU0_GPIO2	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					PR1_PRU0_GPIO2	1	IO							
					RGMII2_RD2	3	I							
					MII2_RXD2	4	I							
					GPIO95	7	IO							
					TRC_DATA2	8	O							
					ADC_EXTCH_XBAROUT8	9	O							
					XBAROUT12	10	O							
J17	M20	J14	L17	GPIO96 GPIO96_CFG_REG 0x5310 0180 0x0000 05F7	PR0_PRU0_GPIO3	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					UART3_TXD	1	O							
					RGMII2_RD3	3	I							
					MII2_RXD3	4	I							
					GPIO96	7	IO							
					TRC_DATA3	8	O							
					ADC_EXTCH_XBAROUT9	9	O							
					XBAROUT13	10	O							
H18	M19	F16	K18	GPIO97 GPIO97_CFG_REG 0x5310 0184 0x0000 05F7	PR0_PRU0_GPIO16	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RGMII2_TXC	3	O							
					MII2_TXCLK	4	I							
					GPIO97	7	IO							
L16	P18	H16	M19	GPIO98 GPIO98_CFG_REG 0x5310 0188 0x0000 05F7	PR0_PRU0_GPIO15	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RMII2_TX_EN	2	O							
					RGMII2_TX_CTL	3	O							
					MII2_TX_EN	4	O							
					GPIO98	7	IO							
M16	P20	J15	N18	GPIO99 GPIO99_CFG_REG 0x5310 018C 0x0000 05F7	PR0_PRU0_GPIO11	0	IO	Off / Off / Off	Off / Off / Off	Mode7	3.3V	Yes	LVCMOS	PU/PD
					RMII2_TXD0	2	O							
					RGMII2_TD0	3	O							
					MII2_TXD0	4	O							
					GPIO99	7	IO							
J15, R7, R9, T15, T7, U4, U5, U6, U7, U8, U9, V3, V4, V5, V6, V7, V8	U17			NC	NC	0	NC				NA	0	-	0
R2	V3	P2	T2	PORz	PORz	0	I			Mode0	3.3V	Yes	HHV	

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
D4	E3	B3	C5	SAFETY_ERRORn SAFETY_ERRORn_CFG_REG 0x5310 0238 0x0000 0410	SAFETY_ERRORn	0	IO	On / Low / Down	On / NA / Down	Mode0	3.3V	Yes	LVCMOS	PU/PD
B3	D4	C6	B6	TCK TCK_CFG_REG 0x5310 0248 0x0000 0210	TCK	0	I	On / Low / Up	On / NA / Up	Mode0	3.3V	Yes	LVCMOS	
C5	C5	D5	C7	TDI TDI_CFG_REG 0x5310 023C 0x0000 06D0	TDI	0	I	On / Low / Up	On / Off / Up	Mode0	3.3V	Yes	LVCMOS	PU/PD
C4	E5	B5	A7	TDO TDO_CFG_REG 0x5310 0240 0x0000 0630	TDO	0	O	Off / Low / Up	Off / NA / Up	Mode0	3.3V	Yes	LVCMOS	PU/PD
U1	W3	P5	W4	TEMPCAL	TEMPCAL		-				-		Analog	
D5	D6	C7	B7	TMS TMS_CFG_REG 0x5310 0244 0x0000 0610	TMS	0	IO	On / Low / Up	On / NA / Up	Mode0	3.3V	Yes	LVCMOS	PU/PD
E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6	F12, F14, F7, F9, G15, G6, J15, J6, M15, M6, P15, P6, R7	E11, E5, E7, E9, F12, G5, H12, J5, K12, L5, M12, M6	E10, E12, E14, E6, E8, F15, F5, H15, H5, K15, K5, M15, M5, P15, P5, R15, R6, T6	VDD	VDD		Power				1.2V/1.25V	0	-	0
R11, R6, R8	U10, U11	N9	U9	VDDA18_LDO	VDDA18_LDO		Power				1.8V	0	-	0
R4	U8	N6	U7	VDDA18_OSC_PLL	VDDA18_OSC_PLL		Power				1.8V	0	-	0
R4	T5	N4	U3	VDDA18_USB	VDDA18_USB		Power				1.8V	0	-	0
P11, P7, P9	T12, T9	M10, M8	T10, T12	VDDA33	VDDA33		Power				3.3V	0	-	0
R15	P5	M4	R3	VDDA33_USB	VDDA33_USB		Power				3.3V	0	-	0
D10	D13	D10	C11	VDDAR2	VDDAR2		Power				1.2V/1.25V	0	-	0
H3	H4	G4	G3	VDDAR3	VDDAR3		Power				1.2V/1.25V	0	-	0
D6, E15, L4, N15	E14, E9, F4, G16, L17, N4, T16	D12, D6, D9, E4, G13, K13, K4, N13	D10, D14, D6, H16, H4, L3, M16, T16	VDDS18	VDDS18		Power				1.8V	0	-	0
T3	U6	P4	V4	VDDS18_LDO	VDDS18_LDO		Power				1.8V	0	-	0

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
D12, D8, H15, H4, L15, P4, R15				VDDS33	VDDS33		Power				3.3V	0	-	0
	E12, E16, E7, G5, J16, M16	D11, D4, D7, F13, J13	C15, D12, D8, F16, F4, K16	VDDSHV_A	VDDS33		Power				3.3V	0	-	0
	M5	L4	P4	VDDSHV_B	VDDS33		Power				3.3V	0	-	0
	T14	N12	T14	VDDSHV_C	VDDS33		Power				3.3V	0	-	0
	J5	H4, J4	K4, M4	VDDSHV_D	VDDS1833_FLASH0		Power				1.8V/3.3V	0	-	0
	P16	M13	P16	VDDSHV_E	VDDS1833_FLASH1		Power				1.8V/3.3V	0	-	0
	T7	N5	U5	VDDSHV_F	VDDS33		Power				3.3V	0	-	0
		F1, J1		VDDSHV_G	VDDS1833_FLASH0-SIP		Power				1.8V/3.3V	0	-	0
T4	V7	N8	T8	VDD_TEMP	VDD_TEMP		Power				1.8V	0	-	0
J16	K17	H13	J17	VNWA	VNWA		Power				1.2V/1.25V	0	-	0
N3	P3	K3	N3	VPP	VPP		Power				VPP	0	-	0

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2, V18	A1, A20, F15, F6, G10, G11, G12, G13, G14, G7, G8, G9, H10, H11, H12, H13, H14, H7, H8, H9, J10, J11, J12, J13, J14, J7, J8, J9, K10, K11, K12, K13, K14, K7, K8, K9, L10, L11, L12, L13, L14, L7, L8, L9, M10, M11, M12, M13, M14, M7, M8, M9, N10, N11, N12, N13, N14, N7, N8, N9, P10, P11, P12, P13, P14, P7, P8, P9, R14, R15, R6, V2, V5, W2, Y1, Y20	A1, A16, E10, E12, E6, E8, F10, F11, F5, F6, F7, F8, F9, G10, G11, G12, G6, G7, G8, G9, H10, H11, H5, H6, H7, H8, H9, J10, J11, J12, J6, J7, J8, J9, K10, K11, K5, K6, K7, K8, K9, L10, L11, L12, L6, L7, L8, L9, M5, M7, R2, R3, R4, T1, T16	A1, A19, D16, D4, E15, E5, F10, F11, F12, F13, F14, F6, F7, F8, F9, G10, G11, G12, G13, G14, G6, G7, G8, G9, H10, H11, H12, H13, H14, H6, H7, H8, H9, J10, J11, J12, J13, J14, J6, J7, J8, J9, K10, K11, K12, K13, K14, K6, K7, K8, K9, L10, L11, L12, L13, L14, L6, L7, L8, L9, M10, M11, M12, M13, M14, M6, M7, M8, M9, N10, N11, N12, N13, N14, N6, N7, N8, N9, P10, P11, P12, P13, P14, P6, P7, P8, P9, R14, R5, R8, T4, U2, V2, V3, W1, W19	VSS	VSS		GND				VSS	0	-	0
P10, P12, P6, P8, R13, R5, V1, V16	R12, R9	M11, M9	R10, R12	VSSA	VSSA		-				-	0	Analog	0
U2	Y4	R5	V5	VSYS_MON	VSYS_MON		-				-		Analog	

Table 5-1. Pin Attributes (ZCZ, ZFG, ZEJ, ZNC Packages) (continued)

ZCZ Ball Number [1]	ZFG Ball Number [1]	ZEJ Ball Number [1]	ZNC Ball Number [1]	Ball Name [2]/ IOMUX Register [14]/ ADDRESS [15]/ DEFAULT VALUE [16]	Signal Name [3]	Mux Mode [4]	TYPE [5]	BALL STATE DURING RESET RX/TX/PULL [6]	BALL STATE AFTER RESET RX/TX/PULL [7]	MUX MODE AFTER RESET [8]	IO VOLTAGE [9]	HYS [11]	BUFFER TYPE [13]	PULL TYPE [12]
C3	G3	C3	C3	WARMRSTn WARMRSTn_CFG_REG 0x5310 0234 0x0000 0510	WARMRSTn	0	IO	On / Low / Off	On / NA / Off	Mode0	3.3V		FS_OPEN_DRAIN	
T1	Y3	T3	W3	XTAL_XI	XTAL_XI	0	I			More0	1.8V	Yes	OSC	
R1	Y2	T2	W2	XTAL_XO	XTAL_XO	0	O			Mode0	1.8V		OSC	

5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

Note

Signal names and descriptions provided in each Signal Descriptions table, represent the pin multiplexed signal function which is implemented at the pin and selected via IOMUX pad configuration registers. Some device subsystems provide secondary multiplexing of signal functions, which are not described in these tables. For more information on secondary multiplexed signal functions, see the respective peripheral chapter of the device TRM.

2. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input, Output, or simultaneously Input and Output
   - ID = Input with open-drain output function
   - OD = Output, with open-drain output function
   - IOD = Input, Output, or simultaneously Input and Output, with open-drain output function
   - IOZ = Input, Output, or simultaneously Input and Output, with three-state output function
   - OZ = Output with three-state output function
   - A = Analog
   - CAP = LDO capacitor
   - PWR = Power
   - GND = Ground
3. **DESCRIPTION:** Description of the signal
4. **BALL:** Associated ball number

For more information on the I/O cell configurations, see the *Pad Configuration Registers* section within the *Device Configuration* chapter of the device TRM.

5.3.1 ADC

Table 5-2. ADC0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC0_AIN0	-	ADC Analog Input 0 (+IN0) CMPSSA0: inH (+IN)	V15	W13	P11	W12
ADC0_AIN1	-	ADC Analog Input 1 (-IN0) CMPSSA0: inL (-IN)	U15	U13	N11	V12
ADC0_AIN2	-	ADC Analog Input 2 (+IN1) CMPSSA1: inH (+IN)	T14	W14	R11	V13
ADC0_AIN3	-	ADC Analog Input 3 (-IN1) CMPSSA1: inL (-IN)	U14	V14	P12	U11
ADC0_AIN4	-	ADC Analog Input 4 (+IN2) CMPSSA2: inH (+IN)	U13	Y14	T12	W13
ADC0_AIN5	-	ADC Analog Input 5 (-IN2) CMPSSA2: inL (-IN)	R14	W15	R12	U13
ADC0_AIN6	-	ADC Analog Input 6		Y15	T13	W14

Table 5-3. ADC1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC1_AIN0	-	ADC Analog Input 0 (+IN0) CMPSSA2: inH (+IN)	T11	W12	R10	
ADC1_AIN1	-	ADC Analog Input 1 (-IN0) CMPSSA2: inL (-IN)	U11	V12	N10	
ADC1_AIN2	-	ADC Analog Input 2 (+IN1) CMPSSA3: inH (+IN)	T12	Y11	P10	
ADC1_AIN3	-	ADC Analog Input 3 (-IN1) CMPSSA3: inL (-IN)	V12	W11	P9	
ADC1_AIN4	-	ADC Analog Input 4 (+IN2) CMPSSA4: inH (+IN)	U12	Y10	T9	
ADC1_AIN5	-	ADC Analog Input 5 (-IN2) CMPSSA4: inL (-IN)	R12	W10	R9	
ADC1_AIN6	-	ADC Analog Input 6		W9	R8	

Table 5-4. ADC2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC2_AIN0	-	ADC Analog Input 0 (+IN0) CMPSSA4: inH (+IN)	R10	W8	R7	W8
ADC2_AIN1	-	ADC Analog Input 1 (-IN0) CMPSSA4: inL (-IN)	T10	Y7	P7	V9
ADC2_AIN2	-	ADC Analog Input 2 (+IN1) CMPSSA5: inH (+IN)	U10	Y6	P8	V6
ADC2_AIN3	-	ADC Analog Input 3 (-IN1) CMPSSA5: inL (-IN)	T9	W7	P6	V7
ADC2_AIN4	-	ADC Analog Input 4 (+IN2) CMPSSA6: inH (+IN)	V9	W6	R6	W9
ADC2_AIN5	-	ADC Analog Input 5 (-IN2) CMPSSA6: inL (-IN)	T8	V9	N7	V8
ADC2_AIN6	-	ADC Analog Input 6		Y5	T6	W7

5.3.1.1 ADC-CMPSS Signal Connections

In each ADC, three sets of differential pins shall be shared with pins of three CMPSSA . These pins are demonstrated in Figure 5-5 and Table 5-5 where the CHSEL values determine how the inputs are fed into ADC.

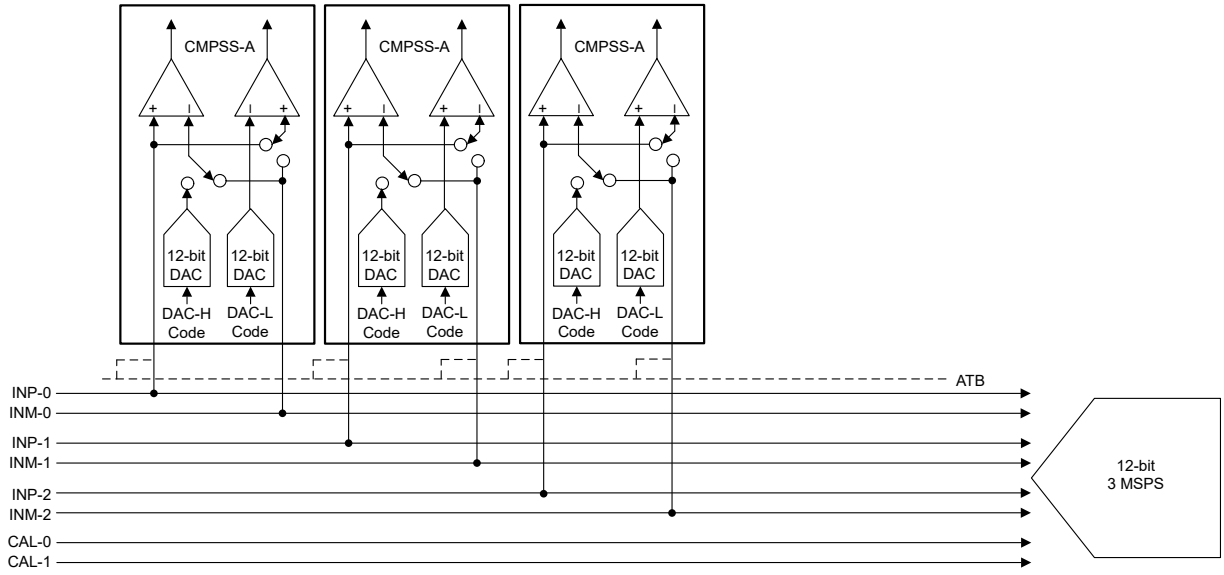


Figure 5-5. CMPSS and ADC Connections

Note

The ADC sampling speed for AM261x is 3MSPS.

Table 5-5. Connectivity between ADC Inputs to CMPSS Signals

Signal/Pin Name	ADC Input	CMPSS Input
ADC0 Channels		
ADC0_AIN0	ADC0:inp0 (+IN0)	CMPSSA0:inH (+IN)
ADC0_AIN1	ADC0:inm0 (-IN0)	CMPSSA0:inL (-IN)
ADC0_AIN2	ADC0:inp1 (+IN1)	CMPSSA1:inH (+IN)
ADC0_AIN3	ADC0:inm1 (-IN1)	CMPSSA1:inL (-IN)
ADC0_AIN4	ADC0:inp2 (+IN2)	CMPSSA2:inH (+IN)
ADC0_AIN5	ADC0:inm2 (-IN2)	CMPSSA2:inL (-IN)
ADC0_AIN6	ADC0:inm3 (-IN3)	X
ADC_CAL0	ADC0:inp3 (+IN3)	X
ADC1 Channels		
ADC1_AIN0	ADC1:inp0 (+IN0)	CMPSSA2:inH (+IN)
ADC1_AIN1	ADC1:inm0 (-IN0)	CMPSSA2:inL (-IN)
ADC1_AIN2	ADC1:inp1 (+IN1)	CMPSSA3:inH (+IN)
ADC1_AIN3	ADC1:inm1 (-IN1)	CMPSSA3:inL (-IN)
ADC1_AIN4	ADC1:inp2 (+IN2)	CMPSSA4:inH (+IN)
ADC1_AIN5	ADC1:inm2 (-IN2)	CMPSSA4:inL (-IN)
ADC1_AIN6	ADC1:inm3 (-IN3)	X
ADC_CAL0	ADC1:inp3 (+IN3)	X
ADC2 Channels		

Table 5-5. Connectivity between ADC Inputs to CMPSS Signals (continued)

Signal/Pin Name	ADC Input	CMPSS Input
ADC2_AIN0	ADC2:inp0 (+IN0)	CMPSSA4:inH (+IN)
ADC2_AIN1	ADC2:inm0 (-IN0)	CMPSSA4:inL (-IN)
ADC2_AIN2	ADC2:inp1 (+IN1)	CMPSSA5:inH (+IN)
ADC2_AIN3	ADC2:inm1 (-IN1)	CMPSSA5:inL (-IN)
ADC2_AIN4	ADC2:inp2 (+IN2)	CMPSSA6:inH (+IN)
ADC2_AIN5	ADC2:inm2 (-IN2)	CMPSSA6:inL (-IN)
ADC2_AIN6	ADC2:inm3 (-IN3)	X
ADC_CAL0	ADC2:inp3 (+IN3)	X

Note

In the **ADC Input** column in ADC-CMPSS Signal Connectivity Table above, "inp" stands for positive inputs and "inm" stands for negative inputs.

5.3.2 ADC_CAL

Table 5-6. ADC_CAL Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_CAL0 (1) (2)	-	ADC Calibration Pin 0	U16	V16	R13	U15

(1) This pin is shared between ADC[0:2].
(2) This pin is tied to Analog input channel ADCIN[7] for each ADC[0:2].

5.3.3 ADC VREF

Table 5-7. ADC_VREF Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_VREFHI0	-	ADC Reference (Positive)				V11
ADC_VREFHI1 (2)	-	ADC Reference (Positive)	V14	Y12	T10	V11
ADC_VREFHI2	-	ADC Reference (Positive)	V10	Y8	T7	V10
ADC_VREFLO0 (1)	-	ADC Reference (Negative)				W11
ADC_VREFLO1 (3)	-	ADC Reference (Negative)	V13	Y13	T11	W11
ADC_VREFLO2 (1)	-	ADC Reference (Negative)	V11	Y9	T8	W10

(1) This pin can be connected (shorted) to analog ground (VSSA).
(2) This pin can be connected (shorted) to ADC_VREFHI0.
(3) This pin can be connected (shorted) to ADC_VREFLO0.

5.3.4 CPSW

Table 5-8. CPSW0 RGMII1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RGMII1_RXC	I	RGMII Receive Clock	E16, R17	F19, W20	E13, P16	D19, V19
RGMII1_RX_CTL	I	RGMII Receive Control	F16, R18	G19, V19	D15, M14	E19, U17
RGMII1_TXC	O	RGMII Transmit Clock	C16, N18	B20, U20	L15	B18, R18
RGMII1_TX_CTL	O	RGMII Transmit Control	A17, M18	E18, T20	M16	A18, T19
RGMII1_RD0	I	RGMII Receive Data 0	F18, U17	H20, Y18	D14, P14	G18, W17
RGMII1_RD1	I	RGMII Receive Data 1	G16, T17	H19, W18	D16, P15	F18, V17
RGMII1_RD2	I	RGMII Receive Data 2	E17, U18	H17, Y19	R16	E17, W18
RGMII1_RD3	I	RGMII Receive Data 3	E18, T18	G20, W19	N14	F19, V18
RGMII1_TD0	O	RGMII Transmit Data 0	B18, P16	F17, V18	N15	D18, U18
RGMII1_TD1	O	RGMII Transmit Data 1	B17, P17	D20, V20	N16	C18, U19
RGMII1_TD2	O	RGMII Transmit Data 2	D16, P18	C20, U19	L13	B19, R17
RGMII1_TD3	O	RGMII Transmit Data 3	C17, N17	D19, T19	M15	C17, T18

Table 5-9. CPSW0 RGMII2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RGMII2_RXC	I	RGMII Receive Clock	K15	N20	H15	L18
RGMII2_RX_CTL	I	RGMII Receive Control	K16	L20	G15	J19
RGMII2_TXC	O	RGMII Transmit Clock	H18	M19	F16	K18
RGMII2_TX_CTL	O	RGMII Transmit Control	L16	P18	H16	M19

Table 5-9. CPSW0 RGMII2 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RGMII2_RD0	I	RGMII Receive Data 0	K17	N17	K14	M18
RGMII2_RD1	I	RGMII Receive Data 1	K18	N19	H14	L19
RGMII2_RD2	I	RGMII Receive Data 2	J18	M18	G16	K19
RGMII2_RD3	I	RGMII Receive Data 3	J17	M20	J14	L17
RGMII2_TD0	O	RGMII Transmit Data 0	M16	P20	J15	N18
RGMII2_TD1	O	RGMII Transmit Data 1	M15	P19	J16	N19
RGMII2_TD2	O	RGMII Transmit Data 2	H17	K20	F15	H19
RGMII2_TD3	O	RGMII Transmit Data 3	H16	L19	G14	H18

Table 5-10. CPSW0 RMII1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RMII1_CRS_DV	I	RMII Carrier Sense / Data Valid	D17, P18	E19, U19	L13	R17
RMII1_REF_CLK	IO	RMII Reference Clock	E16, R17	F19, W20	E13, P16	D19, V19
RMII1_RX_ER	I	RMII Receive Data Error	F15, R18	F20, V19	M14	E18, U17
RMII1_TX_EN	O	RMII Transmit Enable	A17, M18	E18, T20	M16	A18, T19
RMII1_RXD0	I	RMII Receive Data 0	F18, U17	H20, Y18	D14, P14	G18, W17
RMII1_RXD1	I	RMII Receive Data 1	G16, T17	H19, W18	D16, P15	F18, V17
RMII1_TXD0	O	RMII Transmit Data 0	B18, P16	F17, V18	N15	D18, U18
RMII1_TXD1	O	RMII Transmit Data 1	B17, P17	D20, V20	N16	C18, U19

Table 5-11. CPSW0 RMII2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
RMII2_CRS_DV	I	RMII Carrier Sense / Data Valid	G18	J20	E16	J18
RMII2_REF_CLK	IO	RMII Reference Clock	K15	N20	H15	L18
RMII2_RX_ER	I	RMII Receive Data Error	G17	K19	F14	G17
RMII2_TX_EN	O	RMII Transmit Enable	L16	P18	H16	M19
RMII2_RXD0	I	RMII Receive Data 0	K17	N17	K14	M18
RMII2_RXD1	I	RMII Receive Data 1	K18	N19	H14	L19
RMII2_TXD0	O	RMII Transmit Data 0	M16	P20	J15	N18
RMII2_TXD1	O	RMII Transmit Data 1	M15	P19	J16	N19

Table 5-12. CPSW0 MII1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MII1_COL	I	MII Collision Detected	C18, P15	E20, W17	T15	W16
MII1_CRS	I	MII Carrier Sense	D17, R16	E19, Y17	R15	V16
MII1_RXCLK	I	MII Receive Clock	E16, R17	F19, W20	E13, P16	D19, V19
MII1_RXDV	I	MII Receive Data Valid	F16, R18	G19, V19	D15, M14	E19, U17
MII1_RX_ER	I	MII Receive Data Error	F15, T16	F20, Y16	T14	E18, W15
MII1_TXCLK	I	MII Transmit Clock	C16, N18	B20, U20	L15	B18, R18
MII1_TX_EN	O	MII Transmit Enable	A17, M18	E18, T20	M16	A18, T19

Table 5-12. CPSW0 MII1 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MII1_RXD0	I	MII Receive Data 0	F18, U17	H20, Y18	D14, P14	G18, W17
MII1_RXD1	I	MII Receive Data 1	G16, T17	H19, W18	D16, P15	F18, V17
MII1_RXD2	I	MII Receive Data 2	E17, U18	H17, Y19	R16	E17, W18
MII1_RXD3	I	MII Receive Data 3	E18, T18	G20, W19	N14	F19, V18
MII1_TXD0	O	MII Transmit Data 0	B18, P16	F17, V18	N15	D18, U18
MII1_TXD1	O	MII Transmit Data 1	B17, P17	D20, V20	N16	C18, U19
MII1_TXD2	O	MII Transmit Data 2	D16, P18	C20, U19	L13	B19, R17
MII1_TXD3	O	MII Transmit Data 3	C17, N17	D19, T19	M15	C17, T18

Table 5-13. CPSW0 MII2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MII2_COL	I	MII Collision Detected	F17	J19	E15	
MII2_CRS	I	MII Carrier Sense	G18	J20	E16	J18
MII2_RXCLK	I	MII Receive Clock	K15	N20	H15	L18
MII2_RXDV	I	MII Receive Data Valid	K16	L20	G15	J19
MII2_RX_ER	I	MII Receive Error	G17	K19	F14	G17
MII2_TXCLK	I	MII Transmit Clock	H18	M19	F16	K18
MII2_TX_EN	O	MII Transmit Enable	L16	P18	H16	M19
MII2_RXD0	I	MII Receive Data 0	K17	N17	K14	M18
MII2_RXD1	I	MII Receive Data 1	K18	N19	H14	L19
MII2_RXD2	I	MII Receive Data 2	J18	M18	G16	K19
MII2_RXD3	I	MII Receive Data 3	J17	M20	J14	L17
MII2_TXD0	O	MII Transmit Data 0	M16	P20	J15	N18
MII2_TXD1	O	MII Transmit Data 1	M15	P19	J16	N19
MII2_TXD2	O	MII Transmit Data 2	H17	K20	F15	H19
MII2_TXD3	O	MII Transmit Data 3	H16	L19	G14	H18

Table 5-14. MDIO0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MDIO0_MDC	O	MDIO Clock	M17	T18	L14	R19
MDIO0_MDIO	IO	MDIO Data	N16	R17	L16	P18

5.3.5 CPTS

Table 5-15. CPTS0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
CPTS0_TS_SYNC	O	CPTS Time Stamp Counter Bit Output	A16	A19	C16	

5.3.6 DAC

Table 5-16. DAC Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
DAC_OUT	-	DAC Output	T5	W4	T5	W6
DAC_VREF0 (1) (2)	-	DAC Voltage Reference 0	T13	U15	P13	V14

(1) See the *Layout Guidelines* sections for details on connecting these pins.
(2) This pin can be connected (shorted) to VDDA18_LDO.

5.3.7 EPWM

Table 5-17. EPWM0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM0_A	O	EPWM Output A	B2	B3	A4	B5
EPWM0_B	O	EPWM Output B	B1	C3	A5	A6

Table 5-18. EPWM1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM1_A	O	EPWM Output A	D3	A2	B4	A5
EPWM1_B	O	EPWM Output B	D2, E4	A3, D1	C1, C5	A4, B3

Table 5-19. EPWM2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM2_A	O	EPWM Output A	C2	B1	A3	A3
EPWM2_B	O	EPWM Output B	C1	B2	A2	B4

Table 5-20. EPWM3 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM3_A	O	EPWM Output A	E2	C1	B2	A2
EPWM3_B	O	EPWM Output B	E1, E3	C2, F2	C4, E3	B2, E3

Table 5-21. EPWM4 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM4_A	O	EPWM Output A	D1	D2	B1	B1
EPWM4_B	O	EPWM Output B	D2, E4	A3, D1	C1, C5	A4, B3

Table 5-22. EPWM5 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM5_A	O	EPWM Output A	F2	E2	C2	C2

Table 5-22. EPWM5 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM5_B	O	EPWM Output B	F1, G2	E1, G1	D1, D3	C1, D1

Table 5-23. EPWM6 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM6_A	O	EPWM Output A	B9, E1, E3	B11, C2, F2	C4, D8, E3	B10, B2, E3
EPWM6_B	O	EPWM Output B	A9, F3	A11, F1	C10, F4	A11, E2

Table 5-24. EPWM7 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM7_A	O	EPWM Output A	C9, F4	D11, G2	B9, D2	D2
EPWM7_B	O	EPWM Output B	A10, F1, G4	A12, G1, J2	B10, D1	D1

Table 5-25. EPWM8 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM8_A	O	EPWM Output A	B10, G3	D10, H2	A9, E2	E1
EPWM8_B	O	EPWM Output B	D9, G2, H2	C9, E1, H1	C11, D3, E1	C1, F1

Table 5-26. EPWM9 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EPWM9_A	O	EPWM Output A	G1, N1	K4, R2	F2, M2	F2, N2
EPWM9_B	O	EPWM Output B	H2, J2, N4	H1, L2, R1	E1, F3, N1	F1, G1, N1

5.3.8 EQEP

Table 5-27. EQEP0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EQEP0_A	I	EQEP Quadrature Input A	B14, U18	A16, Y19	D13, R16	B15, W18
EQEP0_B	I	EQEP Quadrature Input B	A14, T18	B16, W19	C13, N14	A15, V18
EQEP0_INDEX	IO	EQEP Index	D11, N18	D15, U20	B13, L15	B14, R18
EQEP0_STROBE	IO	EQEP Strobe	C12, M18	C14, T20	C12, M16	A14, T19

Table 5-28. EQEP1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EQEP1_A	I	EQEP Quadrature Input A	D15, P16	C18, V18	N15	B16, U18
EQEP1_B	I	EQEP Quadrature Input B	C15, P17	C19, V20	N16	B17, U19
EQEP1_INDEX	IO	EQEP Index	A12, N17, P2	A14, T19, U2	M15, P3	T1, T18

Table 5-28. EQEP1 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EQEP1_STROBE	IO	EQEP Strobe	B16, P18	B19, U19	C15, L13	R17

5.3.9 FSI

Table 5-29. FSIRX0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
FSIRX0_CLK	I	FSI Clock	A10, T17	A12, W18	B10, P15	V17
FSIRX0_DATA0	I	FSI Data 0	B10, U18	D10, Y19	A9, R16	W18
FSIRX0_DATA1	I	FSI Data 1	D9, T18	C9, W19	C11, N14	V18

Table 5-30. FSITX0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
FSITX0_CLK	O	FSI Clock	A11, R17	A13, W20	A12, P16	A12, V19
FSITX0_DATA0	O	FSI Data 0	C10, R18	B12, V19	A10, M14	B12, U17
FSITX0_DATA1	O	FSI Data 1	B11, U17	C12, Y18	A11, P14	B11, W17

5.3.10 GPIO

Table 5-31. GPIO Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO0	IO	General Purpose Input/Output	P1	U4	N3	R1
GPIO1	IO	General Purpose Input/Output	R3	T2	M3	R2
GPIO2	IO	General Purpose Input/Output	N2	M3	L2	M2
GPIO3 (1)	IO	General Purpose Input/Output (SOP0)	N1	R2	M2	N2
GPIO4 (2)	IO	General Purpose Input/Output (SOP1)	N4	R1	N1	N1
GPIO5	IO	General Purpose Input/Output	M4	T1	L3	P2
GPIO6	IO	General Purpose Input/Output	P3	U1	N2	P1
GPIO7	IO	General Purpose Input/Output	M1	P1	J3	K2
GPIO8	IO	General Purpose Input/Output	L1	P2	K1	L1
GPIO9	IO	General Purpose Input/Output	L2	N2	K2	J2
GPIO10	IO	General Purpose Input/Output	K1	N1	J2	K1
GPIO11	IO	General Purpose Input/Output	C11	B13	B11	C13
GPIO12 (5)	IO	General Purpose Input/Output (SOP2)	A11	A13	A12	A12
GPIO13 (6)	IO	General Purpose Input/Output (SOP3)	C10	B12	A10	B12
GPIO14	IO	General Purpose Input/Output	B11	C12	A11	B11
GPIO15	IO	General Purpose Input/Output	C9	D11	B9	
GPIO16	IO	General Purpose Input/Output	A10	A12	B10	
GPIO17	IO	General Purpose Input/Output	B10	D10	A9	
GPIO18	IO	General Purpose Input/Output	D9	C9	C11	

Table 5-31. GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO19	IO	General Purpose Input/Output	A9	A11	C10	A11
GPIO100	IO	General Purpose Input/Output	M15	P19	J16	N19
GPIO101	IO	General Purpose Input/Output	H17	K20	F15	H19
GPIO102	IO	General Purpose Input/Output	H16	L19	G14	H18
GPIO103	IO	General Purpose Input/Output	F15	F20		E18
GPIO104	IO	General Purpose Input/Output	C18	E20		
GPIO105	IO	General Purpose Input/Output	D17	E19		
GPIO106	IO	General Purpose Input/Output	D18	G18		C19
GPIO107	IO	General Purpose Input/Output	E16	F19	E13	D19
GPIO108	IO	General Purpose Input/Output	F16	G19	D15	E19
GPIO109	IO	General Purpose Input/Output	F18	H20	D14	G18
GPIO110	IO	General Purpose Input/Output	G16	H19	D16	F18
GPIO111	IO	General Purpose Input/Output	E17	H17		E17
GPIO112	IO	General Purpose Input/Output	E18	G20		F19
GPIO113	IO	General Purpose Input/Output	C16	B20		B18
GPIO114	IO	General Purpose Input/Output	A17	E18		A18
GPIO115	IO	General Purpose Input/Output	B18	F17		D18
GPIO116	IO	General Purpose Input/Output	B17	D20		C18
GPIO117	IO	General Purpose Input/Output	D16	C20		B19
GPIO118	IO	General Purpose Input/Output	C17	D19		C17
GPIO119	IO	General Purpose Input/Output	D15	C18		B16
GPIO120	IO	General Purpose Input/Output	C15	C19		B17
GPIO121	IO	General Purpose Input/Output	P2	U2	P3	T1
GPIO122	IO	General Purpose Input/Output	B16	B19	C15	
GPIO123	IO	General Purpose Input/Output	D14	C16	A15	
GPIO124	IO	General Purpose Input/Output	A16	A19	C16	
GPIO125	IO	General Purpose Input/Output	D13	B17	C14	
GPIO126	IO	General Purpose Input/Output	B15	A18	B16	A17
GPIO127	IO	General Purpose Input/Output	C13	A17	A14	A16
GPIO128	IO	General Purpose Input/Output	A15	B18	B15	
GPIO129	IO	General Purpose Input/Output	C14	D17	B14	
GPIO130	IO	General Purpose Input/Output	B14	A16	D13	B15
GPIO131	IO	General Purpose Input/Output	A14	B16	C13	A15
GPIO132	IO	General Purpose Input/Output	C12	C14	C12	A14
GPIO133	IO	General Purpose Input/Output	D11	D15	B13	B14
GPIO134 (4)	IO	General Purpose Input/Output	B13	B15	B12	B13
GPIO135 (3)	IO	General Purpose Input/Output	A13	A15	A13	A13
GPIO136	IO	General Purpose Input/Output	B12	B14		
GPIO137	IO	General Purpose Input/Output	A12	A14		
GPIO138	IO	General Purpose Input/Output	M2	M1	H1	J3
GPIO139	IO	General Purpose Input/Output	V2	V1	R1	V1
GPIO140	IO	General Purpose Input/Output	U3	W1	P1	U1
GPIO20	IO	General Purpose Input/Output	B9	B11	D8	B10
GPIO21	IO	General Purpose Input/Output	B8	B10	B8	A10

Table 5-31. GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO22	IO	General Purpose Input/Output	A8	A10	C9	B9
GPIO23	IO	General Purpose Input/Output	D7	B9	B7	
GPIO24	IO	General Purpose Input/Output	C8	A9	A8	
GPIO25	IO	General Purpose Input/Output	C7	C7	C8	C9
GPIO26	IO	General Purpose Input/Output	B7	D8	A7	A9
GPIO27	IO	General Purpose Input/Output	A7	A8	A6	A8
GPIO28	IO	General Purpose Input/Output	A6	B8	B6	B8
GPIO29	IO	General Purpose Input/Output	R17	W20	P16	V19
GPIO30	IO	General Purpose Input/Output	R18	V19	M14	U17
GPIO31	IO	General Purpose Input/Output	U17	Y18	P14	W17
GPIO32	IO	General Purpose Input/Output	T17	W18	P15	V17
GPIO33	IO	General Purpose Input/Output	U18	Y19	R16	W18
GPIO34	IO	General Purpose Input/Output	T18	W19	N14	V18
GPIO35	IO	General Purpose Input/Output	N18	U20	L15	R18
GPIO36	IO	General Purpose Input/Output	M18	T20	M16	T19
GPIO37	IO	General Purpose Input/Output	P16	V18	N15	U18
GPIO38	IO	General Purpose Input/Output	P17	V20	N16	U19
GPIO39	IO	General Purpose Input/Output	P18	U19	L13	R17
GPIO40	IO	General Purpose Input/Output	N17	T19	M15	T18
GPIO41	IO	General Purpose Input/Output	N16	R17	L16	P18
GPIO42	IO	General Purpose Input/Output	M17	T18	L14	R19
GPIO43	IO	General Purpose Input/Output	B2	B3	A4	B5
GPIO44	IO	General Purpose Input/Output	B1	C3	A5	A6
GPIO45	IO	General Purpose Input/Output	D3	A2	B4	A5
GPIO46	IO	General Purpose Input/Output	D2	A3	C5	A4
GPIO47	IO	General Purpose Input/Output	C2	B1	A3	A3
GPIO48	IO	General Purpose Input/Output	C1	B2	A2	B4
GPIO49	IO	General Purpose Input/Output	E2	C1	B2	A2
GPIO50	IO	General Purpose Input/Output	E3	C2	C4	B2
GPIO51	IO	General Purpose Input/Output	D1	D2	B1	B1
GPIO52	IO	General Purpose Input/Output	E4	D1	C1	B3
GPIO53	IO	General Purpose Input/Output	F2	E2	C2	C2
GPIO54	IO	General Purpose Input/Output	G2	E1	D3	C1
GPIO55	IO	General Purpose Input/Output	E1	F2	E3	E3
GPIO56	IO	General Purpose Input/Output	F3	F1	F4	E2
GPIO57	IO	General Purpose Input/Output	F4	G2	D2	D2
GPIO58	IO	General Purpose Input/Output	F1	G1	D1	D1
GPIO59	IO	General Purpose Input/Output	G3	H2	E2	E1
GPIO60	IO	General Purpose Input/Output	H2	H1	E1	F1
GPIO61 (7) (8)	IO	General Purpose Input/Output	G1	K4	F2	F2
GPIO62	IO	General Purpose Input/Output	J2	L2	F3	G1
GPIO63	IO	General Purpose Input/Output	G4	J2		
GPIO64	IO	General Purpose Input/Output	J3	J1		
GPIO65	IO	General Purpose Input/Output	H1	J3		

Table 5-31. GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPIO66	IO	General Purpose Input/Output	J1	K2	G3	
GPIO67	IO	General Purpose Input/Output	K2	K1	G2	G2
GPIO68	IO	General Purpose Input/Output	J4	L4	H3	H1
GPIO69	IO	General Purpose Input/Output	K4	L1	H2	H2
GPIO70	IO	General Purpose Input/Output	K3	M2	G1	J1
GPIO71	IO	General Purpose Input/Output	V17	W16	R14	V15
GPIO72	IO	General Purpose Input/Output	T16	Y16	T14	W15
GPIO73	IO	General Purpose Input/Output	P15	W17	T15	W16
GPIO74	IO	General Purpose Input/Output	R16	Y17	R15	V16
GPIO75	IO	General Purpose Input/Output	L3	T3	M1	L2
GPIO76	IO	General Purpose Input/Output	M3	R4	L1	M1
GPIO77	IO	General Purpose Input/Output	B6	B7		
GPIO78	IO	General Purpose Input/Output	A4	A6		
GPIO79	IO	General Purpose Input/Output	B5	B6		
GPIO80	IO	General Purpose Input/Output	B4	A5		
GPIO81	IO	General Purpose Input/Output	A3	B5		
GPIO82	IO	General Purpose Input/Output	A2	A4		
GPIO83	IO	General Purpose Input/Output	C6	B4		
GPIO84	IO	General Purpose Input/Output	A5	A7		
GPIO85	IO	General Purpose Input/Output	L17	R19	K15	N17
GPIO86	IO	General Purpose Input/Output	L18	R20	K16	P19
GPIO87	IO	General Purpose Input/Output	G17	K19	F14	G17
GPIO88	IO	General Purpose Input/Output	F17	J19	E15	
GPIO89	IO	General Purpose Input/Output	G18	J20	E16	J18
GPIO90	IO	General Purpose Input/Output	G15	J18	E14	G19
GPIO91	IO	General Purpose Input/Output	K15	N20	H15	L18
GPIO92	IO	General Purpose Input/Output	K16	L20	G15	J19
GPIO93	IO	General Purpose Input/Output	K17	N17	K14	M18
GPIO94	IO	General Purpose Input/Output	K18	N19	H14	L19
GPIO95	IO	General Purpose Input/Output	J18	M18	G16	K19
GPIO96	IO	General Purpose Input/Output	J17	M20	J14	L17
GPIO97	IO	General Purpose Input/Output	H18	M19	F16	K18
GPIO98	IO	General Purpose Input/Output	L16	P18	H16	M19
GPIO99	IO	General Purpose Input/Output	M16	P20	J15	N18

(1) The GPIO3 pin is also used as SOP0 bootmode configuration pin.
(2) The GPIO4 pin is also used as SOP1 bootmode configuration pin.
(3) GPIO135 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(4) GPIO134 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(5) The GPIO12 pin is also used as SOP2 bootmode configuration pin.
(6) The GPIO13 pin is also used as SOP3 bootmode configuration pin.
(7) In OSPI boot mode, the AM261x ROM code configures GPIO61 as OSPI0_RESET_OUT0 and drives the pin low to reset an external OSPI device during this boot mode. However, due to a configuration in the OSPI controller, this pin does not de-assert after and external OSPI flash device resets, thus holding any external flash device in reset and causing the boot to fail. This means that GPIO61 is pulled high and then configured low until after boot is completed, which may affect certain applications. For more information, see the AM261x Errata Document.
(8) For additional information on OSPI flash reset, see OSPI Reset within the *Applications, Implementation and Layout* section.

5.3.11 GPMC0

Table 5-32. GPMC0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPMC0_ADVn_ALE	O	GPMC Address Valid (active low) or Address Latch Enable	A8	A10	C9	B9
GPMC0_CLK (1)	IO	GPMC Clock	L3	T3	M1	L2
GPMC0_CLKLB (2)	IO	GPMC Clock Loopback	B15	A18	B16	A17
GPMC0_DIR	O	GPMC Data Bus Signal Direction Control	B10	D10	A9	
GPMC0_OEn_REn	O	GPMC Output Enable (active low) or Read Enable (active low)	A10, B14, C8	A12, A16, A9	A8, B10, D13	B15
GPMC0_WEn	O	GPMC Write Enable (active low)	C14, D7	B9, D17	B14, B7	
GPMC0_WPn	O	GPMC Flash Write Protect (active low)	D9	C9	C11	
GPMC0_A0	O	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	C11	B13	B11	C13
GPMC0_A1	O	GPMC Address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	C2	B1	A3	A3
GPMC0_A2	O	GPMC Address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	D2	A3	C5	A4
GPMC0_A3	O	GPMC Address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	B2	B3	A4	B5
GPMC0_A4	O	GPMC Address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	D3	A2	B4	A5
GPMC0_A5	O	GPMC Address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	B16	B19	C15	
GPMC0_A6	O	GPMC Address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	B1	C3	A5	A6
GPMC0_A7	O	GPMC Address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	A11	A13	A12	A12
GPMC0_A8	O	GPMC Address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	A16	A19	C16	
GPMC0_A9	O	GPMC Address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	E3	C2	C4	B2
GPMC0_A10	O	GPMC Address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	D1	D2	B1	B1
GPMC0_A11	O	GPMC Address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	E4	D1	C1	B3
GPMC0_A12	O	GPMC Address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	F2	E2	C2	C2

Table 5-32. GPMC0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPMC0_A13	O	GPMC Address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	E2	C1	B2	A2
GPMC0_A14	O	GPMC Address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C1	B2	A2	B4
GPMC0_A15	O	GPMC Address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C12	C14	C12	A14
GPMC0_A16	O	GPMC Address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C10	B12	A10	B12
GPMC0_A17	O	GPMC Address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C15	C19		B17
GPMC0_A18	O	GPMC Address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	P2	U2	P3	T1
GPMC0_A19	O	GPMC Address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	D15	C18		B16
GPMC0_A20	O	GPMC Address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	D17, F3	E19, F1	F4	E2
GPMC0_A21	O	GPMC Address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	C18	E20		
GPMC0_AD0	IO	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	V17	W16	R14	V15
GPMC0_AD1	IO	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	T16	Y16	T14	W15
GPMC0_AD2	IO	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	P15	W17	T15	W16
GPMC0_AD3	IO	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode	F1	G1	D1	D1
GPMC0_AD4	IO	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode	F4	G2	D2	D2
GPMC0_AD5	IO	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode	G2	E1	D3	C1
GPMC0_AD6	IO	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode	A9	A11	C10	A11

Table 5-32. GPMC0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
GPMC0_AD7	IO	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode	D11	D15	B13	B14
GPMC0_AD8	IO	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode	B9, E1	B11, F2	D8, E3	B10, E3
GPMC0_AD9	IO	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode	R16	Y17	R15	V16
GPMC0_AD10	IO	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	D14	C16	A15	
GPMC0_AD11	O	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	N1	R2	M2	N2
GPMC0_AD12	O	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	N4	R1	N1	N1
GPMC0_AD13	IO	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	D13	B17	C14	
GPMC0_AD14	IO	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	A15	B18	B15	
GPMC0_AD15	IO	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	H2	H1	E1	F1
GPMC0_BE0n_CLE	O	GPMC Lower-Byte Enable (active low) or Command Latch Enable	C13	A17	A14	A16
GPMC0_BE1n	O	GPMC Upper-Byte Enable (active low)	B11	C12	A11	B11
GPMC0_CSn0	O	GPMC Chip Select 0 (active low)	A14, B8	B10, B16	B8, C13	A10, A15
GPMC0_CSn1	O	GPMC Chip Select 1 (active low)	G3	H2	E2	E1
GPMC0_CSn2	O	GPMC Chip Select 2 (active low)	U18	Y19	R16	W18
GPMC0_CSn3	O	GPMC Chip Select 3 (active low)	T18	W19	N14	V18
GPMC0_WAIT0	I	GPMC External Indication of Wait	C9	D11	B9	
GPMC0_WAIT1	I	GPMC External Indication of Wait	C7	C7	C8	C9

(1) The RXACTIVE bit of the MSS_IOMUX:PR0_PRU0_GPO9_CFG_REG register must be set to 0x1 and the TX_DIS bit of the MSS_IOMUX:PR0_PRU0_GPO9_CFG_REG register must be reset to 0x0 when GPMC0 is operating in synchronous mode.
(2) GPMC0_CLKLB is a clock loopback signal used internally for retiming purposes.

5.3.12 I2C

Table 5-33. I2C0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
I2C0_SCL (2)	IO	I2C Clock	A13, J3, K15	A15, J1, N20	A13, H15	A13, L18
I2C0_SDA (1)	IO	I2C Data	B13, G15, G4	B15, J18, J2	B12, E14	B13, G19

(1) I2C0_SDA is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(2) I2C0_SCL is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

Table 5-34. I2C1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
I2C1_SCL (2)	IO	I2C Clock	A14, B5, D7, J1	B16, B6, B9, K2	B7, C13, G3	A15
I2C1_SDA (1)	IO	I2C Data	A3, B14, C8, H1	A16, A9, B5, J3	A8, D13	B15

(1) I2C1_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.
(2) I2C1_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

Table 5-35. I2C2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
I2C2_SCL (2)	IO	I2C Clock	C6, C7, D11	B4, C7, D15	B13, C8	B14, C9
I2C2_SDA (1)	IO	I2C Data	A5, B7, C12	A7, C14, D8	A7, C12	A14, A9

(1) I2C2_SDA is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.
(2) I2C2_SCL is implemented with the typical LVCMOS voltage buffer and should be properly configured to operate as an Input/Output Open Drain signal type.

5.3.13 LIN

Table 5-36. LIN0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
LIN0_RXD	IO	LIN Receive Data	A7, B12, B6, G4, L17	A8, B14, B7, J2, R19	A6, K15	A8, N17
LIN0_TXD	IO	LIN Transmit Data	A12, A4, A6, J3, L18	A14, A6, B8, J1, R20	B6, K16	B8, P19

Table 5-37. LIN1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
LIN1_RXD	IO	LIN Receive Data	A9, J2, L3, M2	A11, L2, M1, T3	C10, F3, H1, M1	A11, G1, J3, L2
LIN1_TXD	IO	LIN Transmit Data	B9, G1, L2, M3	B11, K4, N2, R4	D8, F2, K2, L1	B10, F2, J2, M1

Table 5-38. LIN2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
LIN2_RXD	IO	LIN Receive Data	B8	B10	B8	A10
LIN2_TXD	IO	LIN Transmit Data	A8	A10	C9	B9

5.3.14 MCAN

Table 5-39. MCAN0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MCAN0_RX	I	MCAN Receive Data	B6, E16, G3, L17, M1	B7, F19, H2, P1, R19	E13, E2, J3, K15	D19, E1, K2, N17
MCAN0_TX	O	MCAN Transmit Data	A4, F16, H2, L1, L18	A6, G19, H1, P2, R20	D15, E1, K1, K16	E19, F1, L1, P19

Table 5-40. MCAN1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MCAN1_RX	I	MCAN Receive Data	B14, B5, F18, L2, N16	A16, B6, H20, N2, R17	D13, D14, K2, L16	B15, G18, J2, P18
MCAN1_TX	O	MCAN Transmit Data	A14, B4, G16, K1, M17	A5, B16, H19, N1, T18	C13, D16, J2, L14	A15, F18, K1, R19

5.3.15 MMC

Table 5-41. MMC0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
MMC0_CD	I	MMC/SD Card Detect	A5, D9	A7, C9	C11	
MMC0_CLK	IO	MMC/SD Clock	B6, C11	B13, B7	B11	C13
MMC0_CMD	IO	MMC/SD Command	A11, A4	A13, A6	A12	A12
MMC0_WP	I	MMC/SD Write Protect	B10, C6	B4, D10	A9	
MMC0_D0	IO	MMC/SD Data	B5, C10	B12, B6	A10	B12
MMC0_D1	IO	MMC/SD Data	B11, B4	A5, C12	A11	B11
MMC0_D2	IO	MMC/SD Data	A3, C9	B5, D11	B9	
MMC0_D3	IO	MMC/SD Data	A10, A2	A12, A4	B10	

5.3.16 OSPI

Table 5-42. OSPI0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
OSPI0_CLK	O	OSPI0 Clock	H2, K1, L2, N2	H1, M3, N1, N2	E1, J2, K2, L2	F1, J2, K1, M2
OSPI0_DQS	I	OSPI0 Data Strobe (DQS) or Loopback Clock input	L2, M1, M3	N2, P1, R4	J3, K2, L1	J2, K2, M1
OSPI0_ECC_FAIL	I	OSPI0 ECC Failure Status Pin	A9, B10, H1, K3, M2	A11, D10, J3, M1, M2	A9, C10, G1, H1	A11, J1, J3
OSPI0_LBCLKO (1)	O	OSPI0 Loopback Clock output	L3	T3	M1	L2

Table 5-42. OSPI0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
OSPI0_CSn0	O	OSPI0 Chip Select 0	H1, J2, P1	J3, L2, U4	F3, N3	G1, R1
OSPI0_CSn1	O	OSPI0 Chip Select 1	F4, R3	G2, T2	D2, M3	D2, R2
OSPI0_D0	IO	OSPI0 Data bit 0	G3, N1, N2, P1	H2, M3, R2, U4	E2, L2, M2, N3	E1, M2, N2, R1
OSPI0_D1	IO	OSPI0 Data bit 1	F1, J1, K3, N4	G1, K2, M2, R1	D1, G1, G3, N1	D1, J1, N1
OSPI0_D2	IO	OSPI0 Data bit 2	L1, M1, M4	P1, P2, T1	J3, K1, L3	K2, L1, P2
OSPI0_D3	IO	OSPI0 Data bit 3	K4, P3	L1, U1	H2, N2	H2, P1
OSPI0_D4	IO	OSPI0 Data bit 4	M1, M3, P3	P1, R4, U1	J3, L1, N2	K2, M1, P1
OSPI0_D5	IO	OSPI0 Data bit 5	K2, L1	K1, P2	G2, K1	G2, L1
OSPI0_D6	IO	OSPI0 Data bit 6	L1, L2, M4	N2, P2, T1	K1, K2, L3	J2, L1, P2
OSPI0_D7	IO	OSPI0 Data bit 7	J4, K1	L4, N1	H3, J2	H1, K1
OSPI0_RESET_OUT0(2) (3)	O	OSPI0 Reset Out 0	B9, D9, G1, G2, J1, J3	B11, C9, E1, J1, K2, K4	C11, D3, D8, F2, G3	B10, C1, F2
OSPI0_RESET_OUT1	O	OSPI0 Reset Out 1	A9, B8, H1	A11, B10, J3	B8, C10	A10, A11

(1) OSPI0_LBCLKO is a clock loopback output signal used for peripheral timing.
(2) In OSPI boot mode, the AM261x ROM code configures GPIO61 as OSPI0_RESET_OUT0 and drives the pin low to reset an external OSPI device during this boot mode. However, due to a configuration in the OSPI controller, this pin does not de-assert after and external OSPI flash device resets, thus holding any external flash device in reset and causing the boot to fail. For more information, see the AM261x Errata Document.
(3) For additional information on OSPI flash reset, see OSPI Reset within the *Applications, Implementation and Layout* section.

Table 5-43. OSPI1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
OSPI1_CLK	O	OSPI1 Clock	H2, K1, R17	H1, N1, W20	E1, J2, P16	F1, K1, V19
OSPI1_DQS	I	OSPI1 Data Strobe (DQS) or Loopback Clock input	P18	U19	L13	R17
OSPI1_ECC_FAIL	I	OSPI1 ECC Failure Status Pin	A9, M2, N17	A11, M1, T19	C10, H1, M15	A11, J3, T18
OSPI1_LBCLKO (1)	O	OSPI1 Loopback Clock output	L3	T3	M1	L2
OSPI1_CSn0	O	OSPI1 Chip Select 0	J2, P17	L2, V20	F3, N16	G1, U19
OSPI1_CSn1	O	OSPI1 Chip Select 1	F4	G2	D2	D2
OSPI1_D0	IO	OSPI1 Data bit 0	G3, N2, R18	H2, M3, V19	E2, L2, M14	E1, M2, U17
OSPI1_D1	IO	OSPI1 Data bit 1	F1, K3, U17	G1, M2, Y18	D1, G1, P14	D1, J1, W17
OSPI1_D2	IO	OSPI1 Data bit 2	T17	W18	P15	V17
OSPI1_D3	IO	OSPI1 Data bit 3	U18	Y19	R16	W18
OSPI1_D4	IO	OSPI1 Data bit 4	T18	W19	N14	V18
OSPI1_D5	IO	OSPI1 Data bit 5	N18	U20	L15	R18
OSPI1_D6	IO	OSPI1 Data bit 6	M18	T20	M16	T19
OSPI1_D7	IO	OSPI1 Data bit 7	P16	V18	N15	U18
OSPI1_RESET_OUT0	O	OSPI1 Reset Out 0	B9, G1, N16	B11, K4, R17	D8, F2, L16	B10, F2, P18
OSPI1_RESET_OUT1	O	OSPI1 Reset Out 1	B8	B10	B8	A10

(1) OSPI1_LBCLKO is a clock loopback output signal used for peripheral timing.

5.3.17 Power Supply

Table 5-44. Power Supply Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
VDD	Power	1.2V/1.25V Core supply(1)	E11, E9, F11, F9, G13, G14, G5, G6, K13, K14, K5, K6, N13, N14, N5, N6	F12, F14, F7, F9, G15, G6, J15, J6, M15, M6, P15, P6, R7	E11, E5, E7, E9, F12, G5, H12, J5, K12, L5, M12, M6	E10, E12, E14, E6, E8, F15, F5, H15, H5, K15, K5, M15, M5, P15, P5, R15, R6, T6
VDDA18_LDO (4)	Power	1.8V Analog Output	R11, R6, R8	U10, U11	N9	U9
VDDA18_OSC_PLL	Power	1.8V PLL supply		U8	N6	U7
VDDA18_USB	Power	USB 1.8V analog supply	R4	T5	N4	U3
VDDA33	Power	3.3V analog supply	P11, P7, P9	T12, T9	M10, M8	T10, T12
VDDA33_USB	Power	USB 3.3V analog supply	R15	P5	M4	R3
VDDAR2	Power	SRAM Array supply	D10	D13	D10	C11
VDDAR3	Power	SRAM Array supply	H3	H4	G4	G3
VDDS18	Power	1.8V IO supply	D6, E15, L4, N15	E14, E9, F4, G16, L17, N4, T16	D12, D6, D9, E4, G13, K13, K4, N13	D10, D14, D6, H16, H4, L3, M16, T16
VDDS18_LDO (2) (3)	Power	1.8V Digital LDO Output	T3	U6	P4	V4
VDDS1833_FLASH0	Power	1.8V/3.3V Flash 0 IO Supply		J5	H4, J4	K4, M4
VDDS1833_FLASH1	Power	1.8V/3.3V Flash 1 IO Supply		P16	M13	P16
VDDS1833_FLASH0-SIP	Power	1.8V/3.3V SIP Flash Supply. This must be shorted to VDDSHV_D(VDDS1833_FLASH0) on board. Will be used for Flash supply in future Flash SIP packages.			F1, J1	
VDDS33	Power	3.3V IO supply	D12, H15, H4, L15, P4, R15	E12, E16, E7, G5, J16, M16, M5, T14, T7	D11, D4, D7, F13, J13, L4, N12, N5	C15, D12, D8, F16, F4, K16, P4, T14, U5
VDD_TEMP	Power	VDD Temp	T4	V7	N8	T8
VNWA	Power	1.2V/1.25V N-well bias(1)	J16	K17	H13	J17
VPP	Power	eFuse ROM programming supply	N3	P3	K3	N3

Table 5-44. Power Supply Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
VSS	GND	Ground	A1, A18, E10, E12, E13, E14, E5, E6, E7, E8, F10, F12, F13, F14, F5, F6, F7, F8, G10, G11, G12, G7, G8, G9, H10, H11, H12, H13, H14, H5, H6, H7, H8, H9, J10, J11, J12, J13, J14, J5, J6, J7, J8, J9, K10, K11, K12, K7, K8, K9, L10, L11, L12, L13, L14, L5, L6, L7, L8, L9, M10, M11, M12, M13, M14, M5, M6, M7, M8, M9, N10, N11, N12, N7, N8, N9, P13, P14, P5, T2, V18	A1, A20, F15, F6, G10, G11, G12, G13, G14, G7, G8, G9, H10, H11, H12, H13, H14, H7, H8, H9, J10, J11, J12, J13, J14, J7, J8, J9, K10, K11, K12, K13, K14, K7, K8, K9, L10, L11, L12, L13, L14, L7, L8, L9, M10, M11, M12, M13, M14, M7, M8, M9, N10, N11, N12, N13, N14, N7, N8, N9, P10, P11, P12, P13, P14, P7, P8, P9, R14, R15, R6, V2, V5, W2, Y1, Y20	A1, A16, E10, E12, E6, E8, F10, F11, F5, F6, F7, F8, F9, G10, G11, G12, G6, G7, G8, G9, H10, H11, H5, H6, H7, H8, H9, J10, J11, J12, J6, J7, J8, J9, K10, K11, K5, K6, K7, K8, K9, L10, L11, L12, L6, L7, L8, L9, M5, M7, R2, R3, R4, T1, T16	A1, A19, D16, D4, E15, E5, F10, F11, F12, F13, F14, F6, F7, F8, F9, G10, G11, G12, G13, G14, G6, G7, G8, G9, H10, H11, H12, H13, H14, H6, H7, H8, H9, J10, J11, J12, J13, J14, J6, J7, J8, J9, K10, K11, K12, K13, K14, K6, K7, K8, K9, L10, L11, L12, L13, L14, L6, L7, L8, L9, M10, M11, M12, M13, M14, M6, M7, M8, M9, N10, N11, N12, N13, N14, N6, N7, N8, N9, P10, P11, P12, P13, P14, P6, P7, P8, P9, R14, R5, R8, T4, U2, V2, V3, W1, W19
VSSA	AGND	Analog Ground	P10, P12, P6, P8, R13, R5, V1, V16	R12, R9	M11, M9	R10, R12

(1) See *Recommended Operating Conditions* for more information about the core voltage for a specific device.
(2) See the *Layout Guidelines* sections for details on connecting this pin.
(3) PCB should directly route VDDS18_LDO to all of the VDDS18 pins.
(4) On AM261x, the Analog LDO is connected internally to the 1.8V analog supply and therefore functions as a regular 1.8V output.

5.3.18 PRU-ICSS

Table 5-45. PRU-ICSS ECAP Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_ECAP0_APWM_OUT	O	PRU-ICSS Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	D14	C16	A15	
PR1_ECAP0_APWM_OUT	O	PRU-ICSS Enhanced Capture (ECAP) Input or ECAP Auxiliary PWM (APWM) Output	D14	C16	A15	

Table 5-46. PRU-ICSS GPIO Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_PRU0_GPIO0	IO	PRU0 General Purpose Input/Output	K17	N17	K14	M18
PR0_PRU0_GPIO1	IO	PRU0 General Purpose Input/Output	K18	N19	H14	L19
PR0_PRU0_GPIO2	IO	PRU0 General Purpose Input/Output	J18	M18	G16	K19
PR0_PRU0_GPIO3	IO	PRU0 General Purpose Input/Output	J17	M20	J14	L17
PR0_PRU0_GPIO4	IO	PRU0 General Purpose Input/Output	K16	L20	G15	J19
PR0_PRU0_GPIO5	IO	PRU0 General Purpose Input/Output	G17	K19	F14	G17
PR0_PRU0_GPIO6	IO	PRU0 General Purpose Input/Output	K15	N20	H15	L18
PR0_PRU0_GPIO7	IO	PRU0 General Purpose Input/Output	N17	T19	M15	T18
PR0_PRU0_GPIO8	IO	PRU0 General Purpose Input/Output	G15	J18	E14	G19
PR0_PRU0_GPIO9	IO	PRU0 General Purpose Input/Output	F17	J19	E15	
PR0_PRU0_GPIO10	IO	PRU0 General Purpose Input/Output	G18	J20	E16	J18
PR0_PRU0_GPIO11	IO	PRU0 General Purpose Input/Output	M16	P20	J15	N18
PR0_PRU0_GPIO12	IO	PRU0 General Purpose Input/Output	M15	P19	J16	N19
PR0_PRU0_GPIO13	IO	PRU0 General Purpose Input/Output	H17	K20	F15	H19
PR0_PRU0_GPIO14	IO	PRU0 General Purpose Input/Output	H16	L19	G14	H18
PR0_PRU0_GPIO15	IO	PRU0 General Purpose Input/Output	L16	P18	H16	M19
PR0_PRU0_GPIO16	IO	PRU0 General Purpose Input/Output	H18	M19	F16	K18
PR0_PRU1_GPIO0	IO	PRU1 General Purpose Input/Output	F18	H20	D14	G18
PR0_PRU1_GPIO1	IO	PRU1 General Purpose Input/Output	G16	H19	D16	F18
PR0_PRU1_GPIO2	IO	PRU1 General Purpose Input/Output	E17	H17		E17
PR0_PRU1_GPIO3	IO	PRU1 General Purpose Input/Output	E18	G20		F19
PR0_PRU1_GPIO4	IO	PRU1 General Purpose Input/Output	F16	G19	D15	E19
PR0_PRU1_GPIO5	IO	PRU1 General Purpose Input/Output	F15	F20		E18
PR0_PRU1_GPIO6	IO	PRU1 General Purpose Input/Output	E16	F19	E13	D19
PR0_PRU1_GPIO7	IO	PRU1 General Purpose Input/Output	A16, G3	A19, H2	C16, E2	E1
PR0_PRU1_GPIO8	IO	PRU1 General Purpose Input/Output	D18	G18		C19
PR0_PRU1_GPIO9	IO	PRU1 General Purpose Input/Output	C18	E20		
PR0_PRU1_GPIO10	IO	PRU1 General Purpose Input/Output	D17	E19		
PR0_PRU1_GPIO11	IO	PRU1 General Purpose Input/Output	B18	F17		D18
PR0_PRU1_GPIO12	IO	PRU1 General Purpose Input/Output	B17	D20		C18
PR0_PRU1_GPIO13	IO	PRU1 General Purpose Input/Output	D16	C20		B19
PR0_PRU1_GPIO14	IO	PRU1 General Purpose Input/Output	C17	D19		C17
PR0_PRU1_GPIO15	IO	PRU1 General Purpose Input/Output	A17	E18		A18
PR0_PRU1_GPIO16	IO	PRU1 General Purpose Input/Output	C16	B20		B18
PR0_PRU1_GPIO17	IO	PRU1 General Purpose Input/Output	D13	B17	C14	
PR0_PRU1_GPIO18	IO	PRU1 General Purpose Input/Output	C15	C19		B17
PR0_PRU1_GPIO19	IO	PRU1 General Purpose Input/Output	D15	C18		B16
PR1_PRU0_GPIO0	IO	PRU0 General Purpose Input/Output	A3, C10, K17, K2	B12, B5, K1, N17	A10, G2, K14	B12, G2, M18
PR1_PRU0_GPIO1	IO	PRU0 General Purpose Input/Output	A2, B11, J4, K18	A4, C12, L4, N19	A11, H14, H3	B11, H1, L19
PR1_PRU0_GPIO2	IO	PRU0 General Purpose Input/Output	C11, C6, J18, K4	B13, B4, L1, M18	B11, G16, H2	C13, H2, K19
PR1_PRU0_GPIO3	IO	PRU0 General Purpose Input/Output	C2	B1	A3	A3
PR1_PRU0_GPIO4	IO	PRU0 General Purpose Input/Output	D2	A3	C5	A4

Table 5-46. PRU-ICSS GPIO Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR1_PRU0_GPIO5	IO	PRU0 General Purpose Input/Output	B2	B3	A4	B5
PR1_PRU0_GPIO6	IO	PRU0 General Purpose Input/Output	D3	A2	B4	A5
PR1_PRU0_GPIO7	IO	PRU0 General Purpose Input/Output	B16, B7, C1	B19, B2, D8	A2, A7, C15	A9, B4
PR1_PRU0_GPIO8	IO	PRU0 General Purpose Input/Output	B1	C3	A5	A6
PR1_PRU0_GPIO9	IO	PRU0 General Purpose Input/Output	A11, B4, F17, K3	A13, A5, J19, M2	A12, E15, G1	A12, J1
PR1_PRU0_GPIO10	IO	PRU0 General Purpose Input/Output	A16, B5	A19, B6	C16	
PR1_PRU0_GPIO11	IO	PRU0 General Purpose Input/Output	E3	C2	C4	B2
PR1_PRU0_GPIO12	IO	PRU0 General Purpose Input/Output	D1	D2	B1	B1
PR1_PRU0_GPIO13	IO	PRU0 General Purpose Input/Output	E4	D1	C1	B3
PR1_PRU0_GPIO14	IO	PRU0 General Purpose Input/Output	F2	E2	C2	C2
PR1_PRU0_GPIO15	IO	PRU0 General Purpose Input/Output	E2	C1	B2	A2
PR1_PRU0_GPIO16	IO	PRU0 General Purpose Input/Output	C1	B2	A2	B4
PR1_PRU0_GPIO17	IO	PRU0 General Purpose Input/Output	C7, D7	B9, C7	B7, C8	C9
PR1_PRU0_GPIO18	IO	PRU0 General Purpose Input/Output	C8	A9	A8	
PR1_PRU0_GPIO19	IO	PRU0 General Purpose Input/Output	A14	B16	C13	A15
PR1_PRU0_GPIO20	IO	PRU1 General Purpose Input/Output	C12	C14	C12	A14
PR1_PRU1_GPIO0	IO	PRU1 General Purpose Input/Output	V17	W16	R14	V15
PR1_PRU1_GPIO1	IO	PRU1 General Purpose Input/Output	T16	Y16	T14	W15
PR1_PRU1_GPIO2	IO	PRU1 General Purpose Input/Output	P15	W17	T15	W16
PR1_PRU1_GPIO3	IO	PRU1 General Purpose Input/Output	A10, F1	A12, G1	B10, D1	D1
PR1_PRU1_GPIO4	IO	PRU1 General Purpose Input/Output	C9, F4	D11, G2	B9, D2	D2
PR1_PRU1_GPIO5	IO	PRU1 General Purpose Input/Output	G2	E1	D3	C1
PR1_PRU1_GPIO6	IO	PRU1 General Purpose Input/Output	A9, F3	A11, F1	C10, F4	A11, E2
PR1_PRU1_GPIO7	IO	PRU1 General Purpose Input/Output	D11	D15	B13	B14
PR1_PRU1_GPIO8	IO	PRU1 General Purpose Input/Output	B9, E1	B11, F2	D8, E3	B10, E3
PR1_PRU1_GPIO9	IO	PRU1 General Purpose Input/Output	R16	Y17	R15	V16
PR1_PRU1_GPIO10	IO	PRU1 General Purpose Input/Output	D14	C16	A15	
PR1_PRU1_GPIO11	IO	PRU1 General Purpose Input/Output	N1	R2	M2	N2
PR1_PRU1_GPIO12	IO	PRU1 General Purpose Input/Output	N4	R1	N1	N1
PR1_PRU1_GPIO13	IO	PRU1 General Purpose Input/Output	D13	B17	C14	
PR1_PRU1_GPIO14	IO	PRU1 General Purpose Input/Output	A15	B18	B15	
PR1_PRU1_GPIO15	IO	PRU1 General Purpose Input/Output	D9, H2	C9, H1	C11, E1	F1
PR1_PRU1_GPIO16	IO	PRU1 General Purpose Input/Output	B10, G3	D10, H2	A9, E2	E1
PR1_PRU1_GPIO17	IO	PRU1 General Purpose Input/Output	C14	D17	B14	
PR1_PRU1_GPIO18	IO	PRU1 General Purpose Input/Output	B14	A16	D13	B15
PR1_PRU1_GPIO19	IO	PRU1 General Purpose Input/Output	C7	C7	C8	C9

Table 5-47. PRU-ICSS IEP Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_IEP0_EDC_SYNC_OUT0	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	D15	C18		B16

Table 5-47. PRU-ICSS IEP Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_IEP0_EDC_SYNC_OUT1	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	A16, F17, N17	A19, J19, T19	C16, E15, M15	T18
PR0_IEP0_EDIO_DATA_IN_OUT30	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	D13, D17, P2	B17, E19, U2	C14, P3	T1
PR0_IEP0_EDIO_DATA_IN_OUT31	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	C15, C18	C19, E20		B17
PR1_IEP0_EDC_SYNC_OUT0	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	B14, U18	A16, Y19	D13, R16	B15, W18
PR1_IEP0_EDC_SYNC_OUT1	O	PRU-ICSS Industrial Ethernet Distributed Clock Sync Output	B15, N17	A18, T19	B16, M15	A17, T18
PR1_IEP0_EDIO_DATA_IN_OUT30	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	C12, N18	C14, U20	C12, L15	A14, R18
PR1_IEP0_EDIO_DATA_IN_OUT31	IO	PRU-ICSS Industrial Ethernet Digital I/O Data Input/Output	A14, T18	B16, W19	C13, N14	A15, V18

Table 5-48. PRU-ICSS MDIO Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_MDIO0_MDC	O	PRU-ICSS MDIO Clock	L18	R20	K16	P19
PR0_MDIO0_MDIO	IO	PRU-ICSS MDIO Data	L17	R19	K15	N17
PR1_MDIO0_MDC	O	PRU-ICSS MDIO Clock	A4, C13	A17, A6	A14	A16
PR1_MDIO0_MDIO	IO	PRU-ICSS MDIO Data	B15, B6	A18, B7	B16	A17

Table 5-49. PRU-ICSS UART Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PR0_UART0_CTSn	I	PRU-ICSS UART Clear to Send (Active Low)	F17	J19	E15	
PR0_UART0_RTSn	O	PRU-ICSS UART Request to Send (Active Low)	G18	J20	E16	J18
PR0_UART0_RXD	I	PRU-ICSS UART Receive Data	C18	E20		
PR0_UART0_TXD	O	PRU-ICSS UART Transmit Data	D17	E19		
PR1_UART0_CTSn	I	PRU-ICSS UART Clear to Send (Active Low)	B16	B19	C15	
PR1_UART0_RTSn	O	PRU-ICSS UART Request to Send (Active Low)	D14	C16	A15	
PR1_UART0_RXD	I	PRU-ICSS UART Receive Data	A16	A19	C16	
PR1_UART0_TXD	O	PRU-ICSS UART Transmit Data	D13	B17	C14	

5.3.19 SDFM

Table 5-50. SDFM0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SDFM0_CLK0	I	SDFM Channel 0 Clock	B16	B19	C15	
SDFM0_CLK1	I	SDFM Channel 1 Clock	A16	A19	C16	
SDFM0_CLK2	I	SDFM Channel 2 Clock	B15	A18	B16	A17

Table 5-50. SDFM0 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SDFM0_CLK3	I	SDFM Channel 3 Clock	A15	B18	B15	
SDFM0_D0	I	SDFM Channel 0 Data	D14	C16	A15	
SDFM0_D1	I	SDFM Channel 1 Data	D13	B17	C14	
SDFM0_D2	I	SDFM Channel 2 Data	C13	A17	A14	A16
SDFM0_D3	I	SDFM Channel 3 Data	C14	D17	B14	

Table 5-51. SDFM1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SDFM1_CLK0	I	SDFM Channel 0 Clock	B14, B6	A16, B7	D13	B15
SDFM1_CLK1	I	SDFM Channel 1 Clock	B5, C12	B6, C14	C12	A14
SDFM1_CLK2 (2)	I	SDFM Channel 2 Clock	A3, B13	B15, B5	B12	B13
SDFM1_CLK3 (1)	I	SDFM Channel 3 Clock	A13, C6	A15, B4	A13	A13
SDFM1_D0	I	SDFM Channel 0 Data	A14, A16, A4	A19, A6, B16	C13, C16	A15
SDFM1_D1	I	SDFM Channel 1 Data	B15, B4, D11	A18, A5, D15	B13, B16	A17, B14
SDFM1_D2	I	SDFM Channel 2 Data	A15, A2, B12	A4, B14, B18	B15	
SDFM1_D3	I	SDFM Channel 3 Data	A12, A5	A14, A7		

(1) SDFM1_CLK3 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.
(2) SDFM1_CLK2 is implemented with the I2C OD FS (Open Drain Fail Safe) voltage buffer.

5.3.20 SPI

Table 5-52. SPI0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI0_CLK	IO	SPI0 Clock	A11, R3	A13, T2	A12, M3	A12, R2
SPI0_CS0	IO	SPI0 Chip Select 0	C11, P1	B13, U4	B11, N3	C13, R1
SPI0_CS1	IO	SPI0 Chip Select 1	B12, B7	B14, D8	A7	A9
SPI0_D0	IO	SPI0 Data 0	C10, M4	B12, T1	A10, L3	B12, P2
SPI0_D1	IO	SPI0 Data 1	B11, P3	C12, U1	A11, N2	B11, P1

Table 5-53. SPI1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI1_CLK	IO	SPI1 Clock	A10	A12	B10	
SPI1_CS0	IO	SPI1 Chip Select 0	C9	D11	B9	
SPI1_D0	IO	SPI1 Data 0	B10	D10	A9	
SPI1_D1	IO	SPI1 Data 1	D9	C9	C11	

Table 5-54. SPI2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI2_CLK	IO	SPI2 Clock	B9, C14, G1	B11, D17, K4	B14, D8, F2	B10, F2
SPI2_CS0	IO	SPI2 Chip Select 0	A14, A9, M2	A11, B16, M1	C10, C13, H1	A11, A15, J3

Table 5-54. SPI2 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI2_CS1	IO	SPI2 Chip Select 1	B15	A18	B16	A17
SPI2_D0	IO	SPI2 Data 0	B14, B8	A16, B10	B8, D13	A10, B15
SPI2_D1	IO	SPI2 Data 1	A15, A8	A10, B18	B15, C9	B9

Table 5-55. SPI3 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SPI3_CLK	IO	SPI3 Clock	C8	A9	A8	
SPI3_CS0	IO	SPI3 Chip Select 0	D7	B9	B7	
SPI3_CS1	IO	SPI3 Chip Select 1	C13	A17	A14	A16
SPI3_D0	IO	SPI3 Data 0	C7	C7	C8	C9
SPI3_D1	IO	SPI3 Data 1	B7	D8	A7	A9

5.3.21 System and Miscellaneous

5.3.21.1 Boot Mode Configuration

Table 5-56. Boot Mode Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
SOP0		Boot Mode configuration bit 0 (GPIO3)	N1	R2	M2	N2
SOP1		Boot Mode configuration bit 1 (GPIO4)	N4	R1	N1	N1
SOP2		Boot Mode configuration bit 2 (GPIO12)	A11	A13	A12	A12
SOP3		Boot Mode configuration bit 3 (GPIO13)	C10	B12	A10	B12

5.3.21.2 Clocking

Table 5-57. XTAL Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
XTAL_XI (1)	I	External Crystal (XTAL) Input	T1	Y3	T3	W3
XTAL_XO (1)	O	External Crystal (XTAL) Output	R1	Y2	T2	W2

(1) The XTAL interface requires a 25 MHz clock source.

Table 5-58. Output Clock Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
CLKOUT0	O	Output Clock 0	E1, M2	F2, M1	E3, H1	E3, J3
CLKOUT1	O	Output Clock 1	B16	B19	C15	

Table 5-59. External Reference Clock Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
EXT_REFCLK0	I	External Reference Clock Input	P2	U2	P3	T1

5.3.21.3 Emulation and Debug

Table 5-60. Trace Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
TRC_CLK	O	Trace Clock	D15, K16	C18, L20	G15	B16, J19
TRC_CTL	O	Trace Control	C15, G17	C19, K19	F14	B17, G17
TRC_DATA0	O	Trace Data 0	F15, K17	F20, N17	K14	E18, M18
TRC_DATA1	O	Trace Data 1	C18, K18	E20, N19	H14	L19
TRC_DATA2	O	Trace Data 2	D17, J18	E19, M18	G16	K19
TRC_DATA3	O	Trace Data 3	D18, J17	G18, M20	J14	C19, L17
TRC_DATA4	O	Trace Data 4	E16	F19	E13	D19
TRC_DATA5	O	Trace Data 5	F16	G19	D15	E19
TRC_DATA6	O	Trace Data 6	F18	H20	D14	G18
TRC_DATA7	O	Trace Data 7	G16	H19	D16	F18
TRC_DATA8	O	Trace Data 8	E17	H17		E17
TRC_DATA9	O	Trace Data 9	E18	G20		F19
TRC_DATA10	O	Trace Data 10	C16	B20		B18
TRC_DATA11	O	Trace Data 11	A17	E18		A18
TRC_DATA12	O	Trace Data 12	B18	F17		D18
TRC_DATA13	O	Trace Data 13	B17	D20		C18
TRC_DATA14	O	Trace Data 14	D16	C20		B19
TRC_DATA15	O	Trace Data 15	C17	D19		C17

Table 5-61. JTAG Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
TCK	I	JTAG Test Clock Input	B3	D4	C6	B6
TDI	I	JTAG Test Data Input	C5	C5	D5	C7
TDO	O	JTAG Test Data Output	C4	E5	B5	A7
TMS	IO	JTAG Test Mode Select Input	D5	D6	C7	B7

5.3.21.4 SYSTEM

Table 5-62. System Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
PORz	I	Device Power-On (PORz) cold reset	R2	V3	P2	T2
SAFETY_ERRORn	IO	ESM Safety Error Signal	D4, M2, P2	E3, M1, U2	B3, H1, P3	C5, J3, T1
WARMRSTn	IO	Warm Reset Request (Input) / Warm Reset Status (Output)	C3	G3	C3	C3

5.3.21.5 VMON

Table 5-63. VMON Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
VSYS_MON (1)	-	External Voltage Monitor with 0.9 V (+/-3%) setpoint.	U2	Y4	R5	V5

(1) See the *Electrical Specifications - Safety Comparators* section for additional details on this pin.

5.3.21.6 Reserved

Table 5-64. Reserved Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ATESTV1	-	Reserved. This pin must be left unconnected.	T6	W5	T4	W5
TEMPCAL	-	Reserved. This pin must be connected to ground (VSS).	U1	W3	P5	W4

Table 5-65. No Connection Description

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
NC (1)	NC	No Connection	J15, R7, R9, T15, T7, U4, U5, U6, U7, U8, U9, V3, V4, V5, V6, V7, V8	U17		

(1) These pins should be left unconnected.

5.3.22 UART

Table 5-66. UART0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART0_CTSn	I	UART Clear to Send (active low)	A5, B7	A7, D8	A7	A9
UART0_RTSn	O	UART Request to Send (active low)	C6, C7	B4, C7	C8	C9
UART0_RXD	I	UART Receive Data	A7, B6	A8, B7	A6	A8
UART0_TXD	O	UART Transmit Data	A4, A6	A6, B8	B6	B8

Table 5-67. UART1 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART1_CTSn	I	UART Clear to Send (active low)	B15, G4	A18, J2	B16	A17
UART1_DCDn	I	UART Data Carrier Detect (Active Low)	J4, N1	L4, R2	H3, M2	H1, N2
UART1_DSRn	I	UART Data Set Ready (Active Low)	V17	W16	R14	V15
UART1_DTRn	O	UART Data Terminal Ready (Active Low)	K1, K3	M2, N1	G1, J2	J1, K1
UART1_RIn	I	UART Ring Indicator	K4, N4	L1, R1	H2, N1	H2, N1
UART1_RTSn	O	UART Request to Send (active low)	B12, J2	B14, L2	F3	G1

Table 5-67. UART1 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART1_RXD	I	UART Receive Data	A9, L3, M2, U18	A11, M1, T3, Y19	C10, H1, M1, R16	A11, J3, L2, W18
UART1_TXD	O	UART Transmit Data	B9, G1, L2, M3, T18	B11, K4, N2, R4, W19	D8, F2, K2, L1, N14	B10, F2, J2, M1, V18

Table 5-68. UART2 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART2_CTSn	I	UART Clear to Send (active low)	C13, D14, H1	A17, C16, J3	A14, A15	A16
UART2_RTSn	O	UART Request to Send (active low)	A12, B16, F3, J3, R3	A14, B19, F1, J1, T2	C15, F4, M3	E2, R2
UART2_RXD	I	UART Receive Data	B5, B8, D13, J1	B10, B17, B6, K2	B8, C14, G3	A10
UART2_TXD	O	UART Transmit Data	A16, A3, A8, G4	A10, A19, B5, J2	C16, C9	B9

Table 5-69. UART3 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART3_CTSn	I	UART Clear to Send (active low)	C10, G18, K1, K2, K3, N2	B12, J20, K1, M2, M3, N1	A10, E16, G1, G2, J2, L2	B12, G2, J1, J18, K1, M2
UART3_RTSn	O	UART Request to Send (active low)	A2, B11, G17, J1	A4, C12, K19, K2	A11, F14, G3	B11, G17
UART3_RXD	I	UART Receive Data	B12, C11, C7, D15, K16, P1	B13, B14, C18, C7, L20, U4	B11, C8, G15, N3	B16, C13, C9, J19, R1
UART3_TXD	O	UART Transmit Data	A11, A12, B7, C15, J17, R3	A13, A14, C19, D8, M20, T2	A12, A7, J14, M3	A12, A9, B17, L17, R2

Table 5-70. UART4 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART4_CTSn	I	UART Clear to Send (active low)	A14, T16	B16, Y16	C13, T14	A15, W15
UART4_RTSn	O	UART Request to Send (active low)	B14, V17	A16, W16	D13, R14	B15, V15
UART4_RXD	I	UART Receive Data	A10, D11, H1, H2, N18	A12, D15, H1, J3, U20	B10, B13, E1, L15	B14, F1, R18
UART4_TXD	O	UART Transmit Data	C12, C9, G3, J3, N17	C14, D11, H2, J1, T19	B9, C12, E2, M15	A14, E1, T18

Table 5-71. UART5 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART5_CTSn	I	UART Clear to Send (active low)	B15, D13	A18, B17	B16, C14	A17
UART5_RTSn	O	UART Request to Send (active low)	A16	A19	C16	
UART5_RXD	I	UART Receive Data	A15, C13, D9, R16, V2	A17, B18, C9, V1, Y17	A14, B15, C11, R1, R15	A16, V1, V16

Table 5-71. UART5 Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
UART5_TXD	O	UART Transmit Data	B10, B15, C14, P15, U3	A18, D10, D17, W1, W17	A9, B14, B16, P1, T15	A17, U1, W16

5.3.23 USB0

Table 5-72. USB0 Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
USB0_DM	IO	USB 2.0 Differential Data (negative)	U3	W1	P1	U1
USB0_DP	IO	USB 2.0 Differential Data (positive)	V2	V1	R1	V1
USB0_DRVVBUS	O	USB VBUS control output (active high)	B8, M2, P2	B10, M1, U2	B8, H1, P3	A10, J3, T1

5.3.24 XBAR

Table 5-73. Output XBAR Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
XBAROUT0	O	OUTPUTXBAR Signal 0	C11, R3	B13, T2	B11, M3	C13, R2
XBAROUT1	O	OUTPUTXBAR Signal 1	A11, C9	A13, D11	A12, B9	A12
XBAROUT2	O	OUTPUTXBAR Signal 2	A10, C10	A12, B12	A10, B10	B12
XBAROUT3	O	OUTPUTXBAR Signal 3	B10, B11	C12, D10	A11, A9	B11
XBAROUT4	O	OUTPUTXBAR Signal 4	A7, D9	A8, C9	A6, C11	A8
XBAROUT5	O	OUTPUTXBAR Signal 5	A6, A9	A11, B8	B6, C10	A11, B8
XBAROUT6	O	OUTPUTXBAR Signal 6	B9, G17	B11, K19	D8, F14	B10, G17
XBAROUT7	O	OUTPUTXBAR Signal 7	D7, K16	B9, L20	B7, G15	J19
XBAROUT8	O	OUTPUTXBAR Signal 8	C8, K17	A9, N17	A8, K14	M18
XBAROUT9	O	OUTPUTXBAR Signal 9	C7	C7	C8	C9
XBAROUT10	O	OUTPUTXBAR Signal 10	B7	D8	A7	A9
XBAROUT11	O	OUTPUTXBAR Signal 11	D16, K18	C20, N19	H14	B19, L19
XBAROUT12	O	OUTPUTXBAR Signal 12	C17, J18	D19, M18	G16	C17, K19
XBAROUT13	O	OUTPUTXBAR Signal 13	D15, J17	C18, M20	J14	B16, L17
XBAROUT14	O	OUTPUTXBAR Signal 14	C15, L17	C19, R19	K15	B17, N17
XBAROUT15	O	OUTPUTXBAR Signal 15	L18, P2	R20, U2	K16, P3	P19, T1

Table 5-74. External ADC Channel Select XBAR Signal Descriptions

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_EXTCH_XBAROUT0	O	External ADC Channel Select XBAR Signal 0	C11, C13	A17, B13	A14, B11	A16, C13
ADC_EXTCH_XBAROUT1	O	External ADC Channel Select XBAR Signal 1	A11, C14	A13, D17	A12, B14	A12
ADC_EXTCH_XBAROUT2	O	External ADC Channel Select XBAR Signal 2	C10, C12	B12, C14	A10, C12	A14, B12
ADC_EXTCH_XBAROUT3	O	External ADC Channel Select XBAR Signal 3	B11, D11	C12, D15	A11, B13	B11, B14

Table 5-74. External ADC Channel Select XBAR Signal Descriptions (continued)

Signal Name [1]	Pin Type [2]	Description [3]	ZCZ PIN [4]	ZFG PIN [4]	ZEJ PIN [4]	ZNC PIN [4]
ADC_EXTCH_XBAROUT4	O	External ADC Channel Select XBAR Signal 4	C9, G17, P15	D11, K19, W17	B9, F14, T15	G17, W16
ADC_EXTCH_XBAROUT5	O	External ADC Channel Select XBAR Signal 5	A10, K16, R16	A12, L20, Y17	B10, G15, R15	J19, V16
ADC_EXTCH_XBAROUT6	O	External ADC Channel Select XBAR Signal 6	B10, F15, K17	D10, F20, N17	A9, K14	E18, M18
ADC_EXTCH_XBAROUT7	O	External ADC Channel Select XBAR Signal 7	C18, D9, K18	C9, E20, N19	C11, H14	L19
ADC_EXTCH_XBAROUT8	O	External ADC Channel Select XBAR Signal 8	B15, J18	A18, M18	B16, G16	A17, K19
ADC_EXTCH_XBAROUT9	O	External ADC Channel Select XBAR Signal 9	A15, J17	B18, M20	B15, J14	L17

5.4 Pin Connectivity Requirements

This section describes connectivity requirements for package balls that have specific connectivity requirements as well as any unused balls.

Pin Connectivity Requirements

ZCZ Ball Number	ZFG Ball Number	ZEJ Ball Number	ZNC Ball Number	Ball Name	Pin Connectivity Requirements
D4	E3	B3	C5	SAFETY_ERRORn	This pin must be connected to ground (VSS) through a separate external pull resistor to ensure it is held to a valid logic low level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull–down may be used to hold a valid logic low level if no PCB signal trace is connected to the ball.
B3 C5 D5	D4 C5 D6	C6 D5 C7	B6 C7 B7	TCK TDI TMS	Each of these pins must be connected to the corresponding power supply through separate external pull resistors to ensure these balls are held to a valid logic high level if a PCB signal trace is connected and not actively driven by an attached device. The internal pull–up may be used to hold a valid logic high level if no PCB signal trace is connected to the ball.
A13 B13	A15 B15	A13 B12	A13 B13	GPIO135 (I2C0_SCL) GPIO134 (I2C0_SDA)	Each of these pins must be connected to the corresponding power supply through separate external pull resistors to ensure these balls are held to a valid logic high level.
N1 N4 A11 C10	R2 R1 A13 B12	M2 N1 A12 A10	N2 N1 A12 B12	GPIO3 (SOP0) GPIO4 (SOP1) GPIO12 (SOP2) GPIO13 (SOP3)	Each of these pins must be connected to the corresponding power supply or ground (VSS) through separate external pull resistors to ensure these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.
U16	V16	R13	U15	ADC_CAL0	If all ADCx_AINy inputs for all ADC instances (ADC[0:2]_AIN[0:6]) are not used, the ADC_CAL0 analog pin must be connected (shorted) directly to ground (VSS).
U2	Y4	R5	V5	VSYS_MON	If VSYS_MON is not used, this pin may be connected (shorted) directly to ground (VSS).
T4	V7	N8	T8	VDD_TEMP	If the internal temp diode is being used this pin must be connected to the 1.2V/1.25V power rail. If the internal temp diode is not being used this pin can be connected (shorted) directly to ground (VSS).
T6	W5	T4	W5	ATESTV1	This pin is reserved and must be left unconnected.
U1	W3	P5	W4	TEMPCAL	This pin is reserved and must be connected to ground (VSS).
NC ZCZ PIN	NC ZFG PIN	-	-	NC	Any pin labeled NC should be left unconnected.
ADC ZCZ PIN	ADC ZFG PIN	ADC ZEJ PIN	ADC ZNC PIN	ADC[0:2]_AIN[0:6]	Any unused ADCx_AINy input pin for any ADC instance (ADC[0:2]_AIN[0:6]) must be connected (shorted) directly to ground (VSS).
LVCMOS ZCZ PIN	LVCMOS ZFG PIN	LVCMOS ZEJ PIN	LVCMOS ZNC PIN	Any LVCMOS Voltage Buffer Pin	If an associated IOMUX pad configuration register exists for a given pin, it may remain unconnected. After PORz, the LVCMOS voltage buffer is configured to a default state compatible with an unconnected ball.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1) (2)

PARAMETER		MIN	MAX	UNIT
VDD	SOC VDD core supply	–0.5	1.5	V
VDDAR1	SRAM Array Supply 1	–0.5	1.5	V
VDDAR2	SRAM Array Supply 2	–0.5	1.5	V
VDDAR3	SRAM Array Supply 3	–0.5	1.5	V
VDDS18	1.8V IO Bias Supply from Bias LDO routed through Board	–0.5	2.1	V
VDDS33	3.3V IO Supply	–0.5	4.0	V
VDDA18_OSC_PLL	1.8V Analog Supply for PLL. Routed from the 1.8V Analog LDO out through Board	–0.5	2.1	V
VDDA33	Analog 3.3V Supply	–0.5	4.0	V
VDDA18	1.8V Analog Supply. Routed from the 1.8V Analog LDO out through Board	–0.5	2.1	V
IO Pin Steady State Voltage	3.3V LVCMOS IO Buffer	–0.3	VDDS33(3) + 0.3	V
	3.3V I2C Open-Drain IO Buffers	–0.3	VDDS33(3) + 0.3	V
	XTAL Pad	–0.5	2.1	V
Transient Overshoot and Undershoot	All Other IO Terminals	–0.3	VDDS33(3) + 0.2 × VDDS33(3) for up to 20% of signal period	V
	XTAL Pad 20% of VDDA18_OSC_PLL for up to 20% of signal period		0.2 × VDDA18_OSC_PLL	V
Latch Up Performance Class II (150°C)	Latch-up I-test Performance (Current-Pulse Injection on each IO pin)		±100	mA
	Latch-up Overvoltage Performance (Voltage Injection on each IO pin)		1.5 × VDDS33	V
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Storage temperature(4)	T_{stg}	–55	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) VDDS33 is the voltage on the corresponding power-supply pin(s) for the IC.
(4) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.

6.2 Electrostatic Discharge (ESD) Extended Automotive Ratings

over recommended operating conditions (unless otherwise noted)

				VALUE	UNIT
324-ball ZCZ-Q1 Package					
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human body model (HBM), per AEC-Q100-002[1]		±2000	V
		Charged device model (CDM), per AEC-Q100-011	All pins	±500	
			Corner balls on 324-ball ZCZ: A1, A18, V1, V18	±750	
256-ball ZEJ-Q1 Package					
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human body model (HBM), per AEC-Q100-002[1]	Human body model (HBM), per AEC-Q100-002[1]	±2000	V
		Charged device model (CDM), per AEC-Q100-011	All pins	±500	
			Corner balls on 256-ball ZCZ: A1, A16, T1, T16	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Electrostatic Discharge (ESD) Industrial Ratings

over recommended operating conditions (unless otherwise noted)

			VALUE	UNIT
324-ball ZCZ Package				
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	
304-ball ZFG package				
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	
256-Ball ZEJ package				
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	
293-ball ZNC package				
$V_{(ESD)}$	Electrostatic Discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.4 Power-On Hours (POH) Summary

over recommended operating conditions (unless otherwise noted)[1] [2] [3]

Parameter		EXTENDED INDUSTRIAL	EXTENDED AUTOMOTIVE
Operating Junction Temperature (T_j)		–40°C to 125°C	–40°C to 150°C
POH @ Temp Profile	R5F = 400MHz[5] [6]	100K @ 105°C (100% @ 105°C) 25K @ 125°C (100% @ 125°C)	20K @ Automotive Temp Profile[4]
	R5F = 500MHz (Default)	55K @ 105°C (100% @ 105°C) 15K @ 125°C (100% @ 125°C)	20K @ Automotive Temp Profile[4]

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures.
(3) POH is a function of voltage, temperature, and time. Usage at higher voltages and temperatures will result in a reduction in POH.
(4) See *Automotive Temperature Profile* section
(5) For AM261x devices, lowering the R5F core frequency allows for better POH.
(6) Devices of the 'O' Speed grade must follow the Recommended Operating Conditions for R5F at 500MHz regardless of the core frequency settings

6.4.1 Automotive Temperature Profile

T_J (°C)	HOURS	DAYS	YEARS	PERCENT OF TIME
–40	1200	~50	~0.14	6%
75	4000	~167	~0.46	20%
95	13000	~541	~1.48	65%
130	1600	~67	~0.18	8%
150	200	~8.5	~0.023	1%
Total	20000	~833	~2.28	100%

6.5 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION		MIN	NOM	MAX	UNIT
VDD[1]	SOC VDD Core Supply	R5F = 400MHz	1.140	1.2	1.26	V
		R5F = 500MHz	1.188	1.25	1.32	V
VDDAR1, VDDAR2, VDDAR3[1]	SRAM Array Supplies	R5F = 400MHz	1.140	1.2	1.26	V
		R5F = 500MHz	1.188	1.25	1.32	V
VDDS18	1.8V IO Bias Supply from Bias LDO routed through board		1.710	1.800	1.890	V
VDDS33	3.3V IO Supply		3.135	3.300	3.465	V
VDDA18_OSC_PLL	1.8V Analog supply for PLL. Routed from the Analog LDO out through board		1.710	1.800	1.890	V
VDDA33	Analog 3.3V Supply		3.135	3.300	3.465	V
VDDA18	1.8V Analog supply. Routed from 1.8V Analog LDO out through Board		1.710	1.800	1.890	V
Tj	Operating junction temperature range	Extended Automotive	-40		150	°C
T_J	Operating junction temperature range	Extended Industrial	–40		125	°C

(1) Devices of the 'O' Speed grade must follow the Recommended Operating Conditions for R5F at 500MHz regardless of the core frequency settings

6.6 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks, device core clocks, and available memory.

DEVICE	GRADE	RAM (MB)	R5FSS (MHz)	HSM (MHz)	ICSS (MHz)	INFRA[1] (MHz)
AM261x	L	1.5	400	200	200	200
AM261x	O[2]	1.5	500	250	225	200
AM261x	P	1.5	200	200	200	200

(1) Infrastructure includes all other modules and IP integrated in the device (such as CBASS/Interconnect and other SoC level peripherals) unless otherwise noted in the table.
(2) Devices of the 'O' Speed grade must follow the Recommended Operating Conditions for R5F at 500MHz regardless of the core frequency settings

6.7 Power Consumption Summary

Section 6.7.1, *Power Consumption - Maximum* shows the maximum current consumed by each rail and should be used for power supply selection.

6.7.1 Power Consumption - Maximum for R5F at 400MHz

with R5F at 400MHz, T_J at 150°C

SUPPLY NAME	PARAMETER		MIN	MAX(1)	UNIT
VDD + VDDARn	Maximum Current Rating for Core Domain and SRAM power			1.75	A
VDDS33	Maximum Current Rating for 3.3V IO supply	3.3V IOs Only(2)		200	mA
		1.8V IOs and 3.3V IOs(3)		120	mA
VDDS18	Maximum Current Rating for 1.8V IO supply	3.3V IOs Only(2)		0	mA
		1.8V IOs and 3.3V IOs(3)		80	mA
VDDA33	Maximum Current Rating for 3.3V Analog supply			100	mA

(1) The maximum values show the maximum possible current needed for each power rail, and are only intended for power supply selection. For power consumption in typical applications, see *Power Consumption - Typical*.
(2) This is when all IOs are operating in the 3.3V domain.
(3) This is when OSPI0 and OSPI1 IOs are operating in the 1.8V domain.

6.7.2 Power Consumption - Maximum for R5F at 500MHz

with R5F at 500MHz, T_J at 125°C

SUPPLY NAME	PARAMETER		MIN	MAX(1)	UNIT
VDD + VDDARn	Maximum Current Rating for Core Domain and SRAM power			1.5	A
VDDS33	Maximum Current Rating for 3.3V IO supply	3.3V IOs Only(2)		200	mA
		1.8V IOs and 3.3V IOs(3)		120	mA
VDDS18	Maximum Current Rating for 1.8V IO supply	3.3V IOs Only(2)		0	mA
		1.8V IOs and 3.3V IOs(3)		80	mA
VDDA33	Maximum Current Rating for 3.3V Analog supply			100	mA

(1) The maximum values show the maximum possible current needed for each power rail, and are only intended for power supply selection. For power consumption in typical applications, see *Power Consumption - Typical*.
(2) This is when all IOs are operating in the 3.3V domain.
(3) This is when OSPI0 and OSPI1 IOs are operating in the 1.8V domain.

6.8 Electrical Characteristics

Note

The interfaces or signals described in *Digital and Analog IO Electrical Characteristics* correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

AM261x has 1.8V or 3.3V compatible IOs based on supply connected to VDDS1833_FLASH0 and VDDS1833_FLASH1. Electrical characteristics of 1.8V IOs will be updated in future revisions of this data sheet.

6.8.1 Digital and Analog IO Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
PORz IO					
V_{IH}	High-Level Input Voltage	1.35			V
V_{IL}	Low-Level Input Voltage			0.5	V
V_{HYS}	Hysteresis Voltage at an Input	0.070			V
I_L	Input Leakage Current	–2		2	µA
Warm Reset IO					
V_{IH}	High-Level Input Voltage	2.15			V
V_{IL}	Low-Level Input Voltage			0.55	V
V_{HYS}	Hysteresis Voltage at an Input	0.347			V
V_{OL}	Low Level Output Voltage, Driver Enabled: I_{OL} = 6mA			0.45	V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–57			µA
TCK IO					
V_{IH}	High-Level Input Voltage	2.15			V
V_{IL}	Low-Level Input Voltage			0.55	V
V_{HYS}	Hysteresis Voltage at an Input	0.4			V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–3.9	8.9	17.2	µA
	Input Leakage Current, Receiver Disabled, Pullup Enabled		106.9	128.2	µA
	Input Leakage Current, Receiver Disabled, Pulldown Enabled		100.3	130.3	µA
I2C OD IOs					
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.55	V
V_{HYS}	Hysteresis Voltage at an Input	0.165			V
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–18		18	µA
V_{OL}	Low Level Output Voltage, Driver Enabled: I_{OL} = 3mA			0.45	V
All Other LVCMOS					
V_{IH}	High-Level Input Voltage	2			V
V_{IL}	Low-Level Input Voltage			0.55	V
V_{HYS}	Hysteresis Voltage at an Input	0.265			V
V_{OL}	Low Level Output Voltage, Driver Enabled: I_{OL} = 6mA			0.45	V
V_{OH}	High Level Output Voltage, Driver Enabled: I_{OH} = 6mA	VDDS33[(1)] – 0.45			V

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
I_L	Input Leakage Current, Receiver Disabled, Pull Disabled	–18		18	µA
	Input Leakage Current, Receiver Disabled, Pullup Enabled	–243	–100	–19	µA
	Input Leakage Current, Receiver Disabled, Pulldown Enabled	51	100	210	µA

(1) VDDS33 is the voltage on the corresponding power-supply pin on the IC.

6.8.2 Analog to Digital Converter Characteristics

This section describes the Analog to Digital Converter electrical characteristics required to ensure proper device operation.

6.8.2.1 Analog-to-Digital Converter (ADC)

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REFHI}		1.71	1.8	1.89	V
Input Conversion Range (Vin+, Vin-)	Must be < VDDA33	0		33/18 × V_{REFHI}	V
Power-up time				500	µs
Gain error		–5	±3	5	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Same reference group		±4		LSBs
ADC-to-ADC offset error	Same reference group		±2		LSBs
DNL	Controlled environment to minimize input noise	–1	±0.5	1	LSBs
INL	Controlled environment to minimize input noise	–2	±1.0	2	LSBs
SNR	Controlled environment to minimize input noise		68		dB
ENOB (Synchronous Operation)			11		bits
ENOB (Asynchronous Operation)			9.7		bits
ADC-to-ADC isolation	Synchronous operation	–10		10	LSBs
V_{REFHI} input current			500		µA
Conversion time				330	ns
Sampling Duration		75			ns
Parasitic Input Capacitance (C_p)(1)			7		pF
Sample/Hold Resistance (R_{on})(1)				1.2	kΩ
Sample/Hold Capacitance (C_h)(1)				8	pF
Input Leakage		–1.2	0.1	1.2	µA
Power supply (VDDA33)		3.13	3.3	3.46	V
Power supply (VDDA18)		1.71	1.8	1.89	V
Power Consumption (VDDA33)			200		µA
Power Consumption (VDDA18)			500		µA
Maximum input clock frequency	With minimum pulse width of 7.5ns at a 50% duty cycle		50	66.667	MHz

(1) See *ADC Input Model*

6.8.2.2 ADC Input Model

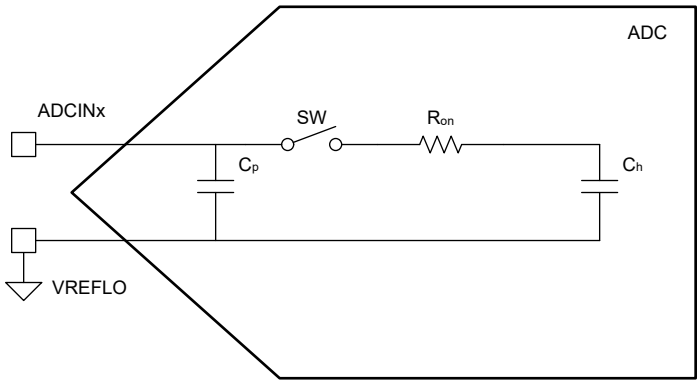


Figure 6-1. ADC Input Model

6.8.3 Comparator Subsystem A (CMPSSA)

SUBGROUP	PARAMETER	MIN	TYP	MAX	UNIT
Comparator	Power-up time			10	µs
	Comparator input range	0.1		VDDA33(1) – 50mV	V
	Input referred offset error	–20		20	mV
	Hysteresis (H1)		NA		LSB
	Hysteresis (H2)		15		LSB
	Hysteresis (H3)		35		LSB
	Hysteresis (H4)		55		LSB
	Propagation delay		21	50	ns
DAC	DAC_VREF reference voltage	1.71	1.8	1.89	V
	DAC output range	0.1		Minimum of 33/18 × DAC_VREF or VDDA33(1) – 50mV	V
	Static offset error	–45		45	mV
	Static gain error	–2		2	% of FSR
	Static DNL	>–1		4	LSB
	Static INL	–16		16	LSB
	Settling time			1	µs
	Resolution		12		bits
	DAC output disturbance (comparator trip kickback)	–100		100	LSB
	DAC output disturbance (comparator trip kickback)		200		ns
	DAC_VREF loading		37		kΩ
Common	Input Leakage	–1.2	0.1	1.2	µA
	Power supply (VDDA33)	3.13	3.3	3.46	V
	Power supply (VDDA18)	1.71	1.8	1.89	V
	Power consumption (VDDA33)		900		µA
	Power consumption (VDDA18)		120		µA
	Failsafe Input current injection			10	mA

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

6.8.4 Digital-to-Analog Converter (DAC)

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-up time				1	µs
DAC_VREF		1.71	1.8	1.89	V
Voltage output range		0.3		VDDA33(1) – 0.3	V
Trimmed offset error	Offset is checked at Midpoint (code 2048)	–10		10	mV
Gain error	DAC_VREF = 1.8V	–2.5		2.5	% of FSR
DNL	Endpoint corrected	–1		1	LSB
INL	Endpoint corrected	–20		20	LSB
Settling time	Settling to 2 LSBs (~1.6mV) after 0.3V-to-3V transition		2		µs
Resolution			12		bits
Capacitive load	Output drive capability			100	pF
Resistive load	Output drive capability	5			kΩ
DAC_VREF loading	DAC_VREF		64		kΩ
Output noise (100Hz-100KHz)	Integrated noise from 100Hz to 100kHz		1		mVrms
SNR @ 1KHz	2MHz DACVALA update rate, 200kHz output filter		60		dB
Power supply (VDDA33)		3.13	3.3	3.46	V
Power supply (VDDA18)		1.71	1.8	1.89	V
Power Consumption (VDDA33)			850		µA
Power Consumption (VDDA18)			35		µA

(1) VDDA33 is the voltage on the corresponding power-supply pin(s) on the IC.

6.8.5 Power Management Unit (PMU)

over operating junction temperature range (unless otherwise noted)

GROUP	PARAMETER	MIN	TYP	MAX	UNIT
PMU	Power supply (VDDA33)	3.1	3.3	3.46	V
Bandgap	V_{REF} trimmed	0.886	0.9	0.914	V
1.8V LDO	DC accuracy	1.764	1.8	1.836	V
	Transient load regulation	1.71	1.8	1.89	V
	DC Load regulation			5	mV
	Load current	0		100	mA
	Power up time			800	uS
	Inrush current			300	mA
	External decoupling capacitance	–20%	4.7	20%	uF
ADC Reference	Load Regulation		±1		mV
	DC accuracy	1.764	1.8	1.836	V
	Power up time			800	uS
	Inrush current			80	mA
	External decoupling capacitance	–20%	4.7	20%	uF

6.8.6 Safety Comparators

PARAMETER			MIN	TYP	MAX	UNIT
C0	C0: 1.8V Monitor Threshold		1.40	1.5	1.6	V
C1	BGAP Monitor	Lower Threshold	0.75	0.8	0.85	V
		Upper Threshold	0.935	1	1.065	V
C2	Monitors 1.8V Supply vs BGAP	Lower Threshold	1.608	1.65	1.691	V
		Upper Threshold	1.907	1.956	2.001	V
C3	Monitors 1.2V/1.25V vs BGAP	Lower Threshold	0.98	1.011	1.041	V
		Upper Threshold	1.407	1.451	1.494	V
C4	Vref Monitor (ROK0)	Lower Threshold	1.56	1.61	1.66	V
		Upper Threshold	2.09	2.16	2.22	V
C5	Monitors IO Bias Supply vs BGAP	Lower Threshold	1.58	1.621	1.661	V
		Upper Threshold	1.928	1.978	2.027	V
C6	Vref Monitor (ROK0B)	Lower Threshold	1.56	1.61	1.66	V
		Upper Threshold	2.09	2.16	2.22	V
C7	System Supply Monitor (VSYS_MON)	Lower Threshold	0.873	0.9	0.927	V
C8	UnderVoltage Threshold		2.606	2.773	2.94	V

6.9 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses.

6.9.1 VPP Specifications

over recommended operating conditions (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	NOM	MAX	UNIT
VDD	Supply voltage range for the core domain during OTP operation(1)	Normal Operation, R5F = 400MHz	1.140	1.200	1.260	V
		Normal Operation, R5F = 500MHz	1.188	1.250	1.320	V
VPP	Supply voltage range for the eFuse ROM domain	Normal Operation	No Connection			V
	Supply voltage range for the eFuse ROM domain during OTP programming	OTP Programming	1.65	1.7	1.75	V
$I_{(VPP)}$	VPP Current	$I_{(VPP)}$			100	mA
T_A	Ambient Temperature	Ambient Temperature	0	30	50	℃

(1) See Section 6.5 for more information

6.9.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP power supply must be disabled when not programming OTP registers.
- The VPP power supply must be ramped up after the proper device power-on sequence (for more details, see Section 6.11.2.1, *Power-On and Reset Sequencing*).

6.9.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-on sequencing. No voltage should be applied on the VPP terminal during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP terminal according to the specification in *VPP Specifications*.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP terminal.

6.9.4 Impact to Your Hardware Warranty

You accept that e-Fusing the TI Devices with security keys permanently alters them. You acknowledge that the e-Fuse can fail, for example, due to incorrect or aborted program sequence or if you omit a sequence step. Further the TI Device may fail to secure boot if the error code correction check fails for the Production Keys or if the image is not signed and optionally encrypted with the current active Production Keys. These types of situations will render the TI Device inoperable and TI will be unable to confirm whether the TI Devices conformed to their specifications prior to the attempted e-Fuse.

CONSEQUENTLY, TI WILL HAVE NO LIABILITY (WARRANTY OR OTHERWISE) FOR ANY TI DEVICES THAT HAVE BEEN e-FUSED WITH SECURITY KEYS.

6.10 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in Recommended Operating Conditions.

6.10.1 ZCZ Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

PARAMETER	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s) (3)
$R\Theta_{JC}$	Junction-to-case	6.5	N/A
$R\Theta_{JB}$	Junction-to-board	6.6	N/A
$R\Theta_{JA}$	Junction-to-free air	19.9	0
$R\Theta_{JA}$	Junction-to-moving air	13.7	1
		12.5	2
		11.9	3
Ψ_{JT}	Junction-to-package top	0.13	0
		0.38	1
		0.52	2
		0.61	3
Ψ_{JB}	Junction-to-board	6.5	0
		6.0	1
		5.9	2
		5.8	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) °C/W = degrees Celsius per watt
(3) m/s = meters per second

6.10.2 ZFG Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

PARAMETER	DESCRIPTION	℃/W(1) (2)	AIR FLOW (m/s) (3)
$R\Theta_{JC}$	Junction-to-case	7.1	N/A
$R\Theta_{JB}$	Junction-to-board	6.7	N/A
$R\Theta_{JA}$	Junction-to-free air	20.7	0
$R\Theta_{JA}$	Junction-to-moving air	14.5	1
		13.3	2
		12.6	3
Ψ_{JT}	Junction-to-package top	0.14	0
		0.40	1
		0.53	2
		0.64	3
Ψ_{JB}	Junction-to-board	6.5	0
		6.0	1
		5.9	2
		5.9	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) ℃/W = degrees Celsius per watt
(3) m/s = meters per second

6.10.3 ZEJ Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

PARAMETER	DESCRIPTION	℃/W(1) (2)	AIR FLOW (m/s) (3)
$R\Theta_{JC}$	Junction-to-case	7.1	N/A
$R\Theta_{JB}$	Junction-to-board	7	N/A
$R\Theta_{JA}$	Junction-to-free air	20.4	0
$R\Theta_{JA}$	Junction-to-moving air	14.6	1
		13.4	2
		12.7	3
Ψ_{JT}	Junction-to-package top	0.15	0
		0.42	1
		0.57	2
		0.67	3
Ψ_{JB}	Junction-to-board	7.0	0
		6.5	1
		6.4	2
		6.3	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) ℃/W = degrees Celsius per watt
(3) m/s = meters per second

6.10.4 ZNC Package Thermal Characteristics

It is recommended to perform thermal simulations at the system level with the worst-case device power consumption.

PARAMETER	DESCRIPTION	°C/W(1) (2)	AIR FLOW (m/s) (3)
$R\Theta_{JC}$	Junction-to-case	8.3	N/A
$R\Theta_{JB}$	Junction-to-board	5.8	N/A
$R\Theta_{JA}$	Junction-to-free air	21.9	0
$R\Theta_{JA}$	Junction-to-moving air	15.5	1
		14.3	2
		13.5	3
Ψ_{JT}	Junction-to-package top	0.15	0
		0.44	1
		0.58	2
		0.69	3
Ψ_{JB}	Junction-to-board	5.8	0
		5.4	1
		5.4	2
		5.3	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-6, Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Packages

(2) °C/W = degrees Celsius per watt
(3) m/s = meters per second

6.11 Timing and Switching Characteristics

Note

The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

6.11.1 Timing Parameters and Information

The timing parameter symbols used in *Timing and Switching Characteristics* sections are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in Table 6-1:

Table 6-1. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

6.11.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation.

Note

Please note that depending on the speed grade of the device, the VDD core voltage supply is different. This section uses the 1.2V/1.25V notation to reference this difference. For your specific device, please reference *Recommended Operating Connections* and *Operating Performance Points* for more information.

6.11.2.1 Power-On and Reset Sequencing

As with previous AM26x devices, AM261x has no sequencing requirement with respect to the primary core digital VDD 1.2V/1.25V and I/O power 3.3V rails. There are two on-die LDO that are supplied through the VDDS33 and VDDA33 power nets respectively. These on-die LDO generate the required VDDS1V8 and VDDA1V8 1.8V digital and analog power. The AM261x does require the minimum ramp time be respected for 3.3V power-on. Additional PORz and SOP boot mode latch timing must be respected by the EVM design as well. Power-On Sequencing describes the device power-on sequencing.

Table 6-2. AM261x Power-On Sequencing

PARAMETER		MIN	MAX	UNIT
t_{RAMP_3V3}	Minimal ramp time for the 3.3V digital VDDSHV_x power nets. Measured from GND to VDDSHV_x 3,.V nominal	100	–	µs
t_{RAMP_1V8}	Minimal ramp time for the 1.8V digital VDDSHV_x power nets. Measured from GND to VDDSHV_x 1.8V nominal.	100	–	µs
t_{RAMP_1V2}	Minimal ramp time for the 1.2V/1.25V core digital VDD and power nets. Measured from GND to VDD 1.2V/1.25V nominal.	100	–	µs
t_{DELAY_3V3}	Minimal delay between when the VDDSHV_x 3.3V power is at nominal voltage until the VDDSHV_x 1.8V and VDD 1.2V/1.25V nets are enabled.	(1)	–	µs
t_{DELAY_PG}	Minimal time between when VDDSHV_x 3.3V, VDDSHV_x 1.8V and VDD 1.2V/1.25V rails are all detected valid at nominal voltage before PORz signal can be transitioned from low to high voltage.	–	–	µs
$t_{SOP\_Sampled}$	Time from PORz de-assertion until the SOP[3:0] pins are sampled. This is a device internal pentameter. Sampling happens when the internally generated supplies are stable. For information only. Refer to T_{SU_SOP} and T_{H_SOP} parameters for application usage.	0	–	µs
t_{SU_SOP}	Setup time for SOP relative to PORz assertion.	20	–	µs
t_{H_SOP}	Hold time for SOP relative to WARMRSTn deassertion.	0	–	µs
$t_{WARMRSTn}$	Time from PORz de-assertion until the device de-asserts the WARMRESETn signal.	2.0	–	ms

(1) When using 1.8V OSPI flash, there is a minimum t_{DELAY_3V3} value of 50µs.

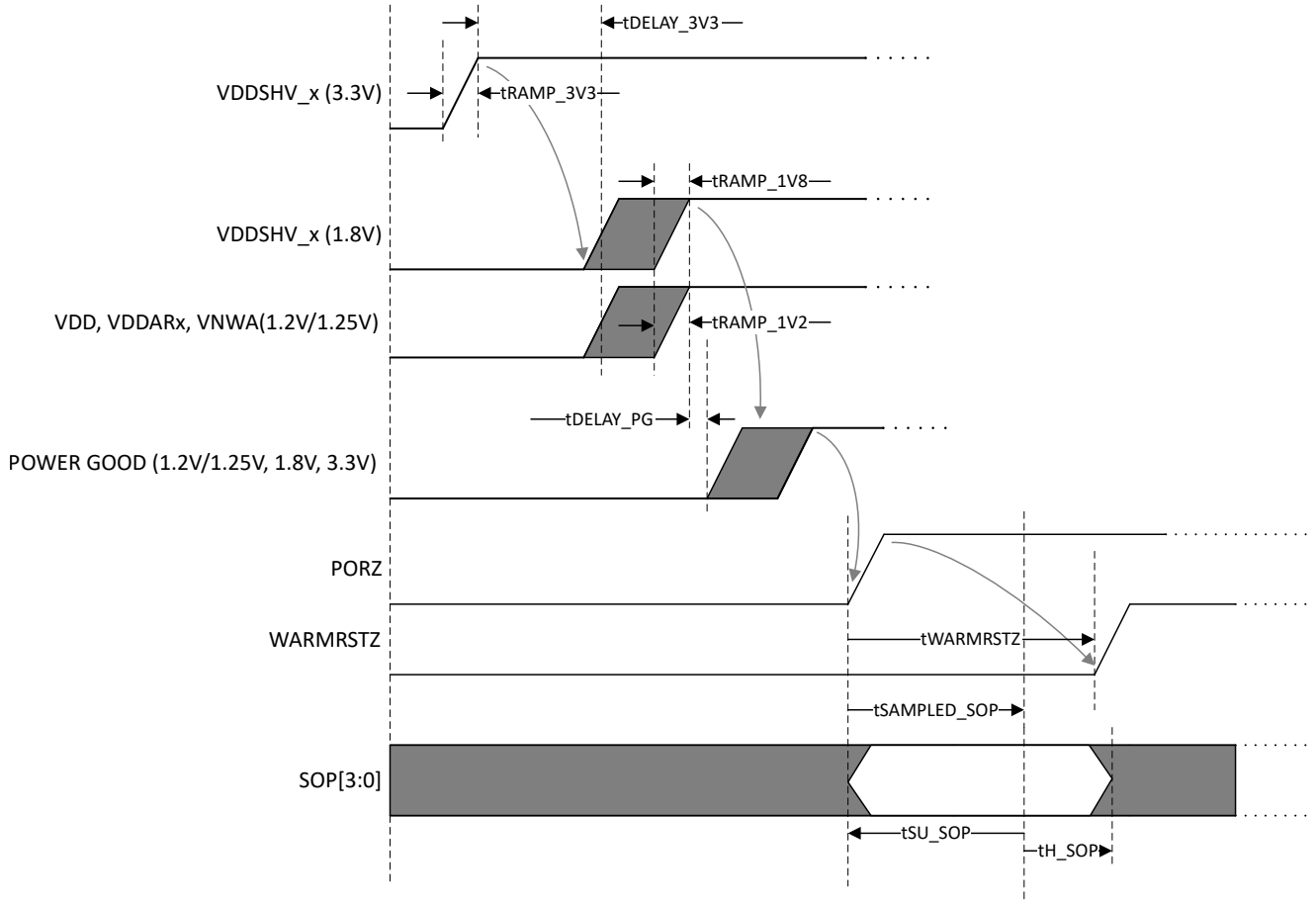


Figure 6-2. Power-On Sequencing

6.11.2.1.1 Power Reset Sequence Description

The following set of steps shall occur on the EVM and AM261x to boot the device from power-on reset.

1. PORz is held low by the external power supply monitor
2. VDDSHV_x 3.3V supply ramps to its nominal voltage
   a. This requires a logical AND be applied to the power good signal generated from each supply
3. Delay at least 50µs after VDDSHV_x 3.3VB is at valid range
4. VDDSHV_x 1.8V and VDD 1.2V/1.25V supplies ramp to their nominal voltages (no constraint on order of 1.8V and 1.2V/1.25V ramp)
5. SOP[3:0] pins held in their boot latch state
6. Power-Good supervisor output triggers based on valid 3.3V, 1.8V, and 1.2V/1.25V all being at valid range
7. PORz low to high transition is triggered by Power-Good supervisor output
   a. Warm Reset output will toggle low to high tWARMRSTZ seconds after PORz transition
8. After internal supply monitors show externally and internally generated supplies are stable, the SOP[3:0] pin states are latched
9. R5F cores are unhalted and SOP selected boot ROM execution begins

6.11.2.2 Power-Down Sequencing

Power-Down Sequencing describes the device power-down sequencing. The order of AM261x 1.8V, 1.2V/1.25V, and 3.3V does not matter.

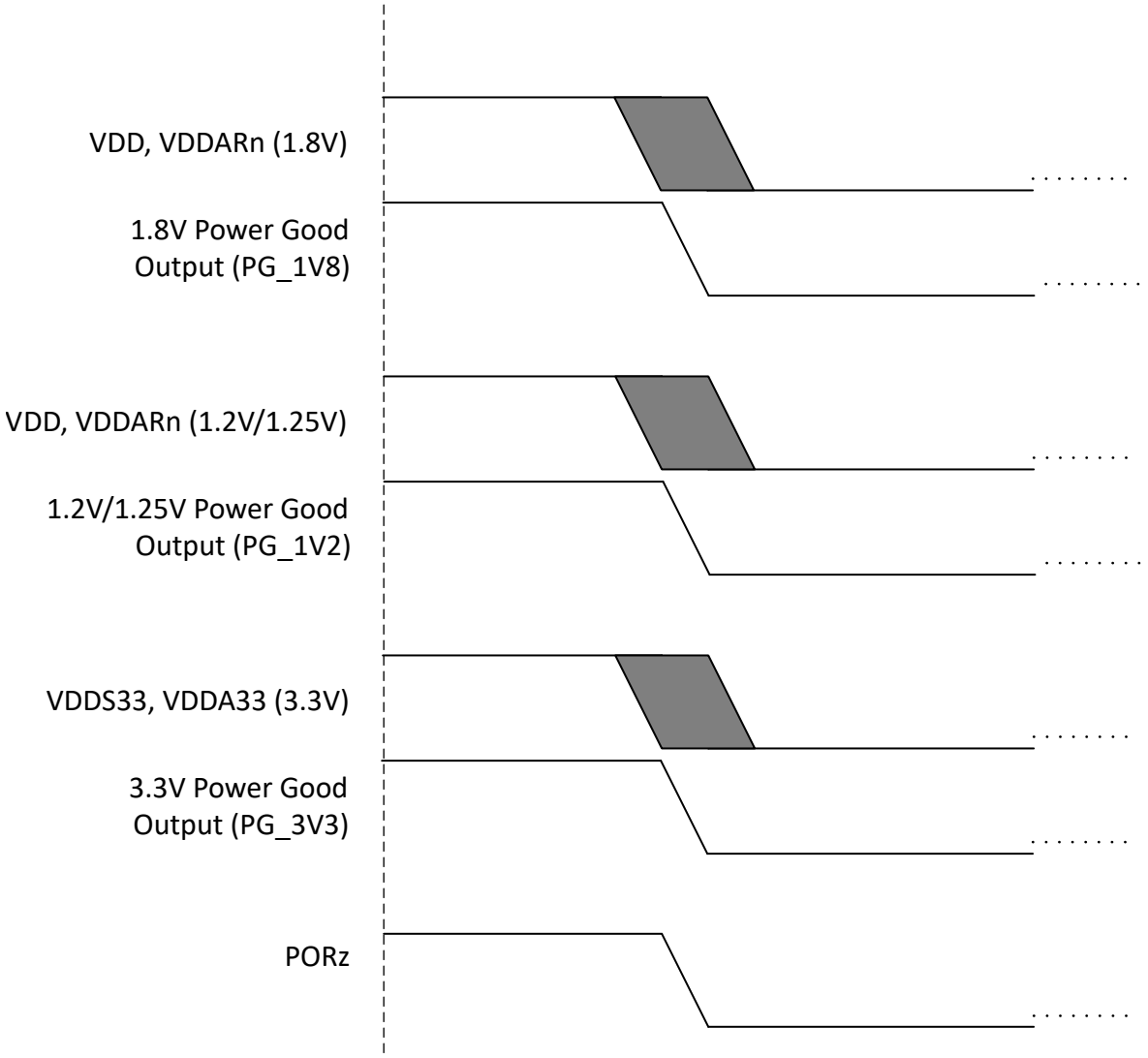


Figure 6-3. Power-Down Sequencing

6.11.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding subsections within the device specific TRM.

6.11.3.1 System Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	2	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	3	30	pF

6.11.3.2 Reset Timing

Tables and figures provided in this section define timing requirements and switching characteristics for reset related signals.

6.11.3.2.1 PORz Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST1	$t_{h(SUPPLIES\_VALID-PORz)}$	Hold time, PORz active (low) at Power-up after supplies valid (using external crystal)	0		ns
RST3	$t_{w(PORzL)}$	Pulse Width minimum, PORz low after Power-up (without removal of Power or system reference clock XTAL_XI/XO)	1000		ns

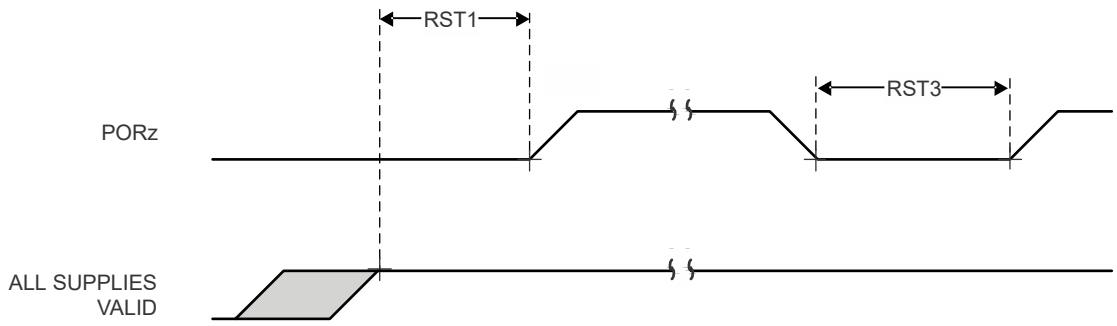


Figure 6-4. PORz Timing Requirements

6.11.3.2.2 WARMRSTn Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST4	$t_{d(PORzL:-WARMRSTnZ)}$	Delay time, PORz active (low) to WARMRSTn high impedance	0	0	ns
RST5	$t_{d(PORzH-WARMRSTnL)}$	Delay time, PORz inactive (high) to WARMRSTn active (low)	0	0	ns
RST6	$t_{d(PORzH-WARMRSTnH)}$	Delay time, PORz inactive (high) to WARMRSTn inactive (high)	2000000	6000000	ns

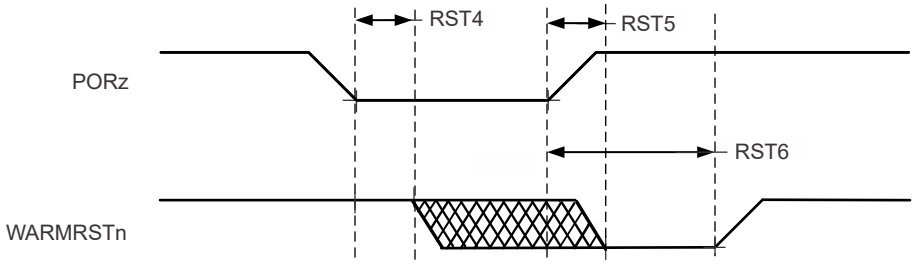


Figure 6-5. WARMRSTn Switching Characteristics

6.11.3.2.3 WARMRSTn Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RST10	$t_{w(WARMRSTnL)}$ (1)	Pulse Width minimum, WARMRSTn active (low)	500	16384000	ns

(1) This timing parameter is controlled by the TOP_RCM.WARM_RSTTIME1/2/3 registers. See the Reset section of the Technical Reference Manual for more details.

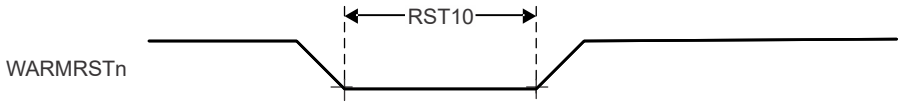


Figure 6-6. WARMRSTn Timing Requirements and Switching Characteristics

6.11.3.3 Safety Signal Timing

Tables and figures provided in this section define switching characteristics for SAFETY_ERRORn.

6.11.3.3.1 SAFETY_ERRORn Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SFTY1	$t_{c(SAFETY\_ERRORn)}$	Cycle time minimum, SAFETY_ERRORn (PWM mode enabled)	(P(1) × H(3)) + (P(1) × L)(4)		ns
SFTY2	$t_{w(SAFETY\_ERRORn)}$	Pulse width minimum, SAFETY_ERRORn active (PWM mode disabled)(5)	P(1) × R(2)		ns
SFTY3	$t_{d(ERROR\_CONDITION-SAFETY\_ERRORnL)}$	Delay time, ERROR_CONDITION to SAFETY_ERRORn active(5)	50 × P(1)		ns

(1) P = ESM functional clock
(2) R = Error Pin Counter Pre-Load Register count value
(3) H = Error Pin PWM High Pre-Load Register count value
(4) L = Error Pin PWM Low Pre-Load Register count value
(5) When PWM mode is enabled, SAFETY_ERRORn stops toggling after SFTY3 and will maintain its value (either high or low) until the error is cleared. When PWM mode is disabled, SAFETY_ERRORn is active low

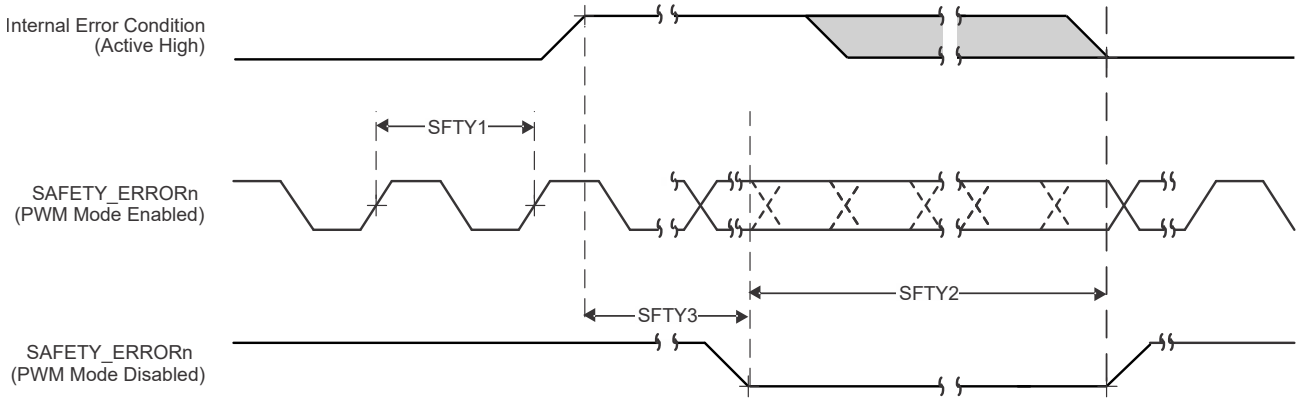


Figure 6-7. SAFETY_ERRORn Timing Requirements and Switching Characteristics

6.11.4 Clock Specifications

6.11.4.1 Input Clocks / Oscillators

6.11.4.1.1 Crystal Oscillator (XTAL) Parameters

PARAMETER		MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency (Fundamental mode oscillation only)	–50ppm	25	50ppm	MHz
Duty Cycle	Duty cycle output of XTAL	45	50	55	%
CC1	Capacitance of C_{L1} + C_{PCBXI}	12		24	pF
CC2	Capacitance of C_{L2} + C_{PCBXO}	12		24	pF
C_{shunt}	Crystal Circuit Shunt Capacitance			5	pF
ESR_{xtal}	Crystal Effective Series Resistance			46	Ω

6.11.4.1.2 External Clock Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
C_{Pkg}	Shunt Capacitance of package		0.01		pF
P_{xtal}	Power dissipation		$0.5 \times ESR \times (2 \times \pi \times F_{xtal} \times C_L \times 1.8)^2$		W
t_s	Startup time		1.5		ms

6.11.4.2 Clock Timing

Tables and figures provided in this section define timing requirements and switching characteristics for clock signals.

6.11.4.2.1 Clock Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CLK1	tc(EXT_REFCLK)	Cycle time minimum, EXT_REFCLK	10		ns
CLK2	tw(EXT_REFCLKH)	Pulse Duration minimum, EXT_REFCLK high	E(1) × 0.45	E(1) × 0.55	ns
CLK3	tw(EXT_REFCLKL)	Pulse Duration minimum, EXT_REFCLK low	E(1) × 0.45	E(1) × 0.55	ns

(1) E = EXT_REFCLK cycle time

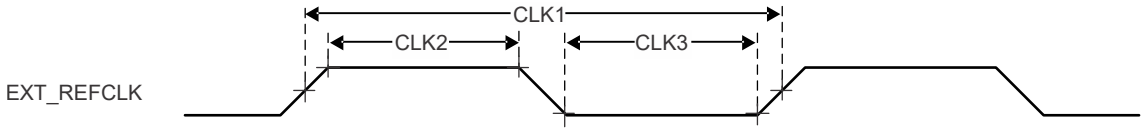


Figure 6-8. Clock Timing Requirements

6.11.4.2.2 Clock Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CLK4	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	10		ns
CLK5	$t_{w(CLKOUT0H)}$	Pulse Duration minimum, CLKOUT0 high	A(1) × 0.4	A(1) × 0.6	ns
CLK6	$t_{w(CLKOUT0L)}$	Pulse Duration minimum, CLKOUT0 low	A(1) × 0.4	A(1) × 0.6	ns
CLK7	$t_{c(CLKOUT1)}$	Cycle time minimum, CLKOUT1	10		ns
CLK8	$t_{w(CLKOUT1H)}$	Pulse Duration minimum, CLKOUT1 high	B(2) × 0.4	B(2) × 0.6	ns
CLK9	$t_{w(CLKOUT1L)}$	Pulse Duration minimum, CLKOUT1 low	B(2) × 0.4	B(2) × 0.6	ns

(1) A = CLKOUT0 cycle time
(2) B = CLKOUT1 cycle time

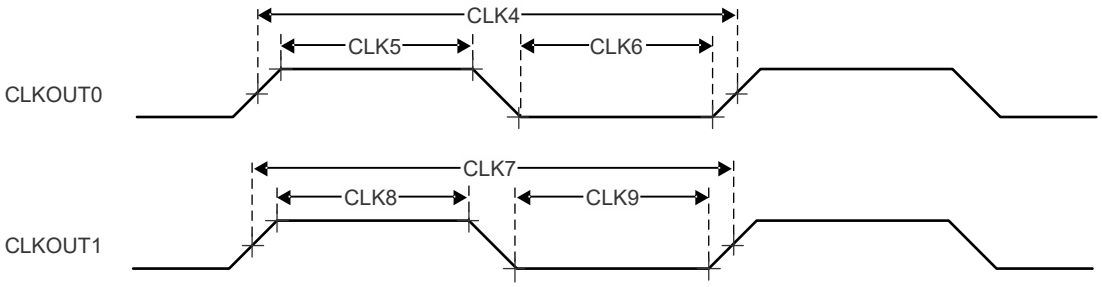


Figure 6-9. Clock Switching Characteristics

6.11.5 Peripherals

6.11.5.1 3-port Gigabit Ethernet MAC (CPSW)

Note

The CPSW supports two external Ethernet ports and one internal CPDMA host port.

For more details about features and additional description information on the device CPSW (3-port Gigabit Ethernet MAC), see the *Gigabit Ethernet Switch* section in the device TRM.

6.11.5.1.1 CPSW MDIO Timing

6.11.5.1.1.1 CPSW MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	10	20	pF

6.11.5.1.1.2 CPSW MDIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{su(MDIO-MDC)}$	Setup time, MDIO_DATA valid before MDIO_CLK high	25		ns
MDIO2	$t_{h(MDC-MDIO)}$	Hold time, MDIO_DATA valid after MDIO_CLK high	0		ns

6.11.5.1.1.3 CPSW MDIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO_CLK	50		ns
MDIO4	$t_{w(MDCH)}$	Pulse duration, MDIO_CLK high	19		ns
MDIO5	$t_{w(MDCL)}$	Pulse duration, MDIO_CLK low	19		ns
MDIO7	$t_{d(MDC\_MDIO)}$	Delay time, MDIO_CLK low to MDIO_DATA valid	–10	10	ns

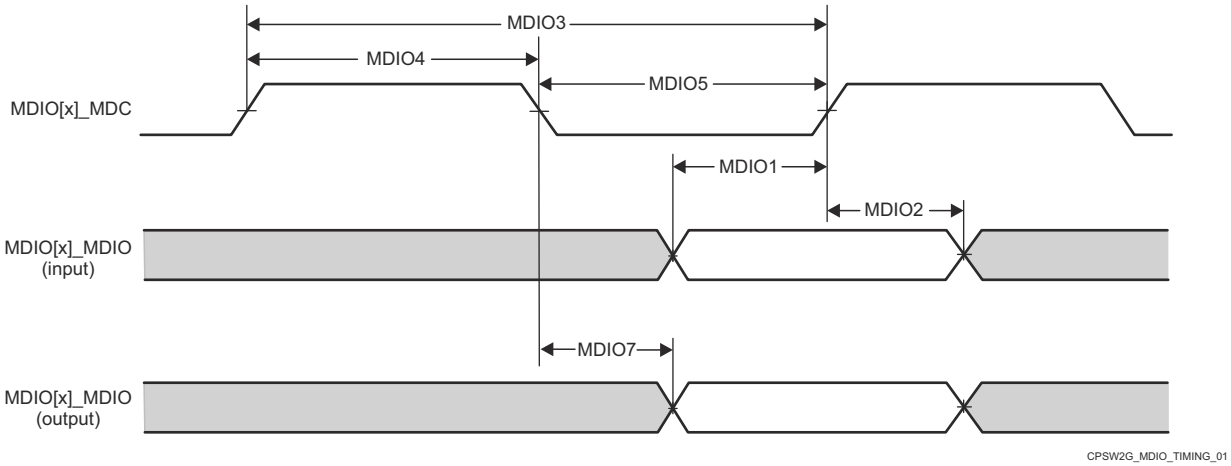


Figure 6-10. CPSW MDIO Timing Requirements and Switching Characteristics

6.11.5.1.2 CPSW RGMII Timing

6.11.5.1.2.1 CPSW RGMII Timing Conditions

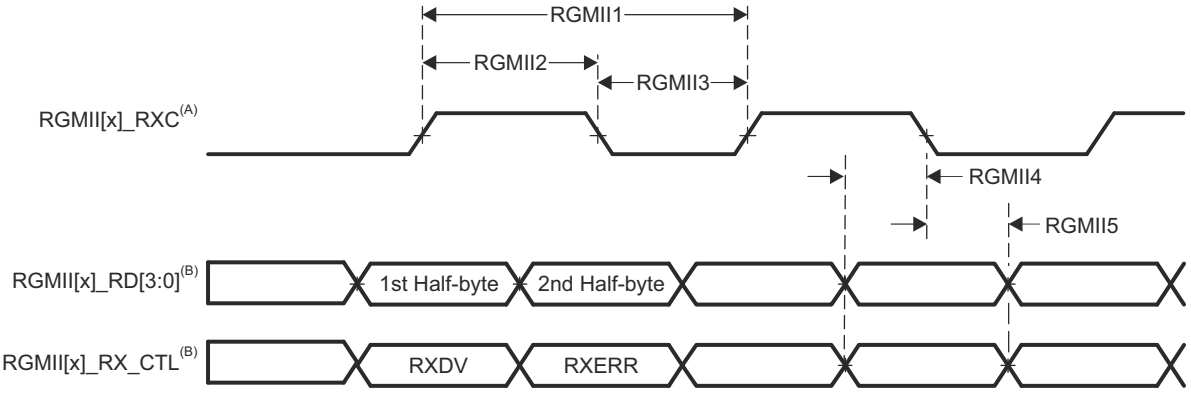
PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		2	20	pF
PCB Connectivity Requirements					
t_d (Trace Mismatch Delay)	Propagation Delay mismatch across all traces	RGMII[x]_RXC RGMII[x]_RD[3:0] RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC RGMII[x]_TD[3:0] RGMII[x]_TX_CTL		50	ps

6.11.5.1.2.2 CPSW RGMII[x]_RCLK Timing Requirements - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(RXC)}$	Cycle time, RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	tw(RXCH)	Pulse duration, RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	tw(RXCL)	Pulse duration, RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.11.5.1.2.3 CPSW RGMII[x]_RD[3:0], and RGMII[x]_RCTL Timing Requirements

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII4	$t_{su(RD-RXC)}$	Setup time, RD[3:0] valid before RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(RX\_CTL-RXC)}$	Setup time, RX_CTL valid before RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(RXC-RD)}$	Hold time, RD[3:0] valid after RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(RXC-RX\_CTL)}$	Hold time, RX_CTL valid after RXC high/low	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII[x]_RXC must be externally delayed relative to the data and control pins.

B. Data and control information is received using both edges of the clocks. RGMII[x]_RD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_RXC and data bits 7-4 on the falling edge of RGMII[x]_RXC. Similarly, RGMII[x]_RX_CTL carries RXDV on rising edge of RGMII[x]_RXC and RXERR on falling edge of RGMII[x]_RXC.

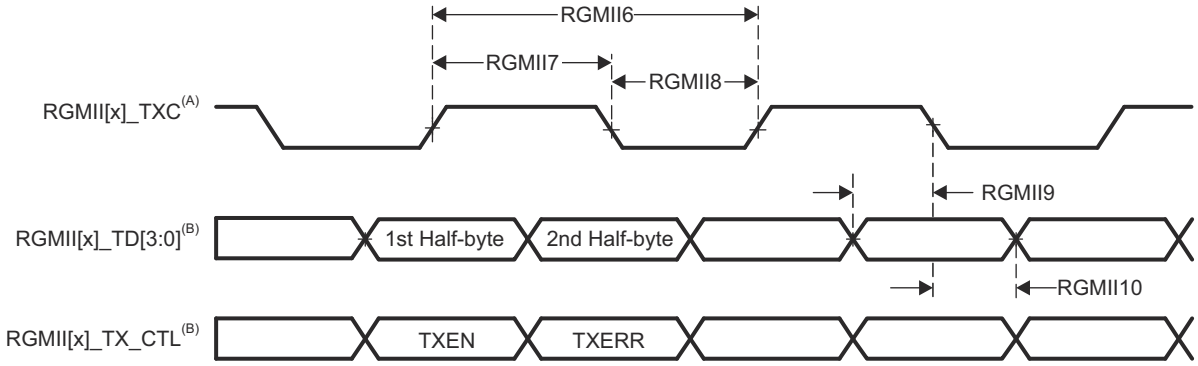
Figure 6-11. CPSW RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL Timing Requirements - RGMII Mode

6.11.5.1.2.4 CPSW RGMII[x]_TCLK Switching Characteristics - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII6	$t_{c(TXC)}$	Cycle time, TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(TXCH)}$	Pulse duration, TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(TXCL)}$	Pulse duration, TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.11.5.1.2.5 CPSW RGMII[x]_TD[3:0], and RGMII[x]_TCTL Switching Characteristics - RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(TD-TXC)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{osu(TX\_CTL-TXC)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
RGMII10	$t_{oh(TXC-TD)}$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns
	$t_{oh(TXC-TX\_CTL)}$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC high/low	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.2		ns



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is by default enabled after POR.

B. Data and control information is received using both edges of the clocks. RGMII[x]_TD[3:0] carries data bits 3-0 on the rising edge of RGMII[x]_TXC and data bits 7-4 on the falling edge of RGMII[x]_TXC. Similarly, RGMII[x]_TX_CTL carries TXEN on rising edge of RGMII[x]_TXC and TXERR on falling edge of RGMII[x]_TXC.

Figure 6-12. CPSW RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

6.11.5.1.3 CPSW RMII Timing

6.11.5.1.3.1 CPSW RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	VDD = 3.3V	0.4	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		3	25	pF

6.11.5.1.3.2 CPSW RMII[x]_REFCLK Timing Requirements - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII1	$t_{c(REF\_CLK)}$	Cycle time, REF_CLK	19.999	20	ns
RMII2	$t_{w(REF\_CLKH)}$	Pulse duration, REF_CLK High	7	13	ns
RMII3	$t_{w(REF\_CLKL)}$	Pulse duration, REF_CLK Low	7	13	ns

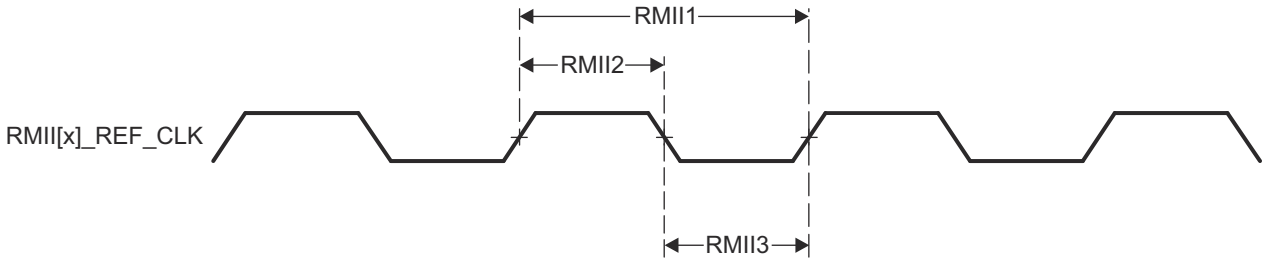


Figure 6-13. CPSW RMII[x]_REF_CLK Timing Requirements – RMII Mode

6.11.5.1.3.3 CPSW RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RXER Timing Requirements - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII4	$t_{su(RXD-REF\_CLK)}$	Setup time, RXD[1:0] valid before REF_CLK	4		ns
	$t_{su(CRS\_DV-REF\_CLK)}$	Setup time, CRS_DV valid before REF_CLK	4		ns
	$t_{su(RX\_ER-REF\_CLK)}$	Setup time, RX_ER valid before REF_CLK	4		ns
RMII5	$t_{h(REF\_CLK-RXD)}$	Hold time, RXD[1:0] valid after REF_CLK	2		ns
	$t_{h(REF\_CLK-CRS\_DV)}$	Hold time, CRS_DV valid after REF_CLK	2		ns
	$t_{h(REF\_CLK-RX\_ER)}$	Hold time, RX_ER valid after REF_CLK	2		ns

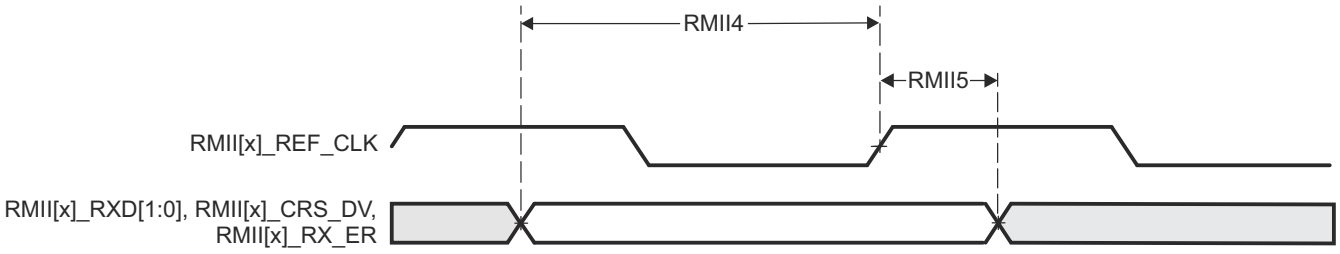


Figure 6-14. CPSW RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

6.11.5.1.3.4 CPSW RMII[x]_TXD[1:0], and RMII[x]_TXEN Switching Characteristics - RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
RMII6	$t_{d(REF\_CLK-TXD)}$	Delay time, REF_CLK High to TXD[1:0] valid	2	10	ns
	$t_{d(REF\_CLK-TXEN)}$	Delay time, REF_CLK to TXEN valid	2	10	ns

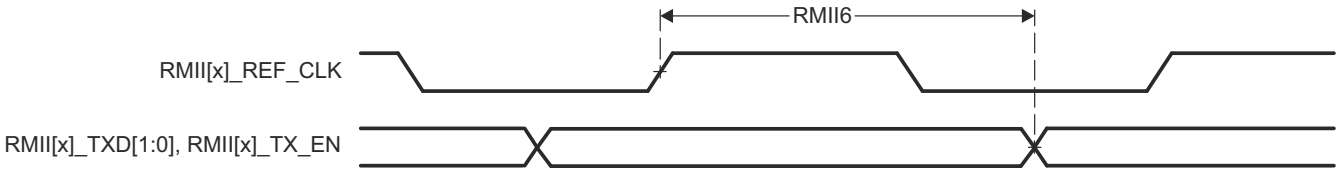


Figure 6-15. CPSW RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

6.11.5.2 Enhanced Capture (eCAP)

Note

The device has multiple ECAP modules. The generic CAP_ prefix is used to represent the signal names for all ECAP instances.

For more information, see *Enhanced Capture (ECAP) Module* section in the device TRM.

6.11.5.2.1 ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.2.2 ECAP Timing Requirements

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
CAP1	$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$(2 + X^{(2)}) \times P^{(1)}$		ns
			Synchronous	$(3 + X^{(2)}) \times P^{(1)}$		
			With input qualifier	$(2 + X^{(2)}) \times P^{(1)} + U^{(3)}$		

(1) P = sysclk period in ns.
(2) X = value of ECCTL0_TYPE3[QUALPRD] setting.
(3) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode

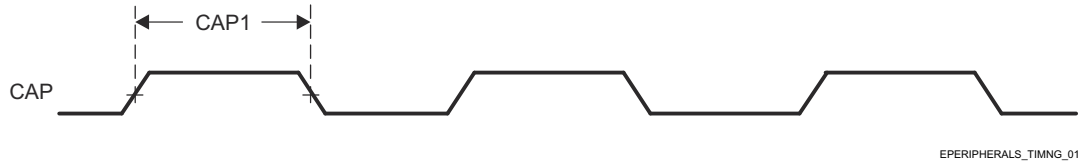


Figure 6-16. ECAP Timings Requirements

6.11.5.2.3 ECAP Switching Characteristics

(1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(APWM)}$	Pulse duration, APWMx output high/low	10		ns

(1) Some ECAP signals are pinmuxed with I2C0 SDA and SCL pins. These pins use an alternate open drain voltage buffer and may not meet the specified parameters. Values are pending additional post-silicon validation.

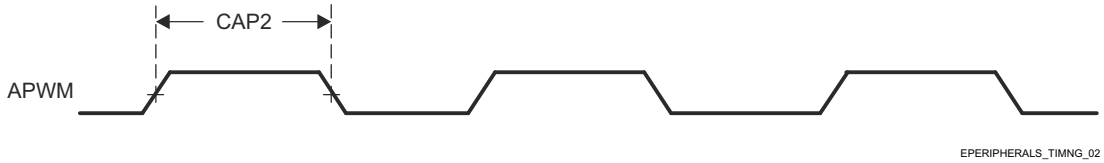


Figure 6-17. ECAP Switching Characteristics

6.11.5.3 Enhanced Pulse Width Modulation (ePWM)

Note

The device has multiple EPWM modules. The generic EHRPWM_ prefix is used to represent the signal names for all EPWM instances.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in the device TRM.

6.11.5.3.1 EPWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.3.2 EPWM Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(SYNCIN)}$	Pulse duration, EHRPWM_SYNCI	2P(1)		ns
PWM7	$t_{w(TZ)}$	Pulse duration, EHRPWM_TZn_IN low	1P(1)		ns

(1) P = sysclk period in ns.

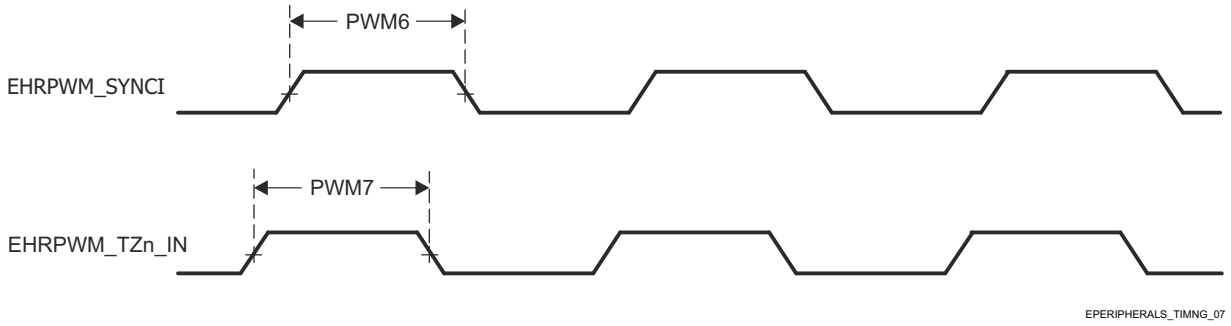


Figure 6-18. EPWM Timing Requirements

6.11.5.3.3 EPWM Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(PWM)}$	Pulse duration, EHRPWM_A/B high/low	20		ns
PWM2	$t_{w(SYNCOUT)}$	Pulse duration, EHRPWM_SYNCO	8P(1)		ns
PWM3	$t_{d(TZ-PWM)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B forced high/low		30	ns
PWM4	$t_{d(TZ-PWMZ)}$	Delay time, EHRPWM_TZn_IN active to EHRPWM_A/B Hi-Z		30	ns
PWM5	$t_{w(SOC)}$	Pulse duration, EHRPWM_SOCA/B output	32P(1)		ns

(1) P = sysclk period in ns.

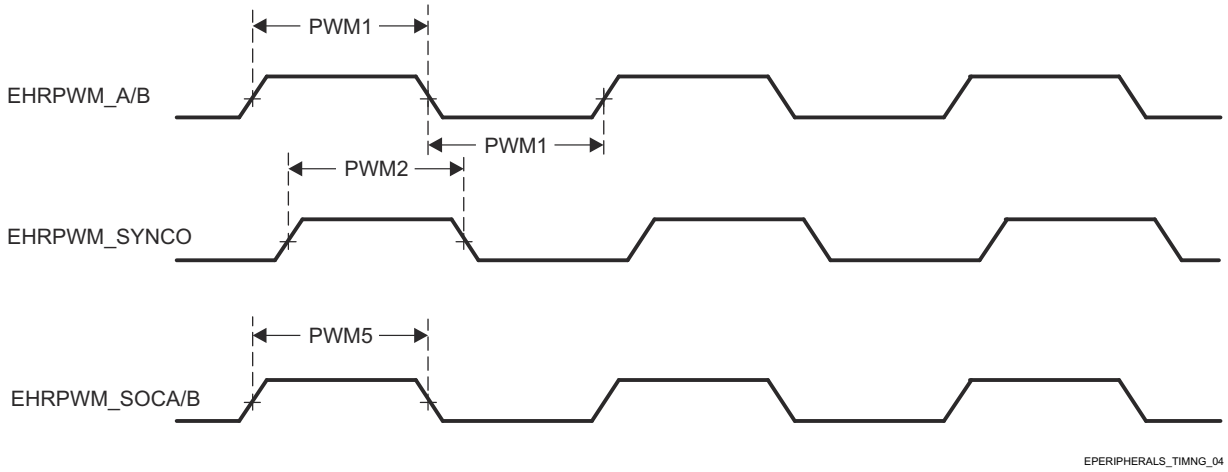


Figure 6-19. EHRPWM Switching Characteristics

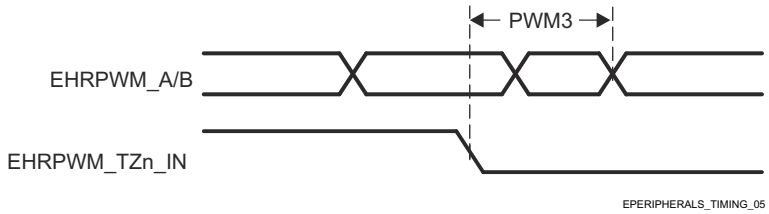


Figure 6-20. EHRPWM_TZn_IN to EHRPWM_A/B Forced Switching Characteristics

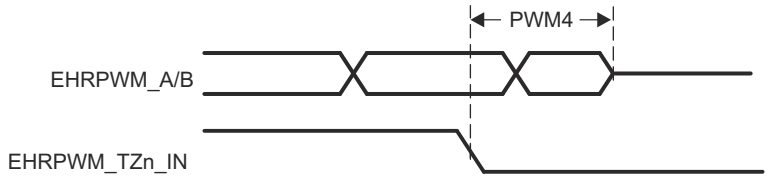


Figure 6-21. EHRPWM_TZn_IN to EHRPWM_A/B Hi-Z Switching Characteristics

EPWM Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1)	70	100	180	ps

(1) The MEP step size will be largest at high temperature and minimum voltage on VDD. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

6.11.5.4 Enhanced Quadrature Encoder Pulse (eQEP)

Note

The device has multiple EQEP modules. The generic QEP_ prefix is used to represent the signal names for all EQEP instances.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in the device TRM.

6.11.5.4.1 EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.4.2 EQEP Timing Requirements

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
QEP1	$t_{w(QEPP)}$	QEP input period	Synchronous[3]	3P[1]		ns
			With input qualifier	2 × (P[1] + U[2])		
QEP2	$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous[3]	2 + 3P[1]		ns
			With input qualifier	2P[1] + U[2]		
QEP3	$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous[3]	3P[1]		ns
			With input qualifier	2P[1] + U[2]		
QEP4	$t_{w(STROBH)}$	QEP Strobe High time	Synchronous[3]	3P[1]		ns
			With input qualifier	2P[1] + U[2]		
QEP5	$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous[3]	3P[1]		ns
			With input qualifier	2P[1] + U[2]		

(1) P = sysclk period in ns.
(2) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode.
(3) The GPIO GPxQSELn Asynchronous mode should not be used for EQEP module input pins.

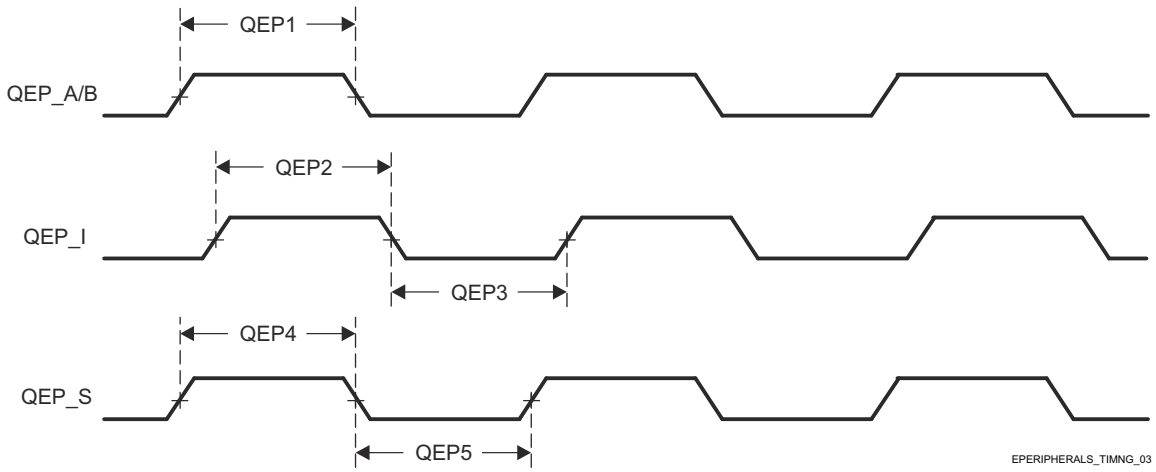


Figure 6-22. EQEP Timing Requirements

6.11.5.4.3 EQEP Switching Characteristics

(3)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
QEP6	$t_{d(CNTR)xin}$	Delay time, external clock to internal counter increment		4 + U(2) + 6P(1)	ns
QEP7	$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		4 + U(2) + 7P(1) + 4	ns

(1) P = sysclk period in ns.
(2) U = the input qualifier sampling window. See GPIO Electrical Data and Timing section for details on Input Qualifier Mode.
(3) Some EQEP signals are pinmuxed with I2C0 SDA and SCl pins. These pins use an alternate open drain voltage buffer and may not meet the specified parameters. Values are pending additional post-silicon validation.

6.11.5.5 Fast Serial Interface (FSI)

Note

The device has multiple FSI modules. FSIn is a generic prefix applied to FSI signal names, where n represents the specific FSI module.

For more information, see *Fast Serial Interface* section in the device TRM.

6.11.5.5.1 FSI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.8	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	7	pF

6.11.5.5.2 FSIRX Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIR1	$t_{c(RX\_CLK)}$	Cycle time, FSIRXn_CLK	16.67		ns
FSIR2	$t_{w(RX\_CLK)}$	Pulse width, FSIRXn_CLK low or FSIRXn_CLK high	0.35P(1) – 1	0.65P(1) + 1	ns
FSIR3	$t_{su(RX\_D–RX\_CLK)}$	Setup time, FSIRXn_D[0:1] valid before FSIRXn_CLK	1.7		ns
FSIR4	$t_{h(RX\_CLK–RX\_D)}$	Hold time with respect to both edges of FSIRXn_CLK	2		ns

(1) $P = T_{c(RXCLK)}$ = RX Interface clock period in ns.

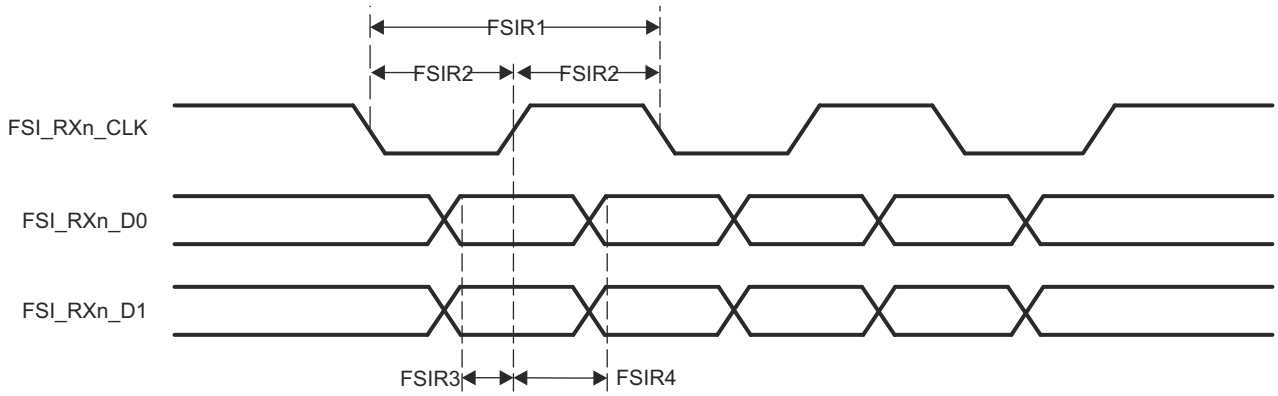


Figure 6-23. FSI Timing Requirements

6.11.5.5.3 FSIRX Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIR5	$t_{d(RX\_CLK)}$	FSIRXn_CLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
FSIR6	$t_{d(RX\_D0)}$	FSIRXn_D0 delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
FSIR7	$t_{d(RX\_D1)}$	FSIRXn_D1 delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31	10	30	ns
FSIR8	$t_{d(DELAY\_ELEMENT)}$	Incremental delay of each delay line element for FSIRXn_CLK, FSIRXn_D0, and FSIRXn_D1	0.3	1	ns

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIR_TDM1	$t_{skew(RX\_CLK-TX\_TDM\_D)}$	Delay skew between FSIRXn_TDM_CLK delay and FSIRXn_TDM_D[0:1]	–3	3	ns
FSIR_TDM2	$t_{skew(RX\_CLK-TX\_TDM\_CLK)}$	Delay time, FSIRXn_CLK input to FSITXn_TDM_CLK output	2	12	ns
FSIR_TDM3	$t_{skew(RX\_D0-TX\_TDM\_D0)}$	Delay time, FSIRXn_D0 input to FSITXn_TDM_D0 output	2	12	ns
FSIR_TDM4	$t_{skew(RX\_D1-TX\_TDM\_D1)}$	Delay time, FSIRXn_D1 input to FSITXn_TDM_D1 output	2	12	ns

6.11.5.5.4 FSITX Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIT1	$t_{c(TX\_CLK)}$	Cycle time, FSITXn_CLK	16.67		ns
FSIT2	$t_{w(TX\_CLK)}$	Pulse width, FSITXn_CLK low or FSITXn_CLK high	0.5P(1) – 1	0.5P(1) + 1	ns
FSIT3	$td_{(TX\_CLK-TX\_D)}$	Delay time, FSITXn_Dx valid after FSITXn_CLK high or FSITXn_CLK low	0.25P(1) – 2	0.25P(1) + 2	ns
FSIT4	$t_{d(TXCLKL)}$	FSITXn_CLK delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
FSIT5	$t_{d(TX\_D0)}$	FSITXn_D0 delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
FSIT6	$t_{d(TX\_D1)}$	FSITXn_D1 delay compensation at TX_DLYLINE_CTRL[TXCLK_DLY]=31	9.95	30	ns
FSIT7	$t_{d(TX\_DELAY\_ELEMENT)}$	Incremental delay of each delay line element for FSITXn_CLK, FSITXn_D0, and FSITXn_D1	0.3	1	ns
FSIT_TDM1	$t_{skew(TX\_TDM\_CLK-TX\_TDM\_D)}$	Delay skew introduced between FSITXn_TDM_CLK delay and FSITXn_TDM_D[0:1] delays	–2.5	2.5	ns
FSIT_TDM2	$t_{skew(TX\_TDM\_CLK-TX\_CLK)}$	Delay time, FSITXn_TDM_CLK input to FSITXn_CLK output	2	12	ns
FSIT_TDM3	$t_{skew(TX\_TDM\_D0-TX\_D0)}$	Delay time, FSITXn_TDM_D0 input to FSITXn_D0 output	2	12	ns
FSIT_TDM4	$t_{skew(TX\_TDM\_D1-TX\_D1)}$	Delay time, FSITXn_TDM_D1 input to FSITXn_D1 output	2	12	ns

(1) P = $t_{c(TX\_CLK)}$ = FSITX Interface clock period in ns.

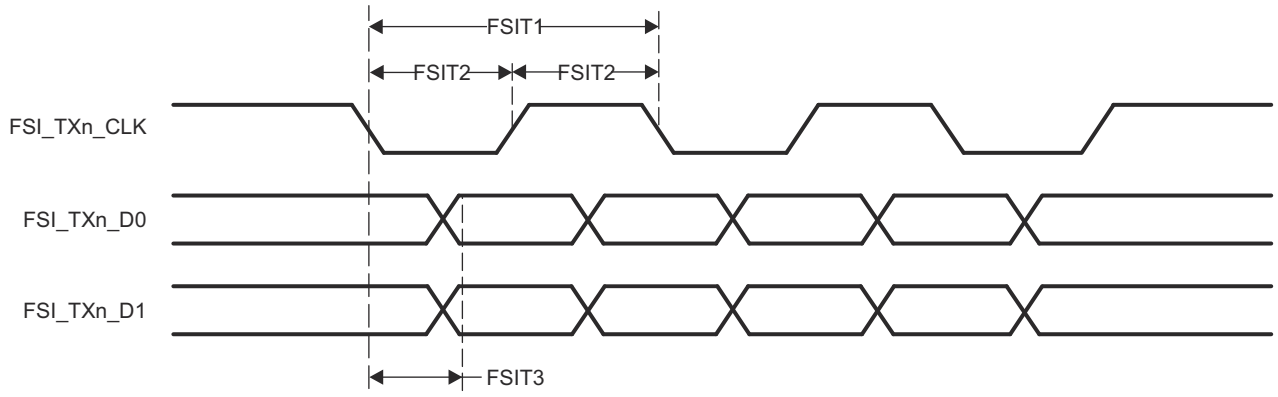


Figure 6-24. FSI Switching Characteristics - FSI Mode

6.11.5.5.5 FSITX SPI Signaling Mode Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FSIT4	$t_{c(TX\_CLK)}$	Cycle time, FSITXn_CLK	16.67		ns
FSIT5	$t_{w(TX\_CLK)}$	Pulse width, FSITXn_CLK low or FSITXn_CLK high	0.5P(1) – 1	0.5P(1) + 1	ns
FSIT6	$t_{d(TX\_CLKH–TX\_D0)}$	Delay time, FSITXn_CLK high to FSITXn_D0 valid		3	ns
FSIT7	$t_{d(TX\_D1-TX\_CLK)}$	Delay time, FSITXn_D1 low to FSITXn_CLK high	P(1) – 3		ns
FSIT8	$t_{d(TX\_CLK-TX\_D1)}$	Delay time, FSITXn_CLK low to FSITXn_D1 high	P(1)		ns

(1) P = $t_{c(TX\_CLK)}$ = FSITX Interface clock period in ns.

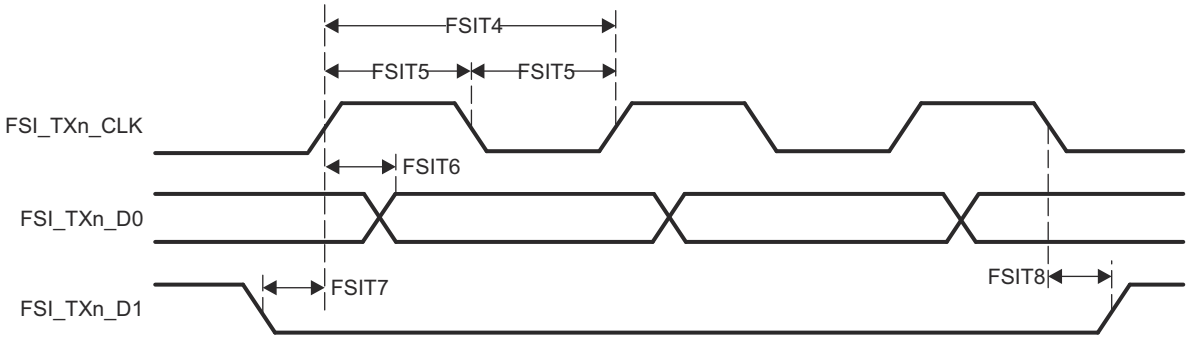


Figure 6-25. FSI Switching Characteristics - SPI Mode

6.11.5.6 General Purpose Input/Output (GPIO)

For more details about features and additional description information on the device GPIO, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *General-Purpose Interface (GPIO)* section in the device TRM.

6.11.5.6.1 GPIO Timing Conditions

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate		0.75	6.6	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	LVCMOS	3	10	pF
		I2C OD FS(1)	3	10	pF

(1) A pull-up resistor is required for buffer type *I2C OD FS*.

6.11.5.6.2 GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
D3	$t_{w(GPIO\_IN)}$	Minimum Input Pulse Width	LVCMOS	2P(1) + 2		ns
D4			I2C OD FS(2)	2P(1) + 2		ns

(1) P = functional clock period in ns.
(2) A pull-up resistor is required for buffer type *I2C OD FS*.

6.11.5.6.3 GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
D1	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width	LVCMOS	0.975P(1) – 2		ns
D2	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width Low	I2C OD FS(2)	2P(1) + 160		ns
D3	$t_{w(GPIO\_OUT)}$	Minimum Output Pulse Width High	I2C OD FS(2)	2P(1) + 160		ns

(1) P = functional clock period in ns.
(2) A pull-up resistor is required for buffer type *I2C OD FS*.

6.11.5.7 General Purpose Memory Controller (GPMC)

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see the *General-Purpose Memory Controller (GPMC)* section in the device TRM.

6.11.5.7.1 GPMC Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate		1.65	4	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance		3	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	100MHz	140	720	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces			200	ps

6.11.5.7.2 GPMC/NOR Flash Timing Requirements - Synchronous Mode 100MHz

(1) (2)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
F12	$t_{su(dV-clkH)}$	Setup time, GPMC0_AD[31:0] valid before GPMC0_CLK high	div_by_1_mode (4)	1.81		ns
			not_div_by_1_mode(5)	1.06		ns
F13	$t_{h(clkH-dV)}$	Hold time, GPMC0_AD[31:0] valid after GPMC0_CLK high	div_by_1_mode (4)	2.29		ns
			not_div_by_1_mode(5)	2.29		ns
F21	$t_{su(waitV-clkH)}$	Setup time, GPMC0_WAIT[x](3) valid before GPMC0_CLK high	div_by_1_mode (4)	1.81		ns
			not_div_by_1_mode(5)	1.06		ns
F22	$t_{h(clkH-waitV)}$	Hold time, GPMC0_WAIT[x](3) valid after GPMC0_CLK high	div_by_1_mode (4)	2.29		ns
			not_div_by_1_mode(5)	2.29		ns

(1) 100MHz GPMC_FCLK selected - CTRLMMR_GPMC_CLKSEL[0] CLK_SEL = 1 = MAIN_PLL2_HSDIV7_CLKOUT (100/60 MHz).
(2) Trace length from GPMC pins to device assumed to be less than 4" and length matched to within 200ps for 100MHz Synchronous Mode.
(3) In GPMC_WAIT[x], x is equal to 0 or 1.
(4) In div_by_1_mode, GPMC0_CLK refers to either GPMC0_CLKOUT or GPMC0_FCLK_MUX (free-running). Both signals are pin-muxed to the same pin.
GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
– GPMC0_CLK frequency = GPMC_FCLK frequency
(5) In not_div_by_1_mode, GPMC_CLK only refers to GPMC0_CLKOUT. GPMC0_FCLK_MUX cannot be clock divided to match the GPMC0_CLKOUT frequency if GPMCFCLKDIVIDER > 0.
GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
– GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)

6.11.5.7.3 GPMC/NOR Flash Switching Characteristics - Synchronous Mode 100MHz

(18) (19) (20)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
F0	$t_{c(clk)}$	Clock period, GPMC0_CLK, GPMC0_FCLK_MUX		10(21)		ns
F1	$t_{w(clk)}$	Typical pulse duration, GPMC0_CLK high or low		0.475P(16) – 0.3(21)		ns
F2	$t_{d(clkH-csnV)}$	Delay time, GPMC0_CLK rising edge to GPMC0_CSn[x](15) transition		F(6) – 2.2(21)	F(6)+3.75	ns
F3	$t_{d(clkH-csnIV)}$	Delay time, GPMC0_CLK rising edge to GPMC0_CSn[x](15) invalid		E(5) – 2.2	E(5)+3.18	ns
F4	$t_{d(aV-clk)}$	Delay time, GPMC0_A[27:1] valid to GPMC0_CLK first edge		B(2) – 2.3(21)	B(2) + 4.5	ns
F5	$t_{d(clkH-aIV)}$	Delay time, GPMC0_CLK rising edge to GPMC0_A[27:1] invalid		–2.3(21)	4.5	ns
F6	$t_{d(be[x]nV-clk)}$	Delay time, GPMC0_BE0n_CLE, GPMC0_BE1n valid to GPMC0_CLK first edge		B(2) – 2.3(21)	B(2) + 1.9	ns
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, GPMC0_CLK rising edge to GPMC0_BE0n_CLE, GPMC0_BE1n invalid(12)		D(4) – 2.3(21)	D(4) + 1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC0_CLK falling edge to GPMC0_BE0n_CLE, GPMC0_BE1n invalid(13)		D(4) – 2.3(21)	D(4) + 1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC0_CLK falling edge to GPMC0_BE0n_CLE, GPMC0_BE1n invalid(14)		D(4) – 2.3(21)	D(4) + 1.9	ns
F8	$t_{d(clkH-advn)}$	Delay time, GPMC0_CLK rising edge to GPMC0_ADVn_ALE transition		G(7) (8) – 2.3(21)	G(7) (8) + 4.5	ns
F9	$t_{d(clkH-advnIV)}$	Delay time, GPMC0_CLK rising edge to GPMC0_ADVn_ALE invalid		D(4) – 2.3(21)	D(4) + 4.5	ns
F10	$t_{d(clkH-oen)}$	Delay time, GPMC0_CLK rising edge to GPMC0_OEn_REn transition		H(9) – 2.3(21)	H(9) + 3.5	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, GPMC0_CLK rising edge to GPMC0_OEn_REn invalid		H(9) – 2.3(21)	H(9) + 3.5	ns
F14	$t_{d(clkH-wen)}$	Delay time, GPMC0_CLK rising edge to GPMC0_WEn transition		I(10) – 2.3(21)	I(10) + 4.5	ns
F15	$t_{d(clkH-do)}$	Delay time, GPMC0_CLK rising edge to GPMC0_AD[31:0] transition(12)		J(11) – 2.3(21)	J(11) + 2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC0_CLK falling edge to GPMC0_AD[31:0] data bus transition(13)		J(11) – 2.3(21)	J(11) + 2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC0_CLK falling edge to GPMC0_AD[31:0] data bus transition(14)		J(11) – 2.3(21)	J(11) + 2.7	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, GPMC0_CLK rising edge to GPMC0_BE0n_CLE transition(12)		J(11) – 2.3(21)	J(11) + 1.9	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC0_CLK falling edge to GPMC0_BE0n_CLE, GPMC0_BE1n transition(13)		J(11) – 2.3(21)	J(11) + 1.9	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC0_CLK falling edge to GPMC0_BE0n_CLE, GPMC0_BE1n transition(14)		J(11) – 2.3(21)	J(11) + 1.9	ns
F18	$t_{w(csnV)}$	Pulse duration, GPMC0_CSn[x](15) low	Read	A(1)		ns
			Write	A(1)		ns
F19	$t_{w(be[x]nV)}$	Pulse duration, GPMC0_BE0n_CLE, GPMC0_BE1n low	Read	C(3)		ns
			Write	C(3)		ns

(18) (19) (20)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
F20	$t_{w(advnV)}$	Pulse duration, GPMC0_ADVn_ALE low	Read	K(17)		ns
			Write	K(17)		ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
With n being the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK(18)

(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst read: C = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst write: C = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
With n being the page burst access number.

(4) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)

(5) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)

(6) For csn falling edge (CS activated):
– Case GpmcFCLKDivider = 0:
– F = 0.5 × CSExtraDelay × GPMC_FCLK(18)
– Case GpmcFCLKDivider = 1:
– F = 0.5 × CSExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
– F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– F = 0.5 × CSExtraDelay × GPMC_FCLK(18) if ((CSOnTime - ClkActivationTime) is a multiple of 3)
– F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK(18) if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
– F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK(18) if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
– Case GpmcFCLKDivider = 0:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18)
– Case GpmcFCLKDivider = 1:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
– G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18) if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
– G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
– G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)
For ADV rising edge (ADV deactivated) in Reading mode:
– Case GpmcFCLKDivider = 0:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18)
– Case GpmcFCLKDivider = 1:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
– G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18) if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
– G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
– G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For ADV rising edge (ADV deactivated) in Writing mode:
– Case GpmcFCLKDivider = 0:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18)
– Case GpmcFCLKDivider = 1:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
– G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– G = 0.5 × ADVExtraDelay × GPMC_FCLK(18) if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
– G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
– G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK(18) if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):
– Case GpmcFCLKDivider = 0:
– H = 0.5 × OEExtraDelay × GPMC_FCLK(18)

– Case GpmcFCLKDivider = 1:
– H = 0.5 × OEExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
– H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– H = 0.5 × OEExtraDelay × GPMC_FCLK(18) if ((OEOnTime - ClkActivationTime) is a multiple of 3)
– H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(18) if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
– H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(18) if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)
For OE rising edge (OE deactivated):
– Case GpmcFCLKDivider = 0:
– H = 0.5 × OEExtraDelay × GPMC_FCLK(18)
– Case GpmcFCLKDivider = 1:
– H = 0.5 × OEExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
– H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– H = 0.5 × OEExtraDelay × GPMC_FCLK(18) if ((OEOffTime - ClkActivationTime) is a multiple of 3)
– H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK(18) if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
– H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK(18) if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10) For WE falling edge (WE activated):
– Case GpmcFCLKDivider = 0:
– I = 0.5 × WEExtraDelay × GPMC_FCLK(18)
– Case GpmcFCLKDivider = 1:
– I = 0.5 × WEExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
– I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– I = 0.5 × WEExtraDelay × GPMC_FCLK(18) if ((WEOnTime - ClkActivationTime) is a multiple of 3)
– I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(18) if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
– I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(18) if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)
For WE rising edge (WE deactivated):
– Case GpmcFCLKDivider = 0:
– I = 0.5 × WEExtraDelay × GPMC_FCLK (18)
– Case GpmcFCLKDivider = 1:
– I = 0.5 × WEExtraDelay × GPMC_FCLK(18) if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
– I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(18) otherwise
– Case GpmcFCLKDivider = 2:
– I = 0.5 × WEExtraDelay × GPMC_FCLK(18) if ((WEOffTime - ClkActivationTime) is a multiple of 3)
– I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK(18) if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
– I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK(18) if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(11) J = GPMC_FCLK(18)

(12) First transfer only for CLK DIV 1 mode.

(13) Half cycle; for all data after initial transfer for CLK DIV 1 mode.

(14) Half cycle of GPMC_CLK_OUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLK_OUT divide down from GPMC_FCLK.

(15) In GPMC_CSn[x], x is equal to 0, 1, 2 or 3. In GPMC_WAIT[x], x is equal to 0 or 1.

(16) P = GPMC_CLK period in ns

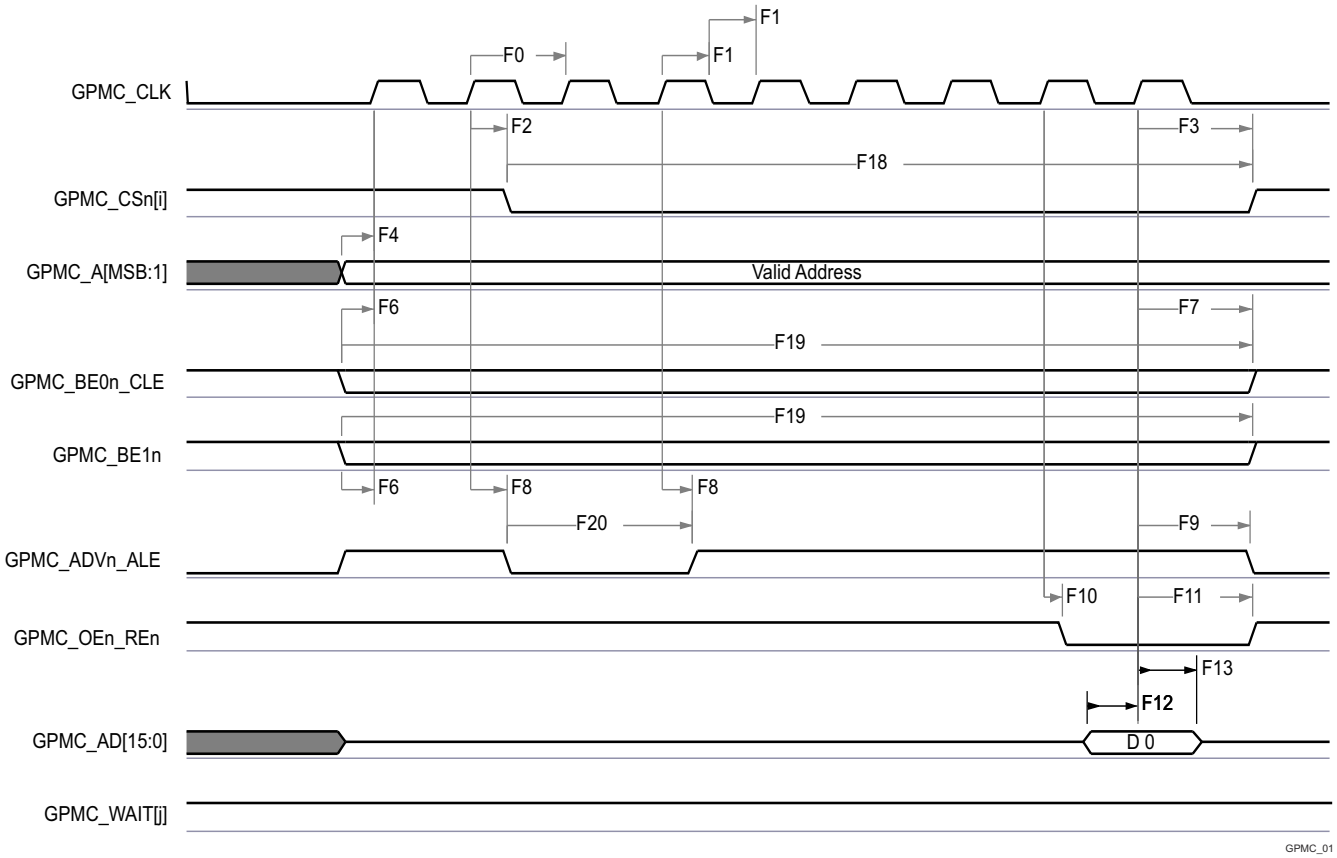
(17) For read: K = (ADVRdOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)
For write: K = (ADVWrOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(18)

(18) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.

(19) 100MHz GPMC_FCLK selected - CTRLMMR_GPMC_CLKSEL[0] CLK_SEL = 1 = MAIN_PLL2_HSDIV7_CLKOUT (100/60 MHz)

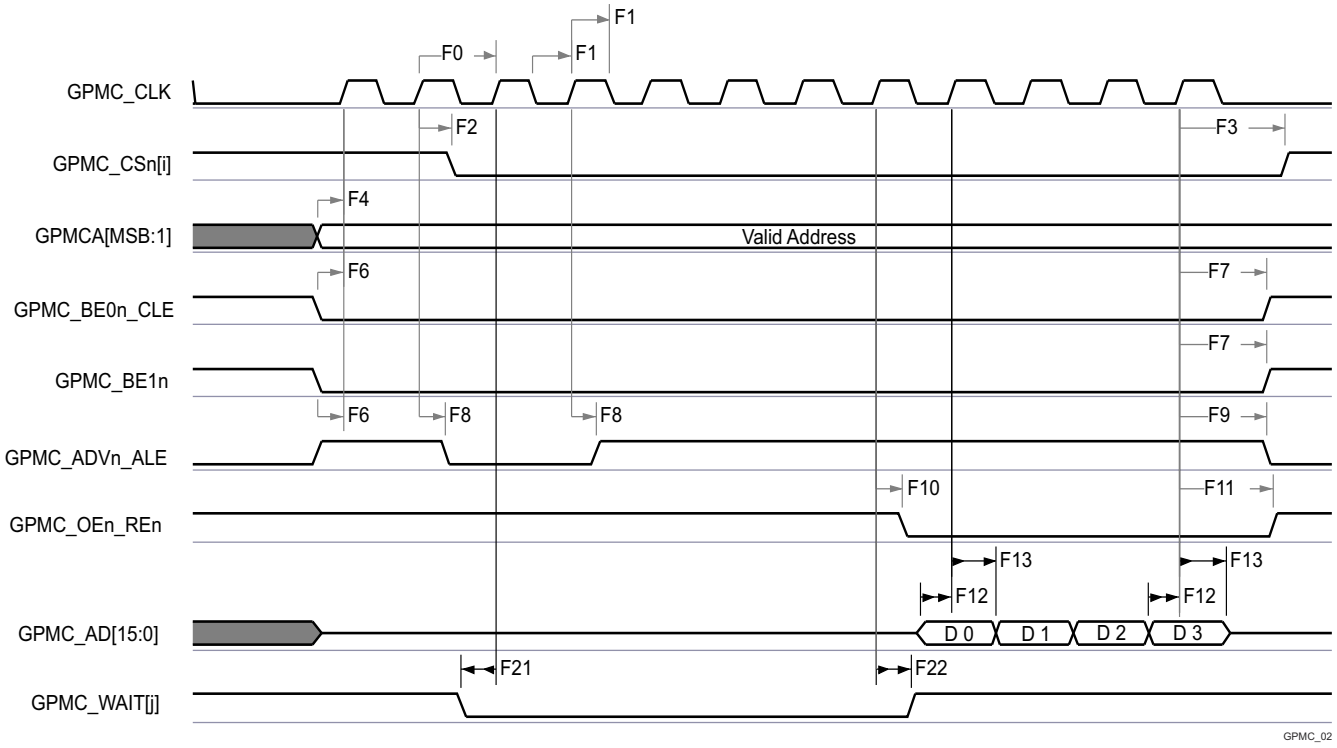
(20) Trace length from GPMC pins to device assumed to be less than 4" and length matched to within 200ps for 100MHz Synchronous Mode.

(21) In div_by_1_mode, GPMC0_CLK refers to either GPMC0_CLKOUT or GPMC0_FCLK_MUX (free-running). Both signals are pin-muxed to the same pin
– GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
– GPMC0_CLK frequency = GPMC_FCLK frequency
In not_div_by_1_mode, GPMC0_CLK only refers to GPMC0_CLKOUT. GPMC0_FCLK_MUX cannot be clock divided to match the GPMC0_CLKOUT frequency if GPMCFCLKDIVIDER > 0
– GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
– GPMC0_CLK frequency = GPMC_FCLK frequency / (2 to 4)



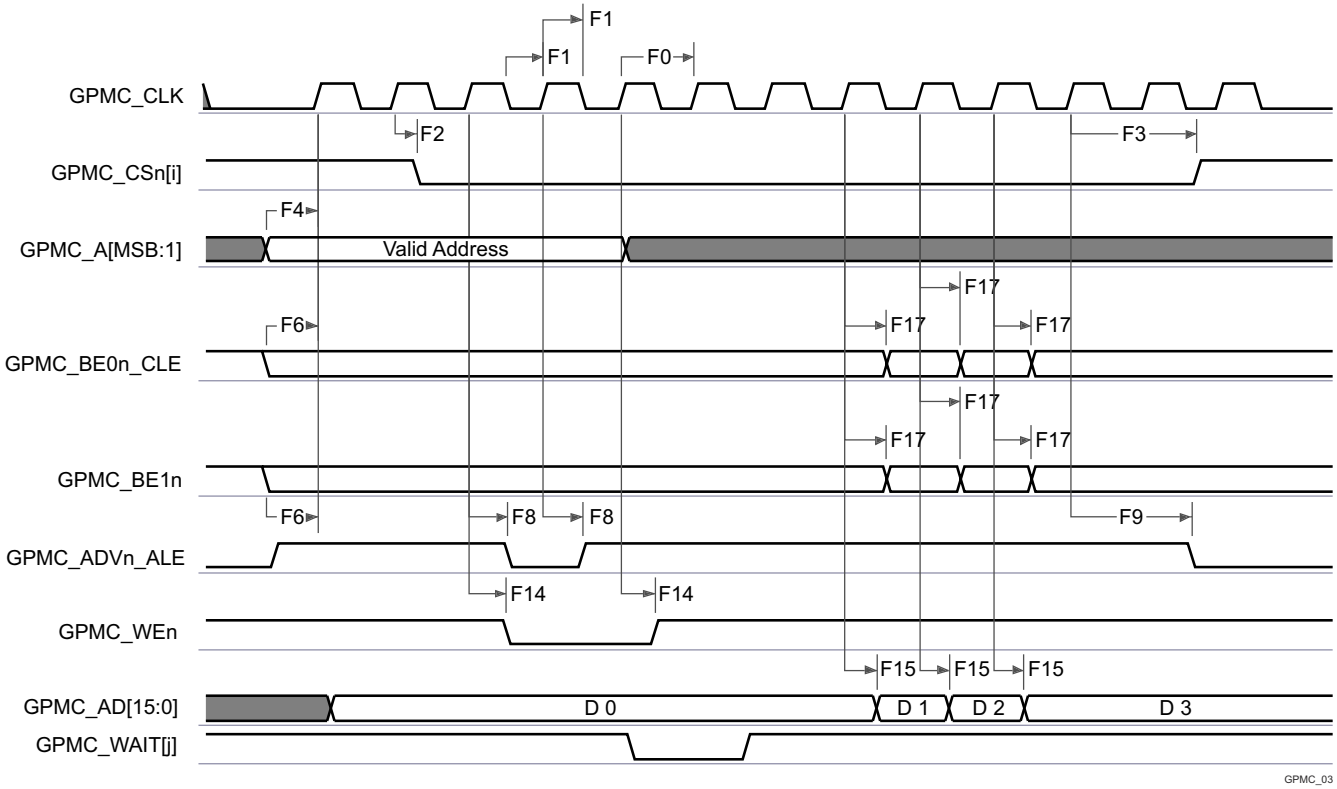
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-26. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

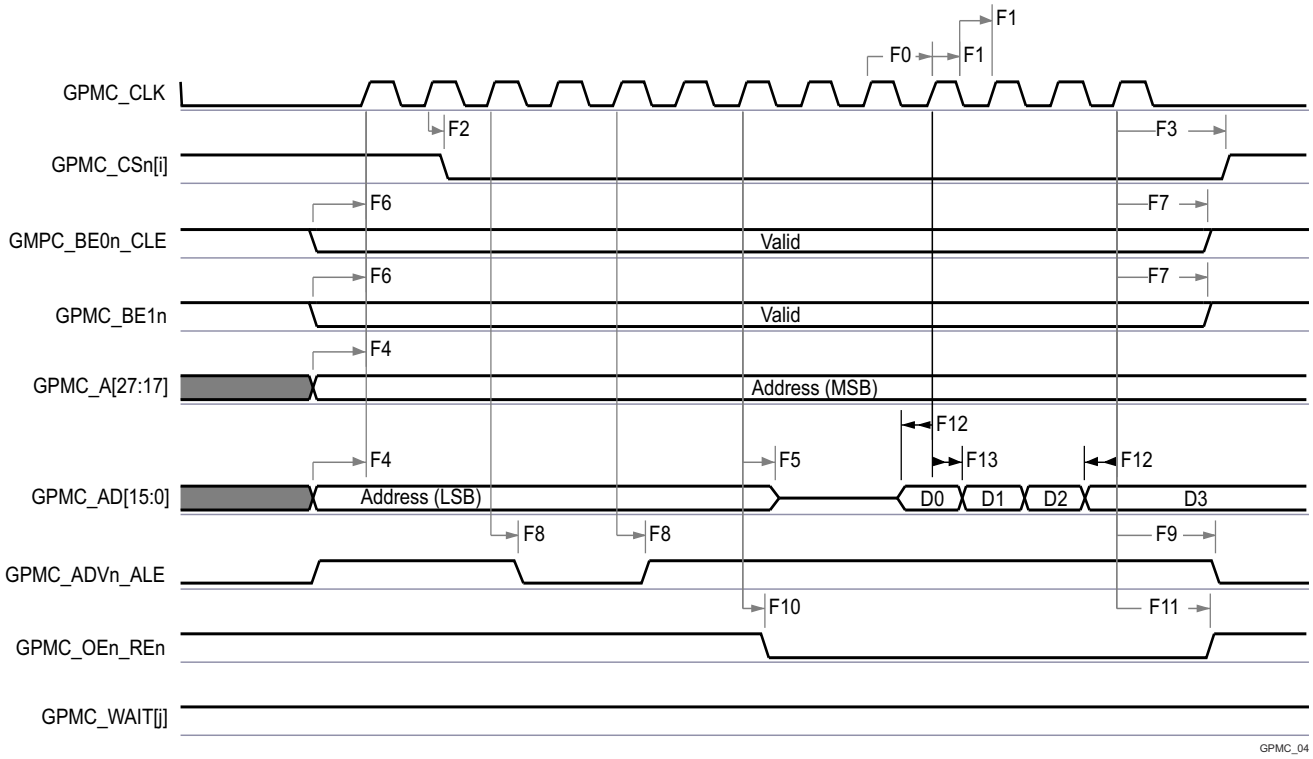
Figure 6-27. GPMC and NOR Flash — Synchronous Burst Read — 4x16–bit (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

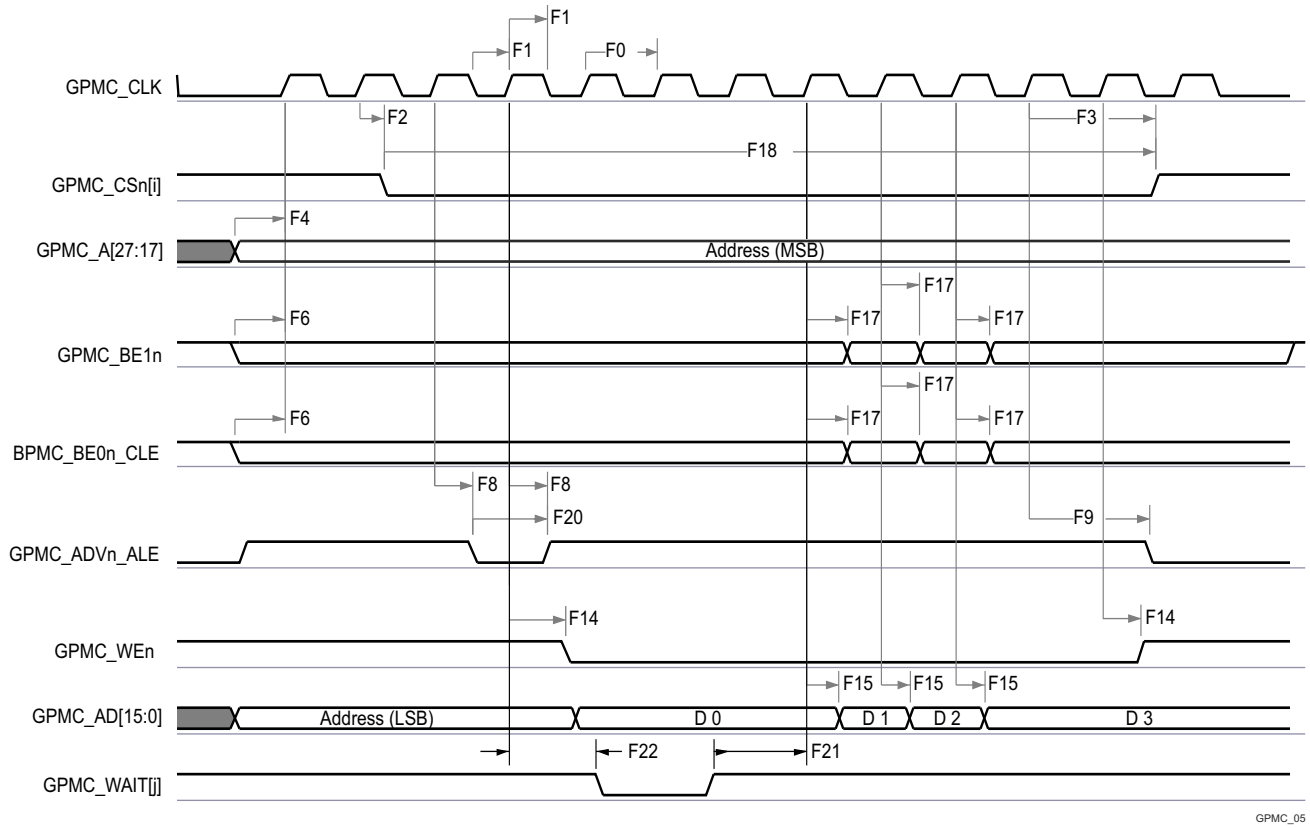
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-28. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-29. GPMC and Multiplexed NOR Flash — Synchronous Burst Read



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-30. GPMC and Multiplexed NOR Flash — Synchronous Burst Write

6.11.5.7.4 GPMC/NOR Flash Timing Requirements - Asynchronous Mode 100MHz

(7)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
FA5(1)	$t_{acc(d)}$	Data access time		H(5)	ns
FA20(2)	$t_{acc1\text{-}pgmode(d)}$	Page mode successive data access time		P(4)	ns
FA21(3)	$t_{acc2\text{-}pgmode(d)}$	Page mode first data access time		H(5)	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) The FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
(4) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(6)
(5) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(6)
(6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(7) 100MHz GPMC_FCLK selected - CTRLMMR_GPMC_CLKSEL[0] CLK_SEL = 1 = MAIN_PLL2_HSDIV7_CLKOUT (100/60 MHz)

6.11.5.7.5 GPMC/NOR Flash Switching Characteristics - Asynchronous Mode 100MHz

(14) (15)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
FA0	$t_{w(be[x]nV)}$	Pulse duration, GPMC0_BE0n_CLE, GPMC0_BE1n valid time	Read		N(12)	ns
			Write		N(12)	ns
FA1	$t_{w(csnV)}$	Pulse duration, GPMC0_CSn[x](13) low	Read		A(1)	ns
			Write		A(1)	ns
FA3	$t_{d(csnV-advnIV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_ADVn_ALE invalid	Read	B(2) – 2	B(2) + 2	ns
			Write	B(2) – 2	B(2) + 2	ns
FA4	$t_{d(csnV-oenIV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_OEn_REn invalid (Single read)		C(3) – 2	C(3) + 2	ns
FA9	$t_{d(aV-csnV)}$	Delay time, GPMC0_A[27:1] valid to GPMC0_CSn[x](13) valid		J(9) – 2	J(9) + 2	ns
FA10	$t_{d(be[x]nV-csnV)}$	Delay time, GPMC0_BE0n_CLE, GPMC0_BE1n valid to GPMC0_CSn[x](13) valid		J(9) – 2	J(9) + 2	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_ADVn_ALE valid		K(10) – 2	K(10) + 2	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_OEn_REn valid		L(11) – 2	L(11) + 2	ns
FA16	$t_{w(aIV)}$	Pulse duration GPMC0_A[26:1] invalid between two successive read and write accesses		G(7)		ns
FA18	$t_{d(csnV-oenIV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_OEn_REn invalid (Burst read)		I(8) – 2	I(8) + 2	ns
FA20	$t_{w(av)}$	Pulse duration, GPMC0_A[27:1] valid - 2nd, 3rd, and 4th accesses		D(4)		ns
FA25	$t_{d(csnV-wenIV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_WEn valid		E(5) – 2	E(5) + 2	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_WEn invalid		F(6) – 2	F(6) + 2	ns
FA28	$t_{d(wenV-dV)}$	Delay time, GPMC0_WEn valid to GPMC0_AD[31:0] valid			2	ns
FA29	$t_{d(dV-csnV)}$	Delay time, GPMC0_AD[31:0] valid to GPMC0_CSn[x](13) valid		J(9) – 2	J(10) + 2	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, GPMC0_OEn_REn valid to GPMC0_AD[31:0] phase end			2	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
with n being the page burst access number

(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(7) G = Cycle2CycleDelay × GPMC_FCLK(14)

(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK(14)

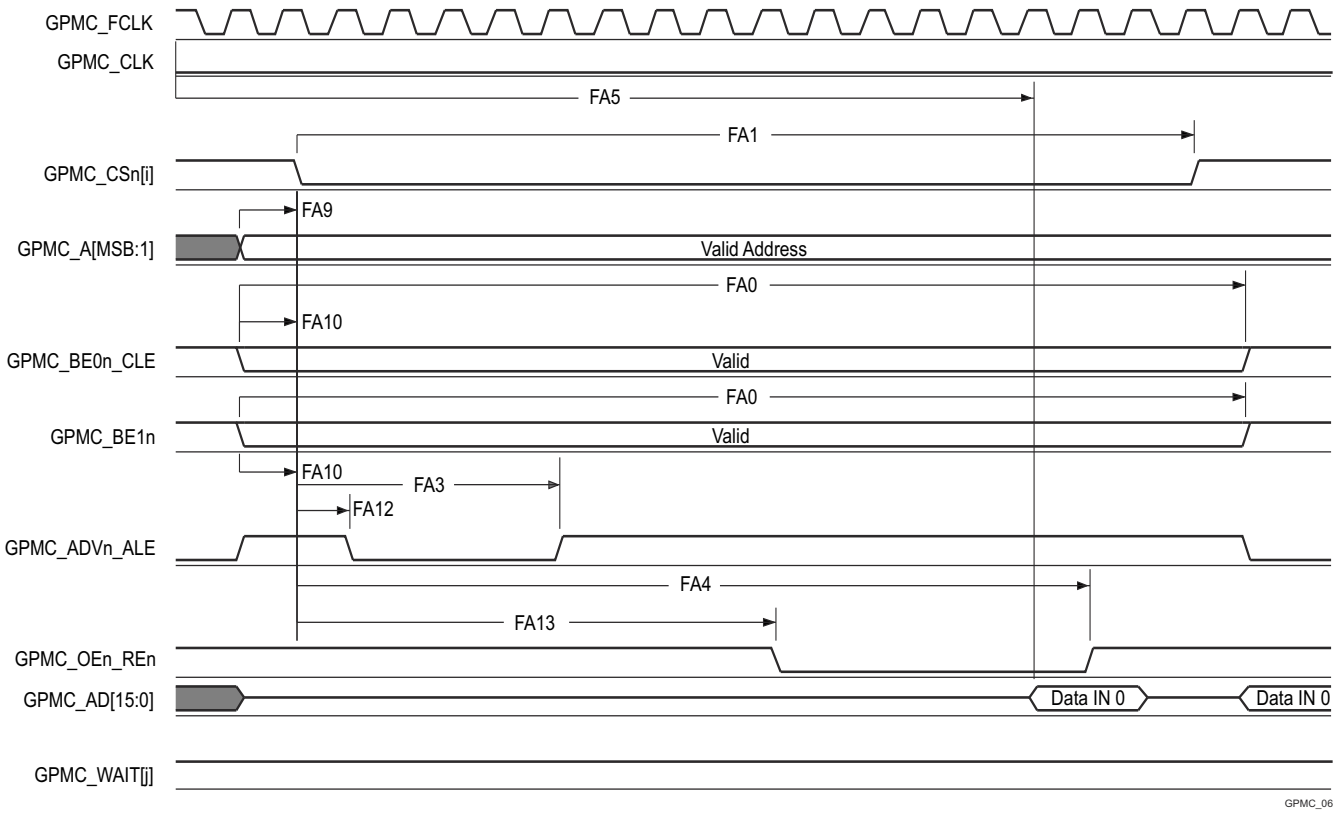
(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)

(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK((14)
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)

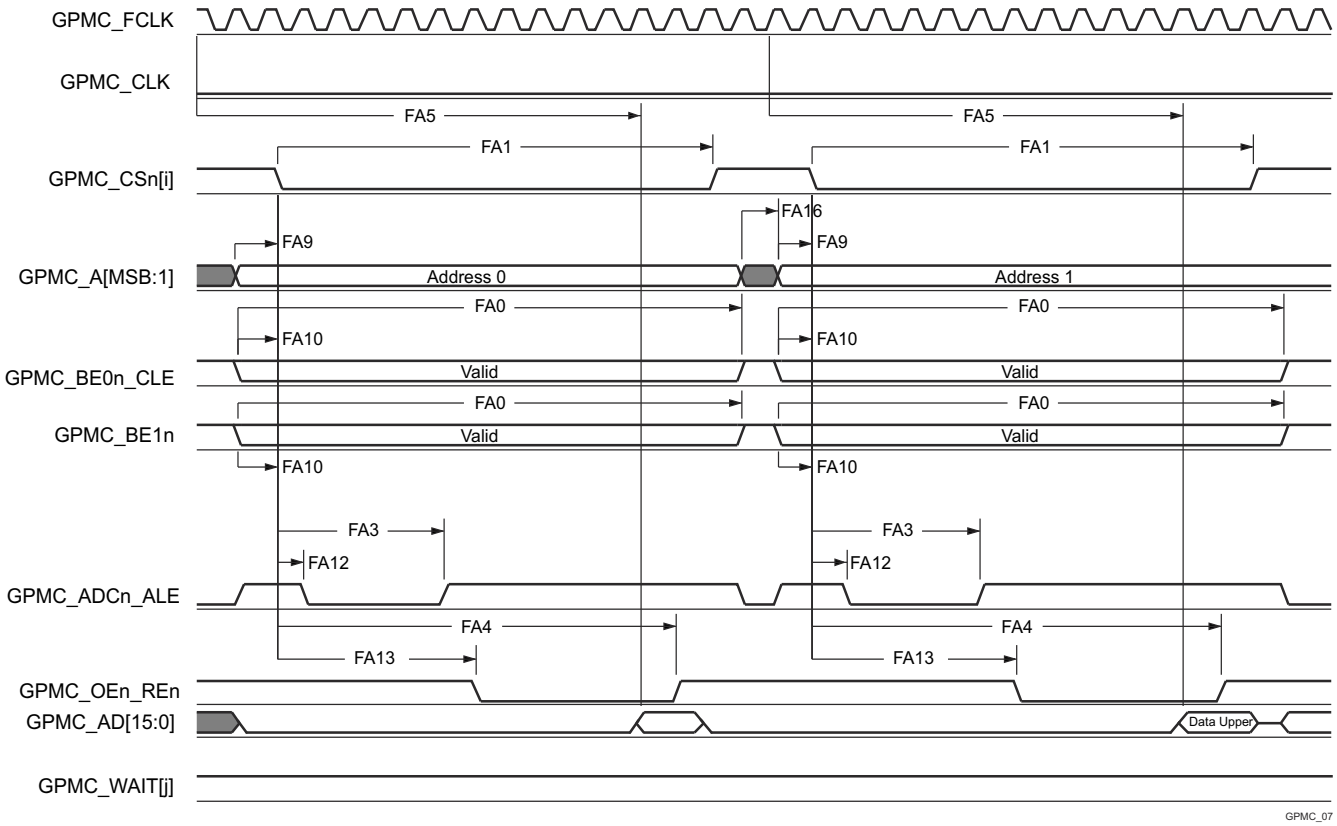
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)

(13) In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) 100MHz GPMC_FCLK selected - CTRLMMR_GPMC_CLKSEL[0] CLK_SEL = 1 = MAIN_PLL2_HSDIV7_CLKOUT (100/60 MHz)



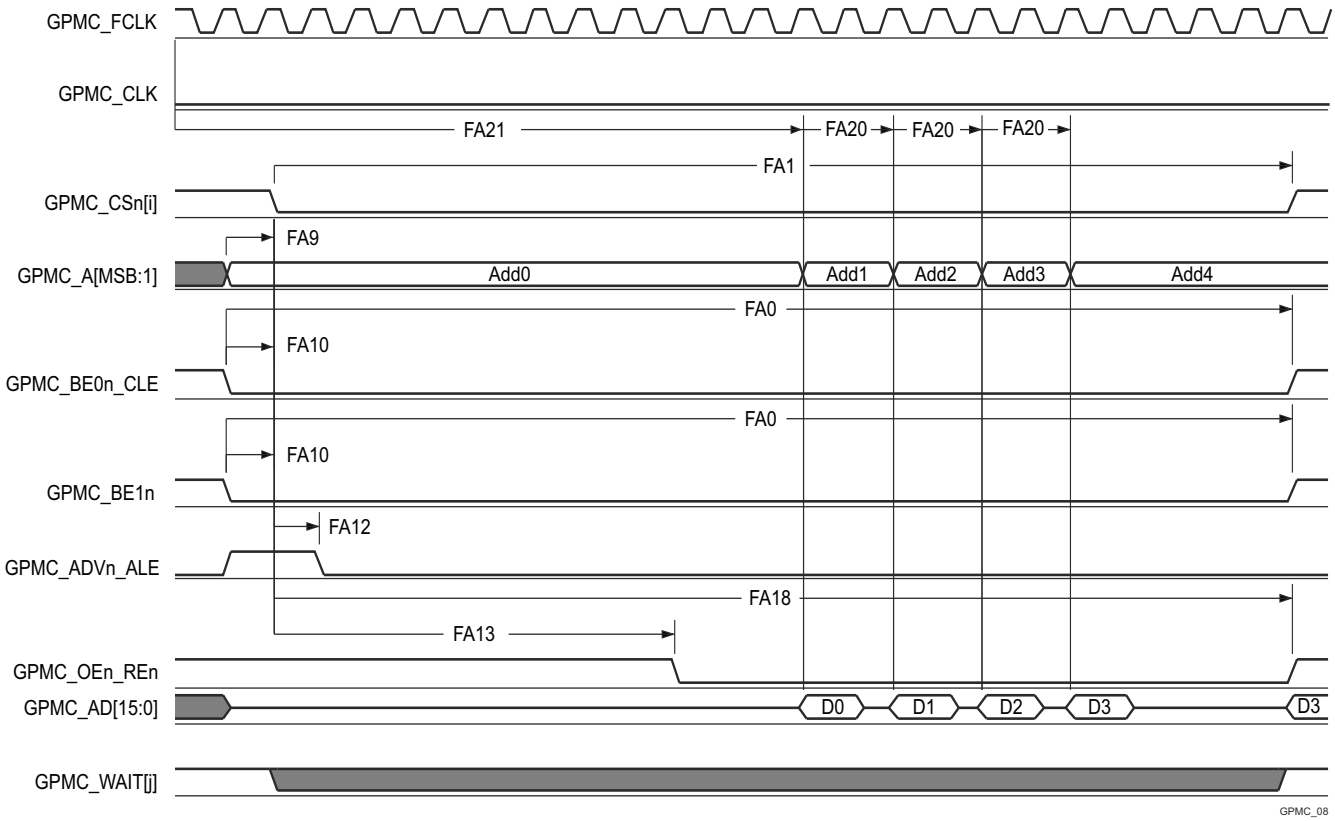
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-31. GPMC and NOR Flash — Asynchronous Read — Single Word



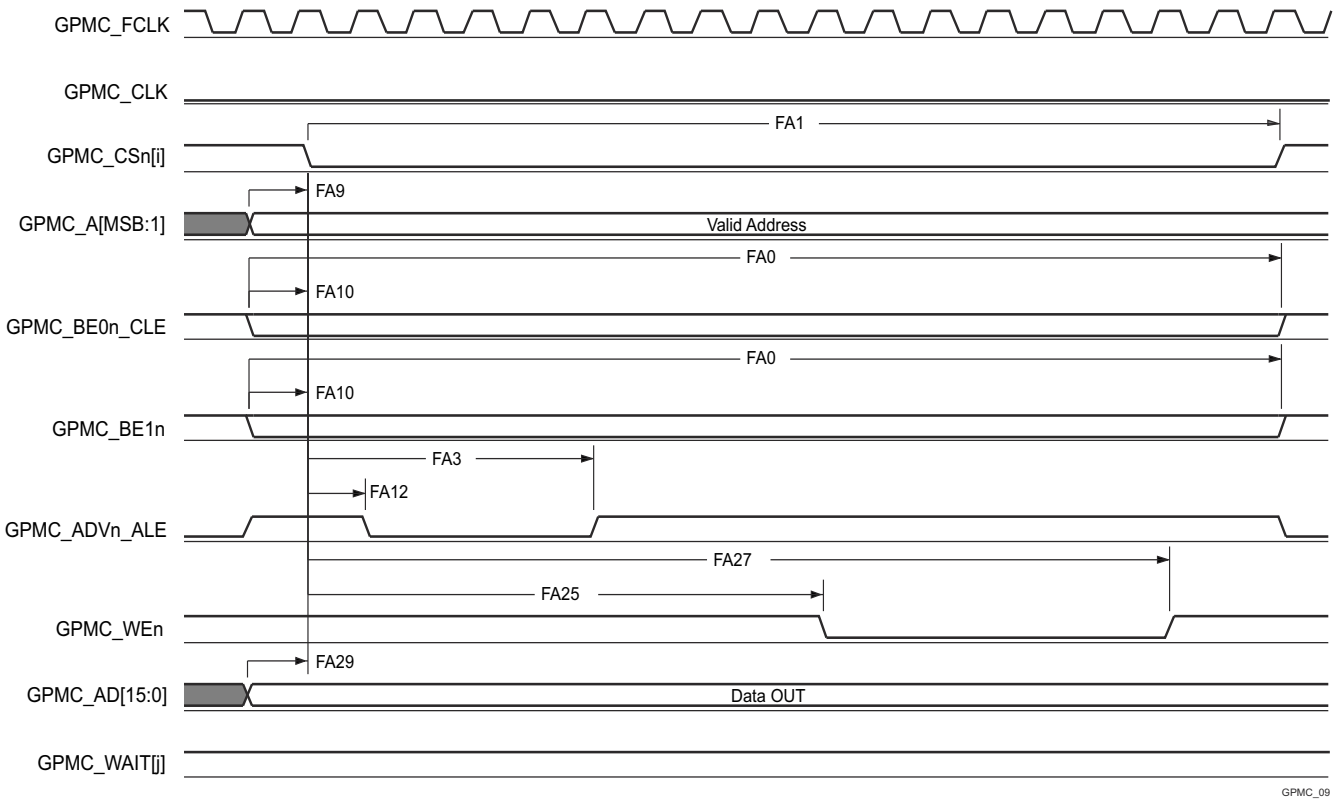
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-32. GPMC and NOR Flash — Asynchronous Read — 32–Bit



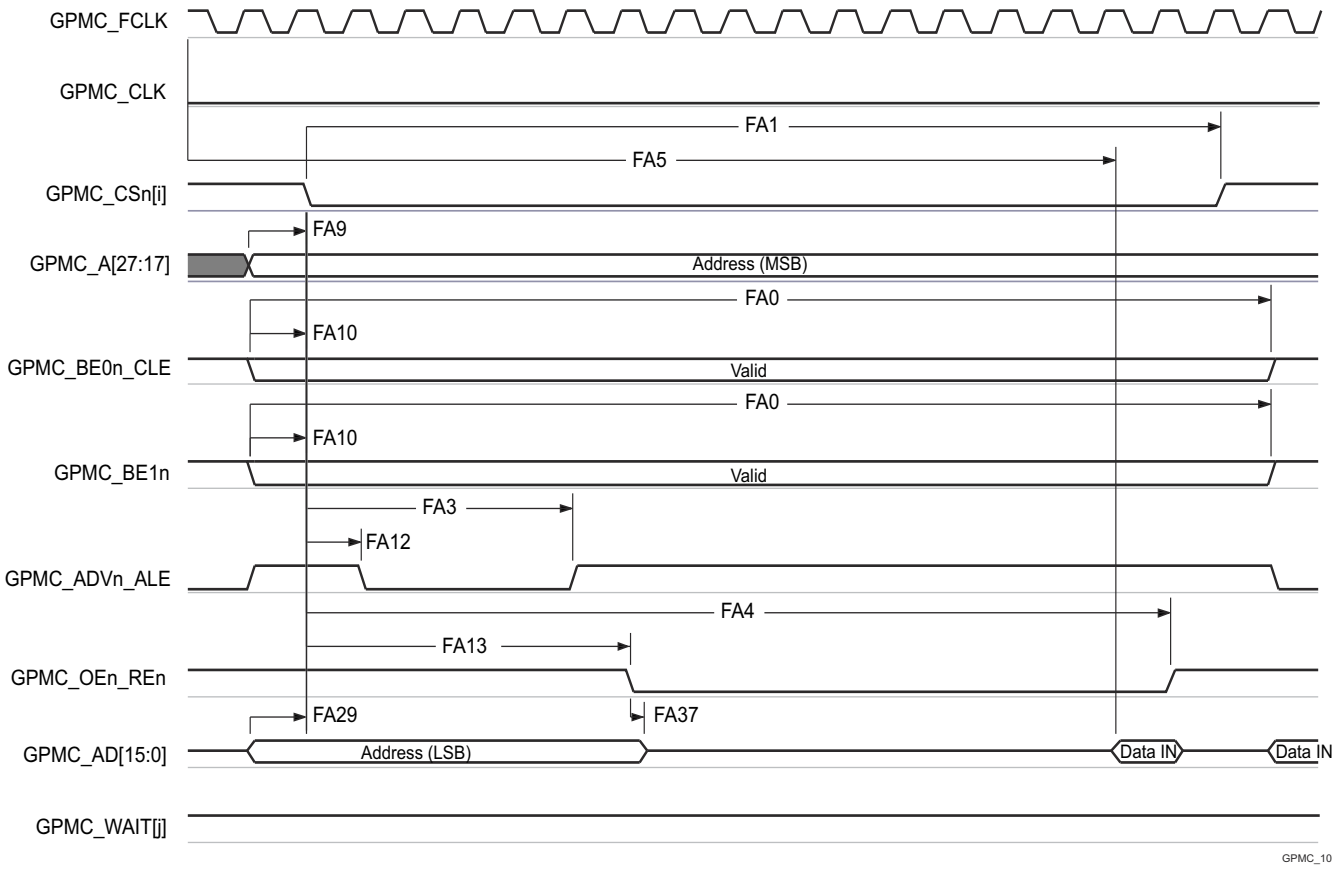
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.
C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.
D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-33. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit



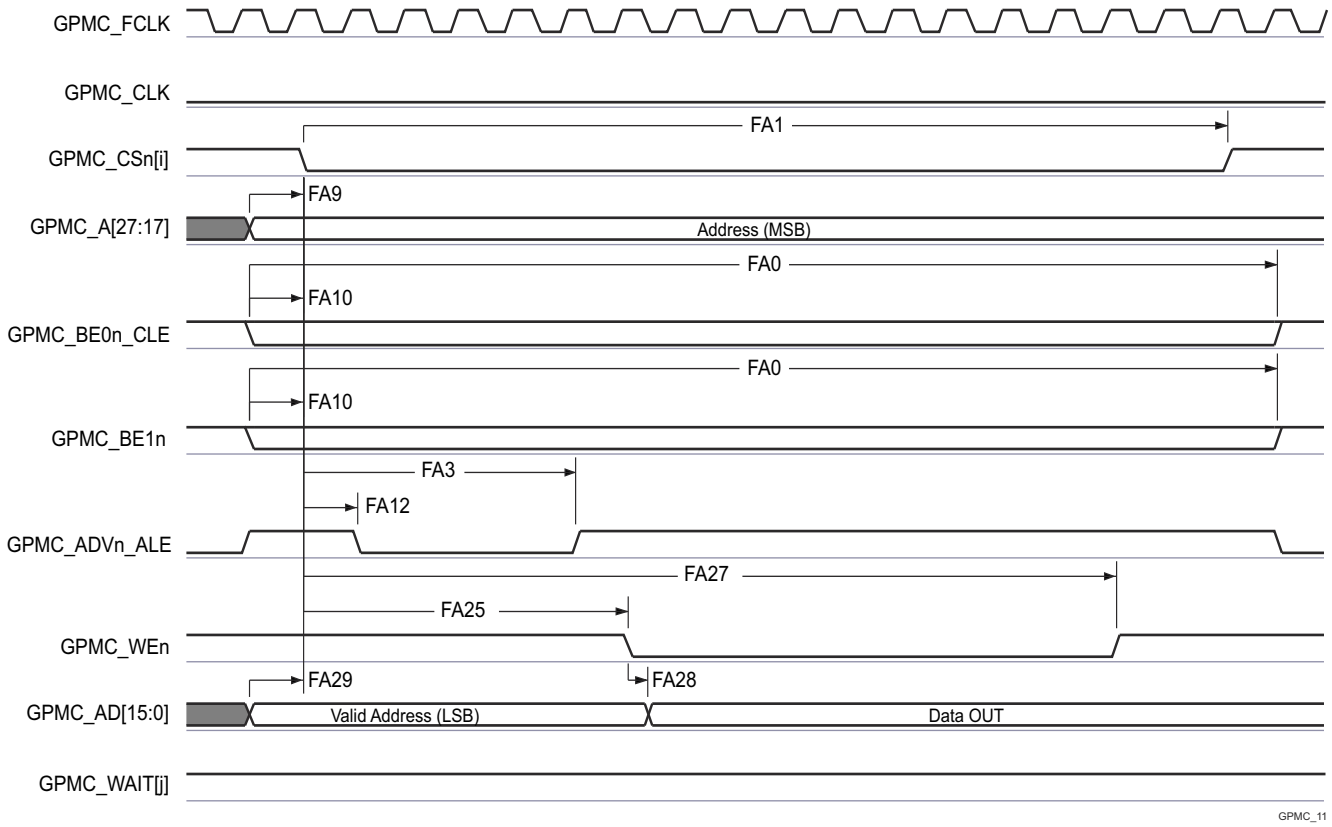
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-34. GPMC and NOR Flash — Asynchronous Write — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

Figure 6-35. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-36. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

6.11.5.7.6 GPMC/NAND Flash Timing Requirements - Asynchronous Mode 100MHz

(4)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GNF12(1)	$t_{acc(d)}$	Access time, GPMC0_AD[31:0](3)		J(2)	ns

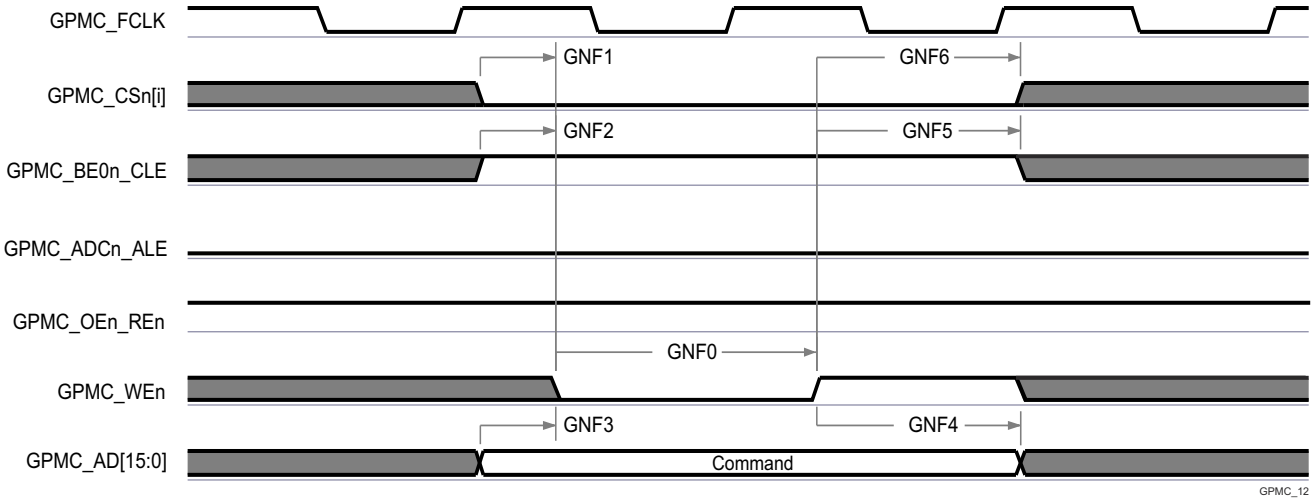
(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK(3)
(3) GPMC_FCLK is general-purpose memory controller internal functional clock.
(4) 100MHz GPMC_FCLK selected - CTRLMMR_GPMC_CLKSEL[0] CLK_SEL = 1 = MAIN_PLL2_HSDIV7_CLKOUT (100/60 MHz)

6.11.5.7.7 GPMC/NAND Flash Switching Characteristics - Asynchronous Mode 100MHz

(15)

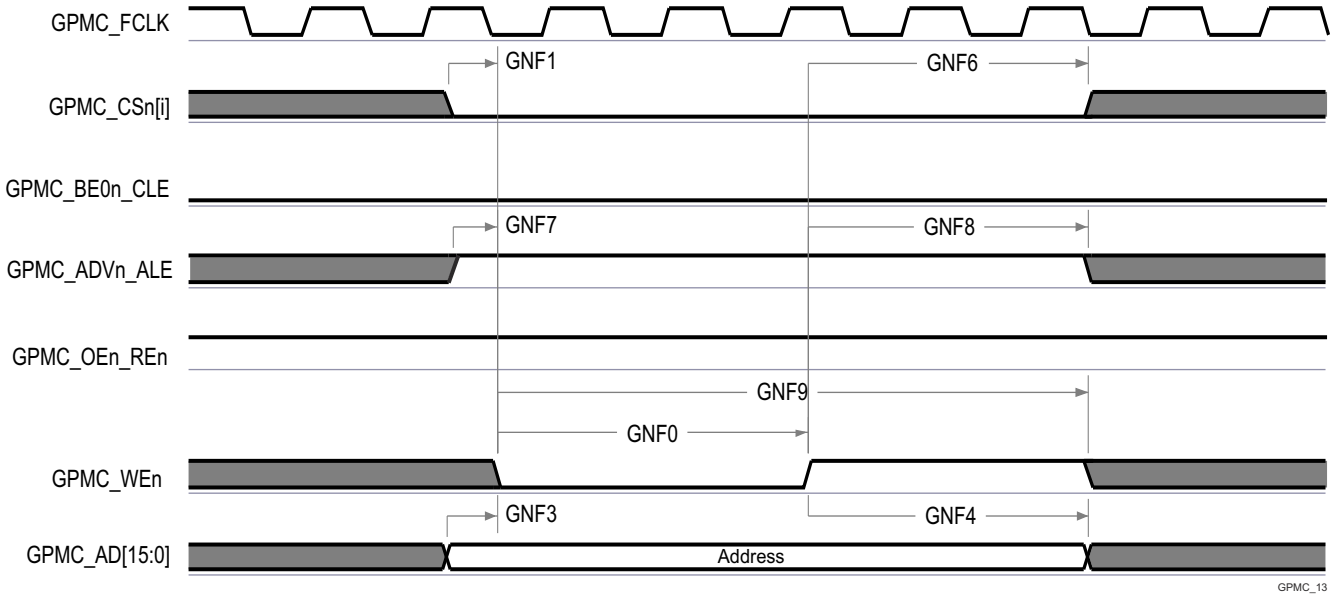
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GNF0	$t_{w(wenV)}$	Pulse duration, GPMC0_WEn valid	A(1)		ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_WEn valid	B(2) – 2	B(2) + 2	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, GPMC0_BE0n_CLE high to GPMC0_WEn valid	C(3) – 2	C(3) + 2	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, GPMC0_AD[31:0] valid to GPMC0_WEn valid	D(4) – 2	D(4) + 2	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, GPMC0_WEn invalid to GPMC0_AD[31:0] invalid	E(5) – 2	E(5) + 2	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, GPMC0_WEn invalid to GPMC0_BE0n_CLE invalid	F(6) – 2	F(6) + 2	ns
GNF6	$t_{w(wenIV-csnIV)}$	Delay time, GPMC0_WEn invalid to GPMC0_CSn[x](13) invalid	G(7) – 2	G(7) + 2	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, GPMC0_ADVn_ALE high to GPMC0_WEn valid	C(3) – 2	C(3) + 2	ns
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, GPMC0_WEn invalid to GPMC0_ADVn_ALE invalid	F(6) – 2	F(6) + 2	ns
GNF9	$t_{c(wen)}$	Cycle time, write		H(8)	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, GPMC0_CSn[x](13) valid to GPMC0_OEn_REn valid	I(9) – 2	I(9) + 2	ns
GNF13	$t_{w(oenV)}$	Pulse duration, GPMC0_OEn_REn valid		K(10)	ns
GNF14	$t_{c(oen)}$	Cycle time, read	L(11)		ns
GNF15	$t_{w(oenIV-csnIV)}$	Delay time, GPMC0_OEn_REn invalid to GPMC0_CSn[x](13) invalid	M(12) – 2	M(12) + 2	ns

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
(2) B = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(3) C = ((WEOnTime - ADVOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - ADVExtraDelay)) × GPMC_FCLK(14)
(4) D = (WEOnTime × (TimeParaGranularity + 1) + 0.5 × WEExtraDelay) × GPMC_FCLK(14)
(5) E = ((WrCycleTime - WEOffTime) × (TimeParaGranularity + 1) - 0.5 × WEExtraDelay) × GPMC_FCLK(14)
(6) F = ((ADVWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - WEExtraDelay)) × GPMC_FCLK(14)
(7) G = ((CSWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - WEExtraDelay)) × GPMC_FCLK(14)
(8) H = WrCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK(14)
(9) I = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(10) K = (OEOffTime - OEOnTime) × (1 + TimeParaGranularity) × GPMC_FCLK(14)
(11) L = RdCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK(14)
(12) M = ((CSRdOffTime - OEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - OEExtraDelay)) × GPMC_FCLK(14)
(13) In GPMC_CSn[x], x is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) 100MHz GPMC_FCLK selected - CTRLMMR_GPMC_CLKSEL[0] CLK_SEL = 1 = MAIN_PLL2_HSDIV7_CLKOUT (100/60 MHz)



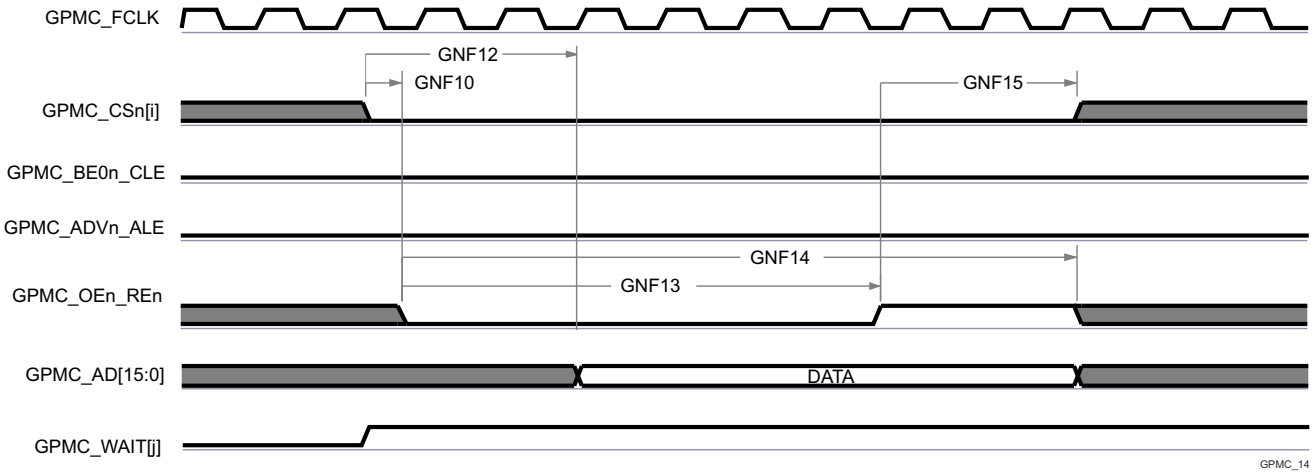
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-37. GPMC and NAND Flash — Command Latch Cycle



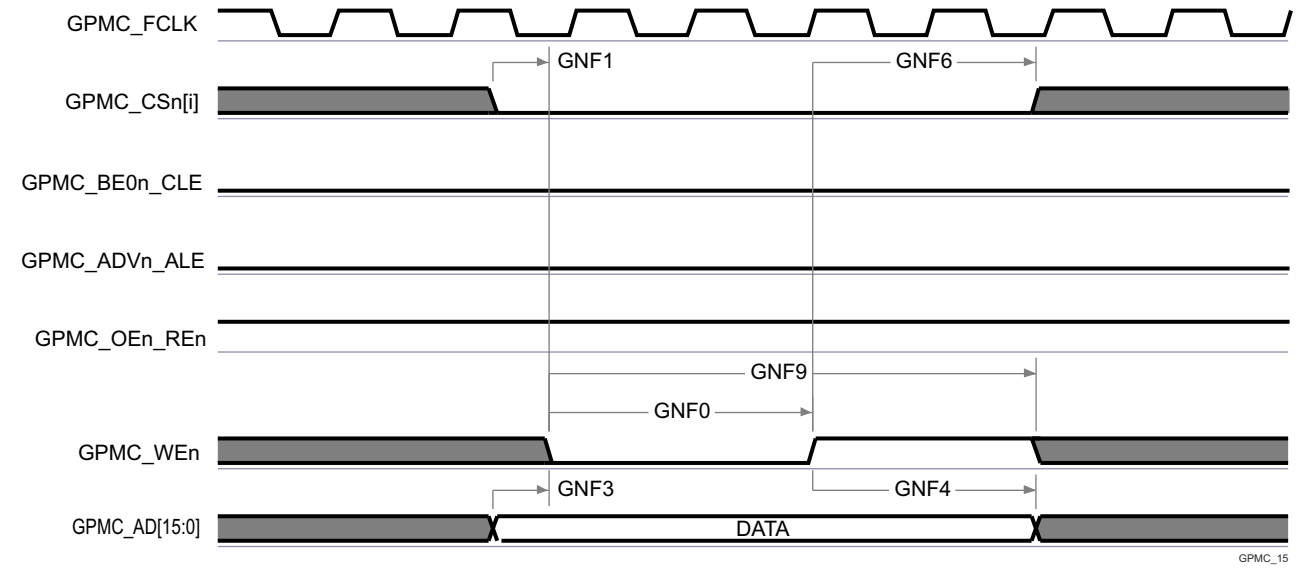
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-38. GPMC and NAND Flash — Address Latch Cycle



A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0 or 1.

Figure 6-39. GPMC and NAND Flash — Data Read Cycle



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

Figure 6-40. GPMC and NAND Flash — Data Write Cycle

6.11.5.8 Inter-Integrated Circuit (I^2C)

For more information, see the *Inter-Integrated Circuit (I2C)* section in the device TRM.

6.11.5.8.1 I2C

The device contains three multicontroller Inter-Integrated Circuit (I2C) controllers. Each I2C controller was designed to be compliant to the Philips I^{2}C-bus™ specification version 2.1. However, the device IOs are not fully compliant to the I2C electrical specification. The speeds supported and exceptions are described per port below:

- I2C1 and I2C2
  - Speeds:
    - Standard-mode (up to 100kbits/s)
      - 3.3V
    - Fast-mode (up to 400kbits/s)
      - 3.3V
  - Exceptions:
    - The IOs associated with these ports are not compliant to the fall time requirements defined in the I2C specification because they are implemented with higher performance LVCMOS push-pull IOs that were designed to support other signal functions that could not be implemented with I2C compatible IOs. The LVCMOS IOs being used on these ports are connected such they emulate open-drain outputs. This emulation is achieved by forcing a constant low output and disabling the output buffer to enter the Hi-Z state.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this data sheet.
- I2C0
  - Speeds:
    - Standard-mode (up to 100kbits/s)
      - 3.3V
    - Fast-mode (up to 400kbits/s)
      - 3.3V
  - Exceptions:
    - The IOs associated with this port were not design to support HS-mode.
    - The rise and fall times of the I2C signals connected to these ports must not exceed a slew rate of 0.8V/ns (or 8E+7V/s). This limit is more restrictive than the minimum fall time limits defined in the I2C specification. Therefore, it may be necessary to add additional capacitance to the I2C signals to slow the rise and fall times such that they do not exceed a slew rate of 0.8V/ns.
    - The I2C specification defines a maximum input voltage V_{IH} of ($V_{DD_{max}}$ + 0.5V), which exceeds the absolute maximum ratings for the device IOs. The system must be designed to ensure the I2C signals never exceed the limits defined in the *Absolute Maximum Ratings* section of this data sheet.

Refer to the Philips I2C-bus specification version 2.1 for timing details.

6.11.5.9 Local Interconnect Network (LIN)

Note

The device has multiple LIN modules. LINn is a generic prefix applied to LIN signal names, where n represents the specific LIN module.

For more information, see the *Local Interconnect Network (LIN) Module* section in the device TRM.

6.11.5.9.1 LIN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	20	pF

6.11.5.9.2 LIN Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LIN2	$t_{d(LINn\_RX)}$	Delay time, LINn_RX shift register to LINn_RX pin		10	ns

6.11.5.9.3 LIN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LIN4	$t_{d(LINn\_TX)}$	Delay time, LINn_TX shift register to LINn_TX pin		10	ns

6.11.5.10 Modular Controller Area Network (MCAN)

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

For more information, see *Controller Area Network (MCAN)* section in the device TRM.

6.11.5.10.1 MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	20	pF

6.11.5.10.2 MCAN Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
M1	$t_{d(MCAN\_TX)}$	Delay time, transmit shift register to MCAN_TX pin		10	ns
M2	$t_{d(MCAN\_RX)}$	Delay time, MCAN_RX pin to receive shift register		10	ns

6.11.5.11 Serial Peripheral Interface (SPI)

For more details about features and additional description information on the device Serial Port Interface, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

Note

The device has multiple SPI modules. The generic SPI_ prefix is used to represent the signal names for all SPI instances.

For more information, see the *Serial Peripheral Interface (SPI)* section in the device TRM.

6.11.5.11.1 SPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	2	8.5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	24	pF

6.11.5.11.2 SPI Controller Mode Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Normal Mode					
SM4	$t_{su(MISO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_SCLK active edge	2		ns
SM5	$t_{h(SPICLK-MISO)}$	Hold time, SPI_D[x] valid after SPI_SCLK active edge	3		ns

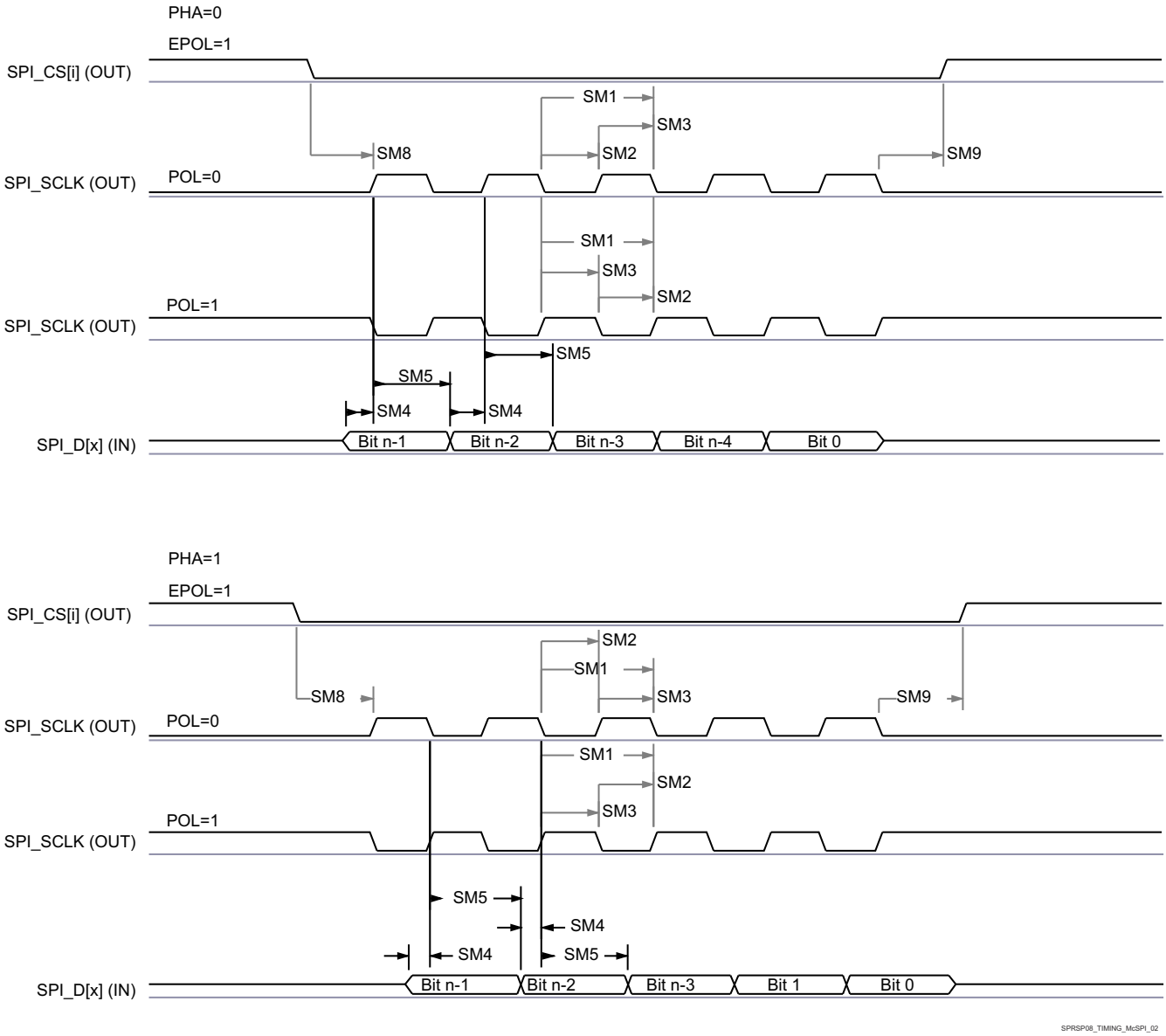


Figure 6-41. SPI Controller Mode Receive Timing

6.11.5.11.3 SPI Controller Mode Switching Characteristics (Clock Phase = 0)

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
Normal Mode						
SM1	$t_{c(SPICLK)}$	Cycle time, SPI_SCLK		20		ns
SM2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_SCLK low		–1 + 0.5P[1]		ns
SM3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_SCLK high		–1 + 0.5P[1]		ns
SM6	$t_{d(SPICLK-SIMO)}$	Delay time, SPI_SCLK active edge to SPI_D[x] transition		–3	2	ns
SM7	$t_{sk(CS-SIMO)}$	Delay time, SPI_CS[i] active to SPI_D[x] transition		5		ns
SM8	$t_{d(SPICLK-CS)}$	Delay time, SPI_CS[i] active to SPI_SCLK first edge	PHA = 0	–4 + B[3]		ns
			PHA = 1	–4 + A[2]		ns

NO.	PARAMETER	DESCRIPTION		MIN	MAX	UNIT
SM9	$t_{d(SPICLK-CS)}$	Delay time, SPI_SCLK last edge to SPI_CS[i] inactive	PHA = 0	–4 + A(2)		ns
			PHA = 1	–4 + B(3)		ns

(1) P = SPICLK period in ns.
(2) When P = 20.8ns, A = (TCS + 1) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register. When P > 20.8ns, A = (TCS + 0.5) * Fratio * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register.
(3) B = (TCS + .5) * TSPICLKREF, where TCS is a bit field of the SPI_CH(i)CONF register and F_{ratio} = Even >= 2.

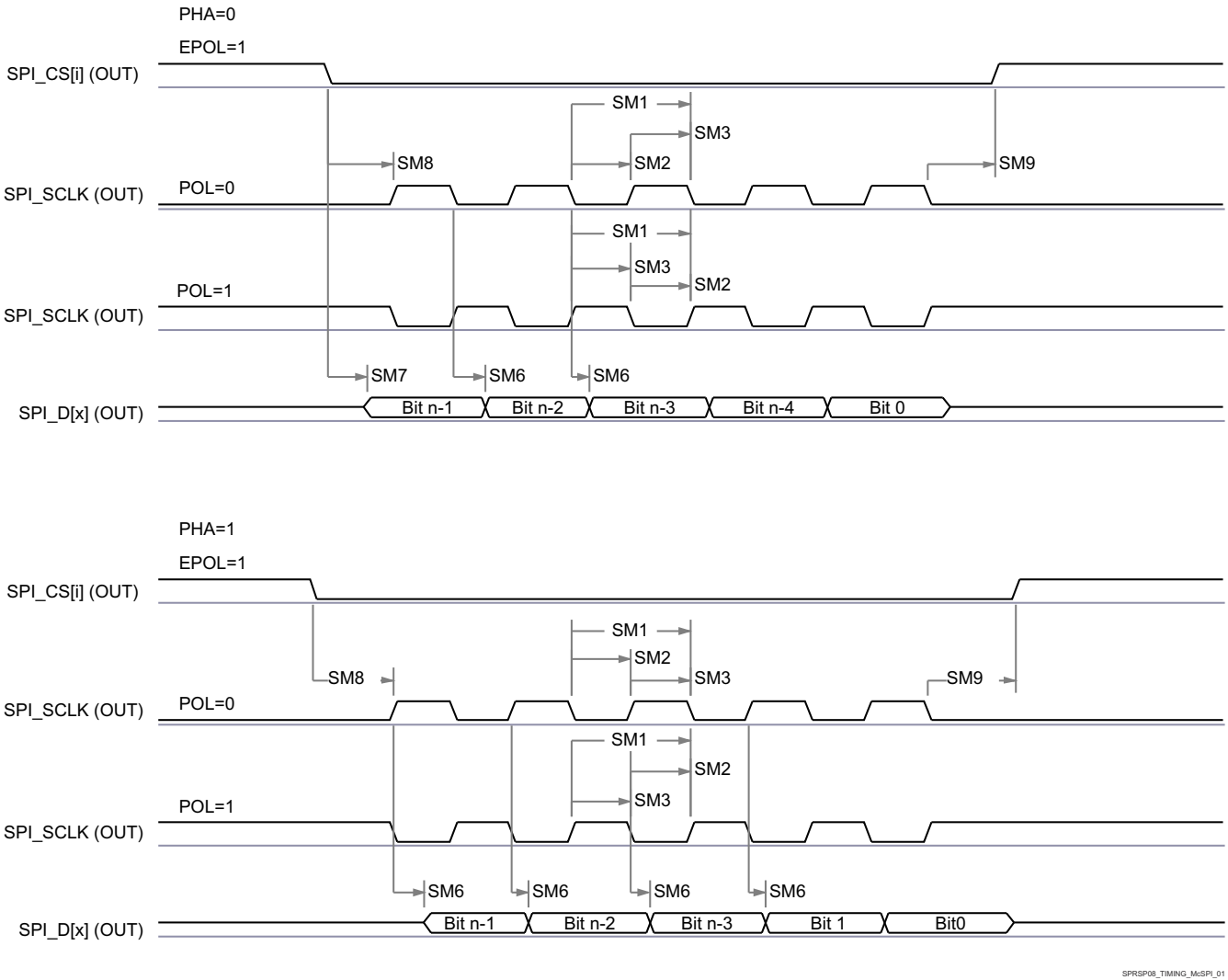


Figure 6-42. SPI Controller Mode Transmit Timing

6.11.5.11.4 SPI Peripheral Mode Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS1	$t_{c(SPICLK)}$	Cycle time, SPI_SCLK	40		ns
SS2	$t_{w(SPICLKL)}$	Typical Pulse duration, SPI_SCLK low	0.45 × P(1)		ns
SS3	$t_{w(SPICLKH)}$	Typical Pulse duration, SPI_SCLK high	0.45 × P(1)		ns
SS4	$t_{su(SIMO-SPICLK)}$	Setup time, SPI_D[x] valid before SPI_SCLK active edge	5		ns
SS5	th(SPICLK-SIMO)	Hold time, SPI_D[x] valid after SPI_SCLK active edge	5		ns

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS8	$t_{su(CS-SPICLK)}$	Setup time, SPI_CS[i] valid before SPI_SCLK first edge	5		ns
SS9	$t_{h(SPICLK-CS)}$	Hold time, SPI_CS[i] valid after SPI_SCLK last edge	5		ns

(1) P = SPICLK period.

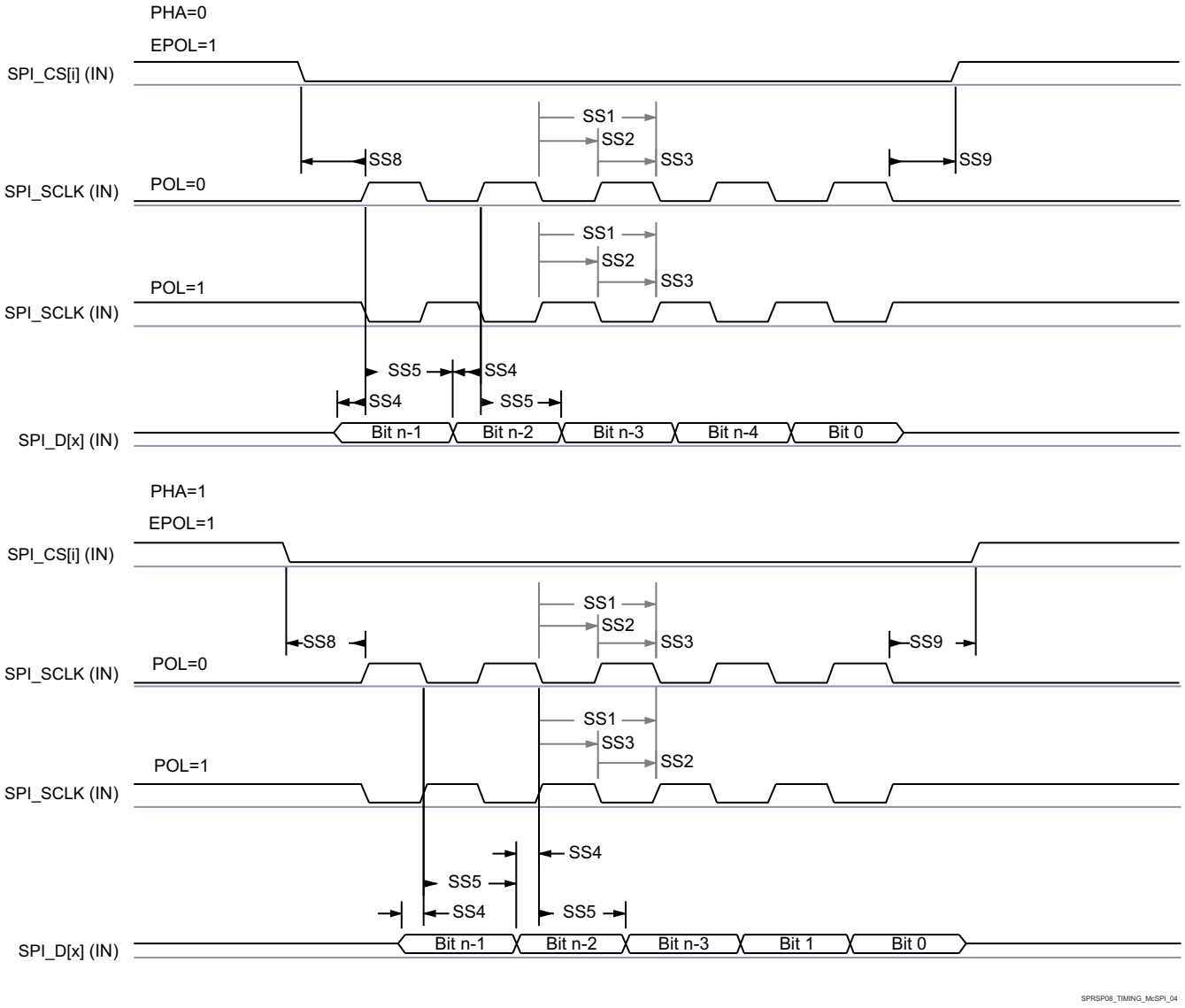


Figure 6-43. SPI Peripheral Mode Receive Timing

6.11.5.11.5 SPI Peripheral Mode Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Normal Mode					
SS6	$t_{d(SPICLK-SOMI)}$	Delay time, SPI_SCLK active edge to MCSPI_SOMI transition	2	17.12	ns
SS7	$t_{sk(CS-SOMI)}$	Delay time, SPI_CS[i] active edge to MCSPI_SOMI transition	20.95		ns

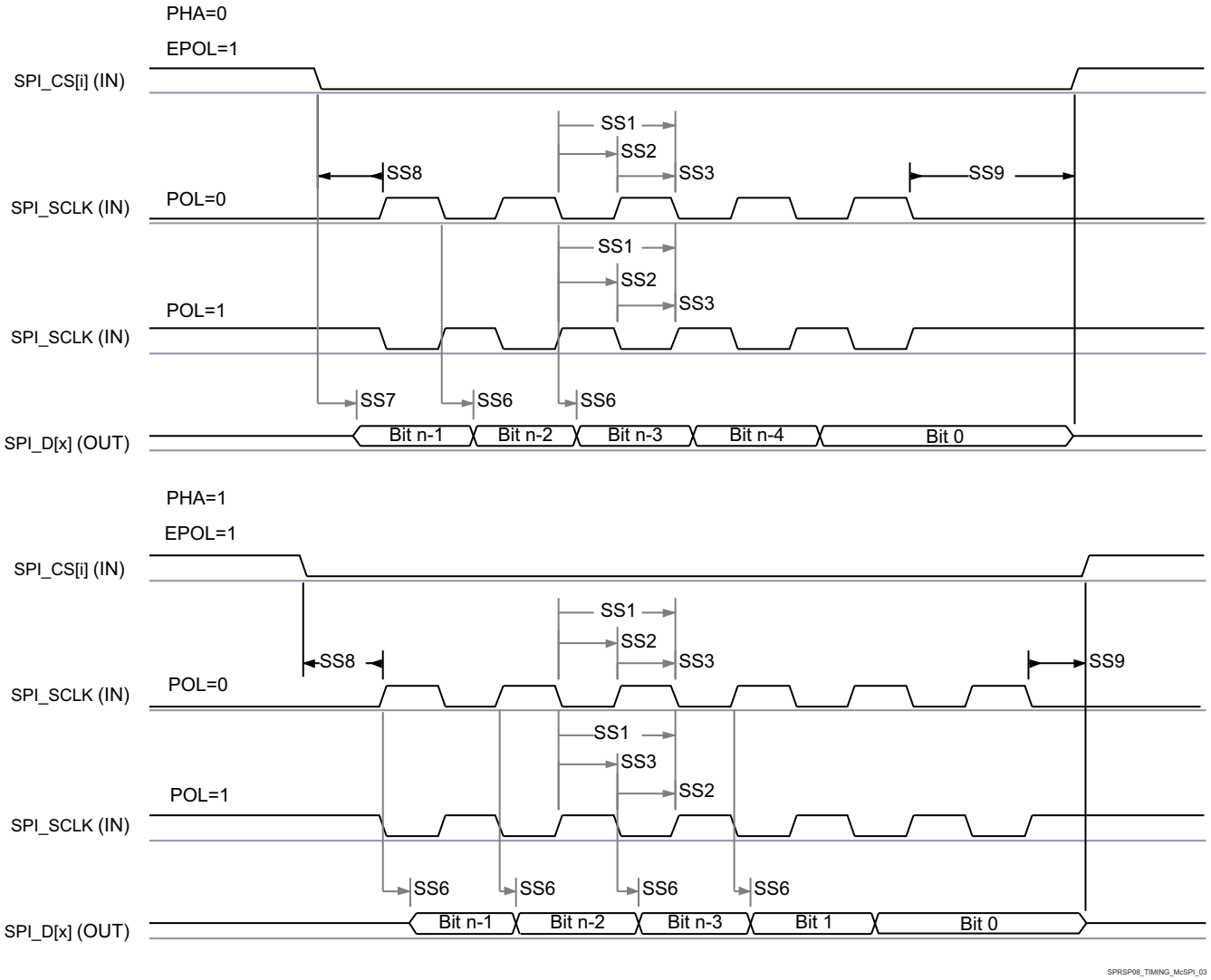


Figure 6-44. SPI Peripheral Mode Transmit Timing

6.11.5.12 Multi-Media Card/Secure Digital (MMCSD)

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC) and Secure Digital (SD)devices. The MMCSD Host Controller deals with MMC/SD protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

6.11.5.12.1 MMC Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	Default Speed	0.69	2.06	V/ns
		High Speed	0.69	2.06	V/ns
OUTPUT CONDITIONS					
C_L	Output Load Capacitance	Default Speed	1	10	pF
		High Speed	1	10	pF

6.11.5.12.2 MMC Timing Requirements - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMC_CMD valid before MMC_CLK rising edge	2.15		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMC_CMD valid after MMC_CLK rising edge	19.67		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMC_DAT[3:0] valid before MMC_CLK rising edge	2.15		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMC_DAT[3:0] valid after MMC_CLK rising edge	19.67		ns

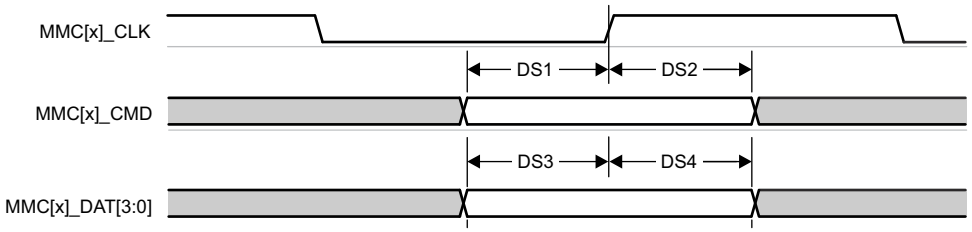


Figure 6-45. MMC – Default Speed – Receive Mode

6.11.5.12.3 MMC Switching Characteristics - SD Card Default Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		25	MHz
DS5	$t_{c(clk)}$	Operating period, MMC_CLK		40	ns
DS6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	–14.1	14.1	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition	–14.1	14.1	ns

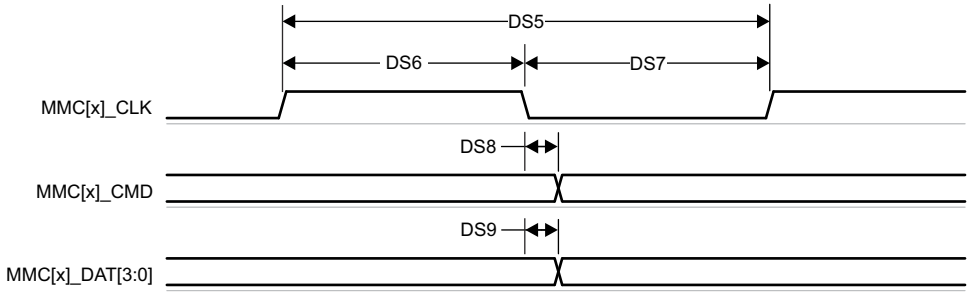


Figure 6-46. MMC – Default Speed – Transmit Mode

6.11.5.12.4 MMC Timing Requirements - SD Card High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMC_CMD valid before MMC_CLK rising edge	2.15		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMC_CMD valid after MMC_CLK rising edge	2.67		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMC_DAT[3:0] valid before MMC_CLK rising edge	2.15		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMC_DAT[3:0] valid after MMC_CLK rising edge	2.67		ns

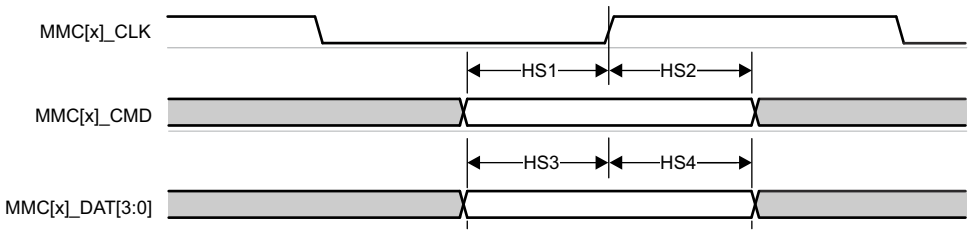


Figure 6-47. MMC – High Speed – Receive Mode

6.11.5.12.5 MMC Switching Characteristics - SD Card High Speed Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC_CLK		50	MHz
HS5	$t_{c(clk)}$	Operating period, MMC_CLK		20	ns
HS6	$t_{w(clkH)}$	Pulse duration, MMC_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMC_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMC_CLK falling edge to MMC_CMD transition	–7.35	3.35	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMC_CLK falling edge to MMC_DAT[3:0] transition	–7.35	3.35	ns

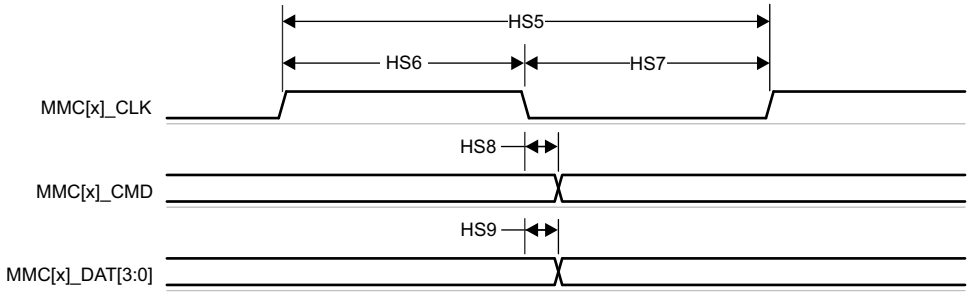


Figure 6-48. MMC – High Speed – Transmit Mode

6.11.5.13 Octal Serial Peripheral Interface (OSPI)

OSPI offers two data capture modes, PHY mode and Tap mode.

PHY mode uses an internal reference clock to transmit and receive data via a DLL based PHY, where each reference clock cycle produces a single cycle of OSPI_CLK for Single Data Rate (SDR) transfers or a half cycle of OSPI_CLK for Double Data Rate (DDR) transfers. PHY mode supports three clocking topologies for the receive data capture clock. Internal PHY Loopback - uses the internal reference clock as the PHY receive data capture clock. Internal Pad Loopback - uses OSPI_LBCLKO looped back into the PHY from the OSPI_LBCLKO pin as the PHY receive data capture clock. DQS - uses the DQS output from the attached device as the PHY receive data capture clock. SDR transfers are not supported when using the Internal Pad Loopback and DQS clocking topologies. DDR transfers are not supported when using the Internal PHY Loopback or Internal Pad Loopback clocking topologies.

Tap mode uses an internal reference clock with selectable taps to adjusted data transmit and receive capture delays relative to OSPI_CLK, which is a divide by 4 of the internal reference clock for SDR transfers or a divide by 8 of the internal reference clock for DDR transfers. Tap mode only supports one clocking topology for the receive data capture clock. No Loopback - uses the internal reference clock as the Tap receive data capture clock. This clocking topology supports a maximum internal reference clock rate of 200MHz, which produces an OSPI_CLK rate up to 50MHz for SDR mode or 25MHz for DDR mode.

OSPI PHY Mode defines timing requirements and switching characteristics associated with PHY mode and *OSPI Tap Mode* defines timing requirements and switching characteristics associated with Tap mode.

OSPI Timing Conditions presents timing conditions for OSPI.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in the device TRM.

6.11.5.13.1 OSPI Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2	6	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	15	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI_CLK trace(1)	No Loopback Internal PHY Loopback Internal Pad Loopback		450	ps
	Propagation delay of OSPI_DQS trace	DQS	L(2) - 30	L(2) + 30	ps
$t_{d(Trace\ Delay)}$	Propagation delay of OSPI_LBCLKO trace	External Board Loopback	2L(2) - 30	2L(2) + 30	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch of OSPI_D[7:0] and OSPI_CSn[1:0] relative to OSPI_CLK	All modes		60	ps

(1) Not applicable when using DQS clocking topology
(2) L = Propagation delay of OSPI_CLK trace

6.11.5.13.2 OSPI PHY Mode

6.11.5.13.2.1 OSPI With PHY Data Training

Read and write data valid windows will shift due to variation in process, voltage, temperature, and operating frequency. A data training method may be implemented to dynamically configure optimal read and write timing. Implementing data training enables proper operation across temperature with a specific process, voltage, and frequency operating condition, while achieving a higher operating frequency.

Data transmit and receive timing parameters are not defined for the data training use case since they are dynamically adjusted based on the operating condition.

6.11.5.13.2.1.1 OSPI DLL Delay Mapping for PHY Data Training

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	(1)
Receive		
All modes	PHY_CONFIG_RX_DLL_DELAY_FLD	(2)

(1) Transmit DLL delay value determined by training software
(2) Receive DLL delay value determined by training software

6.11.5.13.2.1.2 OSPI Timing Requirements - PHY Data Training

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_DQS edge	DDR with DQS	(1)		ns
O16	$t_{h(LBCLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_DQS edge	DDR with DQS	(1)		ns

(1) Minimum setup and hold time requirements for OSPI_D[7:0] inputs are not defined when Data Training is used to find the optimum data valid window.

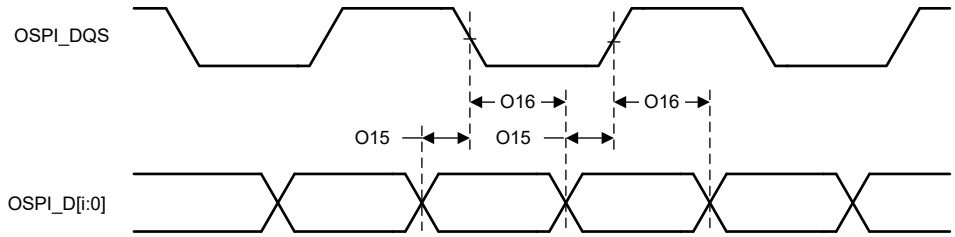


Figure 6-49. . OSPI Timing Requirements – PHY Data Training, DDR with DQS

6.11.5.13.2.1.3 OSPI Switching Characteristics - PHY Data Training

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI_CLK	1.8V, DDR	6.024		ns
			3.3V, DDR	7.52		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI_CLK low	DDR	0.475P(1) - 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI_CLK high	DDR	0.475P(1) - 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI_CSn[1:0] active edge to OSPI_CLK rising edge	DDR	0.475P(1) + (0.975 × M(2) × R(4)) + 0.35TD(5) - 1	0.525P(1) + (1.025 × M(2) × R(4)) + 0.95TD(5) + 1	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI_CLK rising edge to OSPI_CSn[1:0] inactive edge	DDR	0.475P(1) + (0.975 × N(3) × R(4)) - 0.35TD(5) - 1	0.525P(1) + (1.025 × N(3) × R(4)) - 0.95TD(5) + 1	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI_CLK active edge to OSPI_D[7:0] transition	DDR	(6)	(6)	ns

(1) P = OSPI_CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns
(5) TD = PHY_CONFIG_TX_DLL_DELAY_FLD

(6) Minimum and maximum delay times for OSPI_D[7:0] outputs are not defined when Data Training is used to find the optimum data valid window.

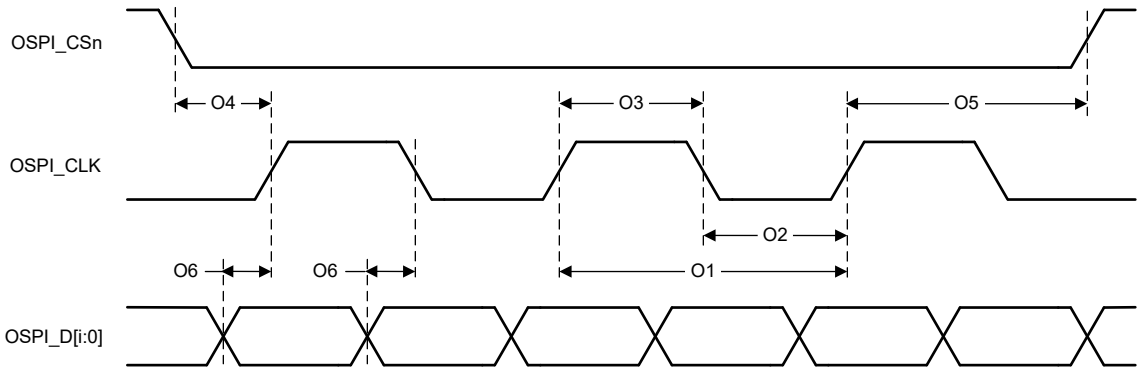


Figure 6-50. OSPI Switching Characteristics – PHY DDR Data Training

6.11.5.13.2.2 OSPI0 Without Data Training

Note

Timing parameters defined in this section are only applicable for the OSPI0 interface when data training is not implemented and DLL delays are configured as described in *OSPI0 DLL Delay Mapping for PHY SDR Timing Modes* and *OSPI0 DLL Delay Mapping for PHY DDR Timing Modes*.

6.11.5.13.2.2.1 OSPI0 PHY SDR Timing

6.11.5.13.2.2.1.1 OSPI0 DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x23
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x2F
Receive		
1.8V, Internal PHY Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x3C
3.3V, Internal PHY Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x32
1.8V, External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0
3.3V, External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

6.11.5.13.2.2.1.2 OSPI0 Timing Requirements - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_CLK edge	1.8V, SDR with Internal PHY Loopback	6		ns
			3.3V, SDR with Internal PHY Loopback	7		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_CLK edge	1.8V, SDR with Internal PHY Loopback	0.25		ns
			3.3V, SDR with Internal PHY Loopback	0		ns

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_DQS edge	1.8V, SDR with External Board Loopback	6		ns
			3.3V, SDR with External Board Loopback	7		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_DQS edge	1.8V, SDR with External Board Loopback	2		ns
			3.3V, SDR with External Board Loopback	2		ns

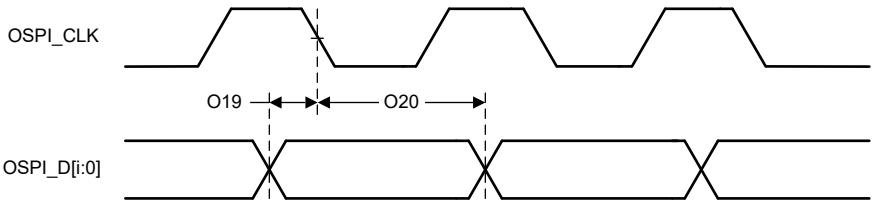


Figure 6-51. OSPI Timing Requirements – PHY SDR with Internal PHY Loopback

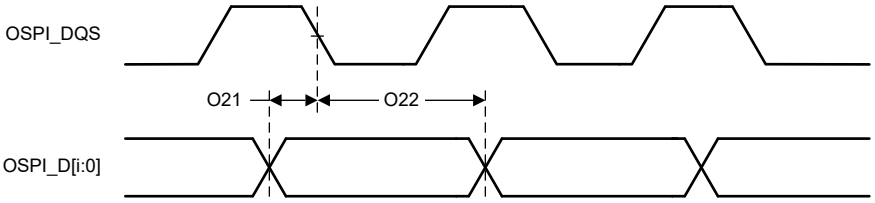


Figure 6-52. OSPI Timing Requirements – PHY SDR with External Board Loopback

6.11.5.13.2.2.1.3 OSPI0 Switching Characteristics - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI_CLK		12.5		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI_CLK low		0.475P(1) - 0.3		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI_CLK high		0.475P(1) - 0.3		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI_CSn[1:0] active edge to OSPI_CLK rising edge		0.475P(1) + (0.975 × M(2) × R(4)) - 1	0.525P(1) + (1.025 × M(2) × R(4)) + 1	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI_CLK rising edge to OSPI_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) - 1	0.525P(1) + (1.025 × N(3) × R(4)) + 1	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI_CLK active edge to OSPI_D[7:0] transition	1.8V	–1.5	–3.8	ns
			3.3V	–2	–5.15	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

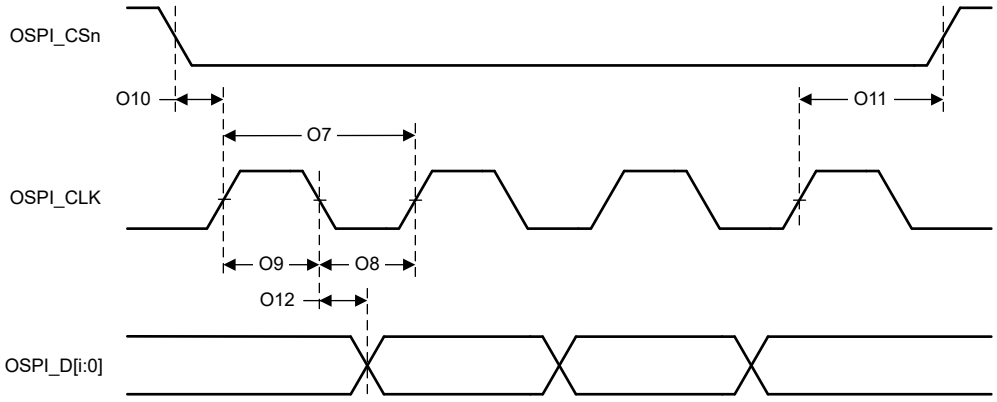


Figure 6-53. OSPI Switching Characteristics – PHY SDR

6.11.5.13.2.2.2 OSPI0 PHY DDR Timing

6.11.5.13.2.2.2.1 OSPI0 DLL Delay Mapping for PHY DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x1E
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x1E
Receive		
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x14
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x19
1.8V, DDR with External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x64
3.3V, DDR with External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x69

6.11.5.13.2.2.2.2 OSPI0 Timing Requirements - PHY DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_DQS edge	1.8V, DDR with DQS	0.400		ns
			3.3V, DDR with DQS	0.800		ns
			1.8V, DDR with External Board Loopback	6		ns
			3.3V, DDR with External Board Loopback	7		ns
O16	$t_{h(LBTCLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_DQS edge	1.8V, DDR with DQS	0.500		ns
			3.3V, DDR with DQS	0.400		ns
			1.8V, DDR with External Board Loopback	0		ns
			3.3V, DDR with External Board Loopback	0		ns

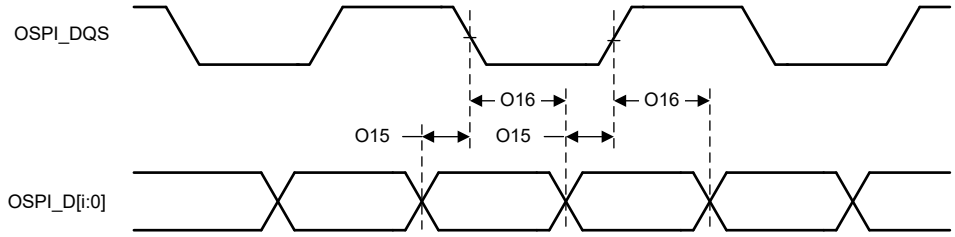


Figure 6-54. OSPI Timing Requirements – PHY DDR with External Board Loopback or DQS

6.11.5.13.2.2.2.3 OSPI0 Switching Characteristics - PHY DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI_CLK		12.5		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI_CLK low		0.475P(1) - 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI_CLK high		0.475P(1) - 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI_CSn[1:0] active edge to OSPI_CLK rising edge		0.475P(1) - (0.975 × M(2) × R(4))	0.525P(1) - (1.025 × M(2) × R(4)) + 7	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI_CLK rising edge to OSPI_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) - 7	0.525P(1) + (1.025 × N(3) × R(4))	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI_CLK active edge to OSPI_D[7:0] transition	1.8V	–1.45	–3.4	ns
			3.3V	–1.45	–3.6	ns

(1) P = OSPI_CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

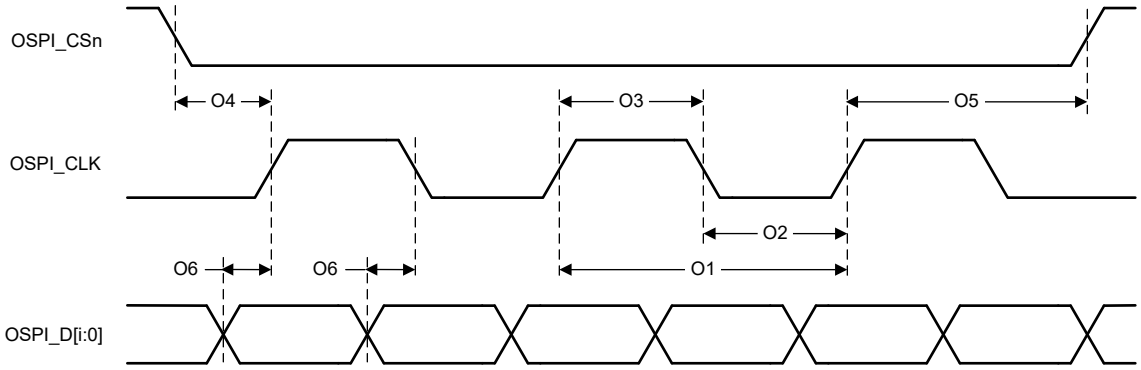


Figure 6-55. OSPI Switching Characteristics – PHY DDR

6.11.5.13.2.3 OSPI1 Without Data Training

Note

Timing parameters defined in this section are only applicable for the OSPI1 interface when data training is not implemented and DLL delays are configured as described in *OSPI1 DLL Delay Mapping for PHY SDR Timing Modes* and *OSPI1 DLL Delay Mapping for PHY DDR Timing Modes*.

6.11.5.13.2.3.1 OSPI1 PHY SDR Timing

6.11.5.13.2.3.1.1 OSPI1 DLL Delay Mapping for PHY SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x20

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x2F
Receive		
1.8V, Internal PHY Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x40
3.3V, Internal PHY Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x32
1.8V, External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0
3.3V, External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

6.11.5.13.2.3.1.2 OSPI1 Timing Requirements - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_CLK edge	1.8V, SDR with Internal PHY Loopback	6		ns
			3.3V, SDR with Internal PHY Loopback	7		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_CLK edge	1.8V, SDR with Internal PHY Loopback	0.25		ns
			3.3V, SDR with Internal PHY Loopback	0		ns
O21	$t_{su(D-LBCLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_DQS edge	1.8V, SDR with External Board Loopback	6		ns
			3.3V, SDR with External Board Loopback	7		ns
O22	$t_{h(LBCLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_DQS edge	1.8V, SDR with External Board Loopback	2		ns
			3.3V, SDR with External Board Loopback	2		ns

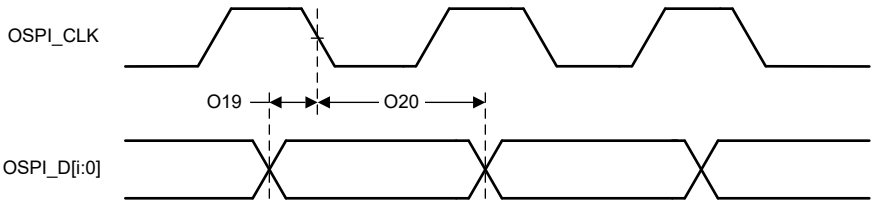


Figure 6-56. OSPI Timing Requirements – PHY SDR with Internal PHY Loopback

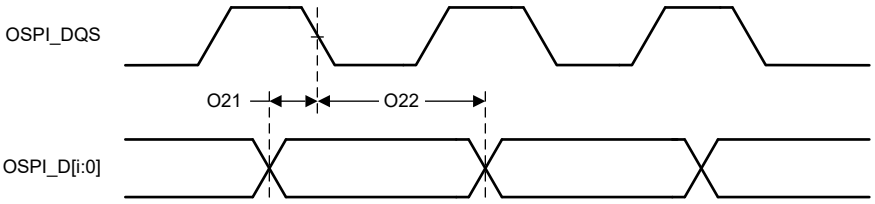


Figure 6-57. OSPI Timing Requirements – PHY SDR with External Board Loopback

6.11.5.13.2.3.1.3 OSPI1 Switching Characteristics - PHY SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI_CLK		12.5		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI_CLK low		0.475P(1) - 0.3		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI_CLK high		0.475P(1) - 0.3		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI_CSn[1:0] active edge to OSPI_CLK rising edge		0.475P(1) + (0.975 × M(2) × R(4)) - 1	0.525P(1) + (1.025 × M(2) × R(4)) + 1	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI_CLK rising edge to OSPI_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) - 1	0.525P(1) + (1.025 × N(3) × R(4)) + 1	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI_CLK active edge to OSPI_D[7:0] transition	1.8V	–1.6	–3.9	ns
			3.3V	–2.12	–5.2	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

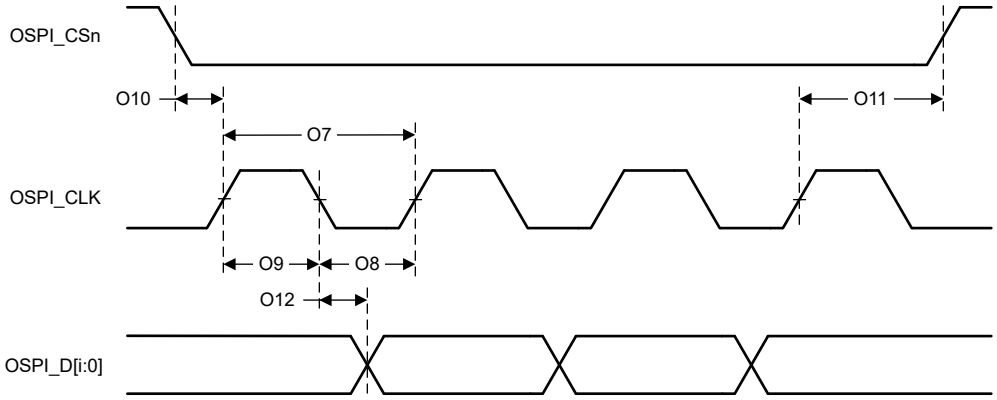


Figure 6-58. OSPI Switching Characteristics – PHY SDR

6.11.5.13.2.3.2 OSPI1 PHY DDR Timing

6.11.5.13.2.3.2.1 OSPI1 DLL Delay Mapping for PHY DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
Transmit		
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x1E
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x1E
Receive		
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x14
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x19
1.8V, DDR with External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x64
3.3V, DDR with External Board Loopback	PHY_CONFIG_RX_DLL_DELAY_FLD	0x69

6.11.5.13.2.3.2.2 OSPI1 Timing Requirements - PHY DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_DQS edge	1.8V, DDR with DQS	0.400		ns
			3.3V, DDR with DQS	0.800		ns
			1.8V, DDR with External Board Loopback	6		ns
			3.3V, DDR with External Board Loopback	7		ns
O16	$t_{h(LBTCLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_DQS edge	1.8V, DDR with DQS	0.500		ns
			3.3V, DDR with DQS	0.400		ns
			1.8V, DDR with External Board Loopback	0		ns
			3.3V, DDR with External Board Loopback	0		ns

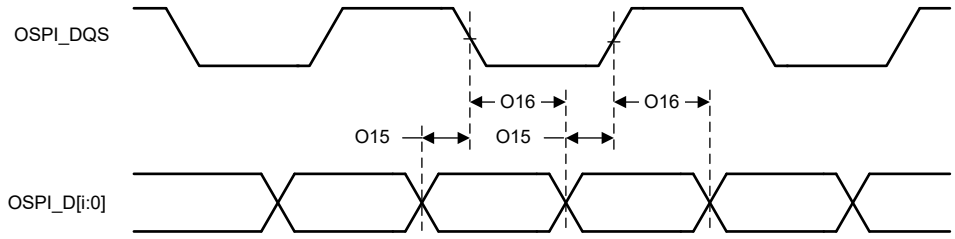


Figure 6-59. OSPI Timing Requirements – PHY DDR with External Board Loopback or DQS

6.11.5.13.2.3.2.3 OSPI1 Switching Characteristics - PHY DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI_CLK		12.5		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI_CLK low		0.475P(1) - 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI_CLK high		0.475P(1) - 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI_CSn[1:0] active edge to OSPI_CLK rising edge		0.475P(1) - (0.975 × M(2) × R(4))	0.525P(1) - (1.025 × M(2) × R(4)) + 7	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI_CLK rising edge to OSPI_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) - 7	0.525P(1) + (1.025 × N(3) × R(4))	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI_CLK active edge to OSPI_D[7:0] transition	1.8V	–1.5	–3.7	ns
			3.3V	–1.5	–3.7	ns

(1) P = OSPI_CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

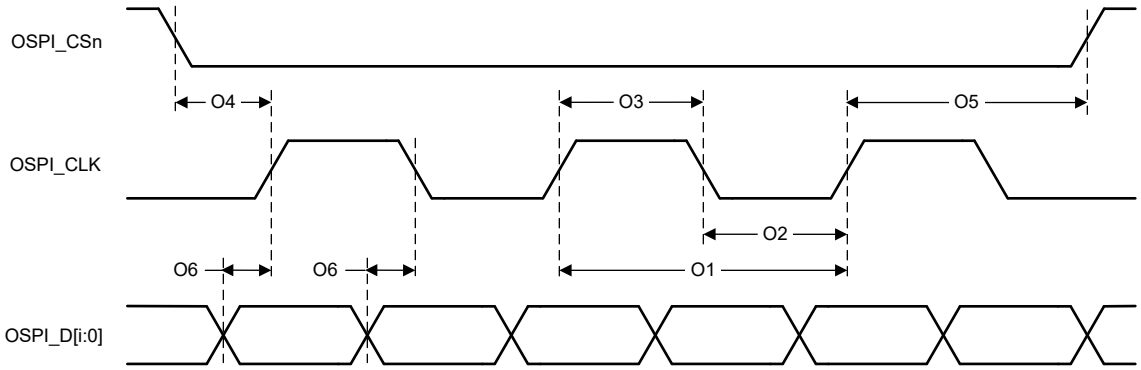


Figure 6-60. OSPI Switching Characteristics – PHY DDR

6.11.5.13.3 OSPI Tap Mode

6.11.5.13.3.1 OSPI Tap SDR Timing

6.11.5.13.3.1.1 OSPI Timing Requirements - Tap SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_CLK edge	No Loopback	10.4 - (0.975 × T(1) × R(2))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_CLK edge	No Loopback	0.7 + (0.975 × T(1) × R(2))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = REFCLK cycle time in ns

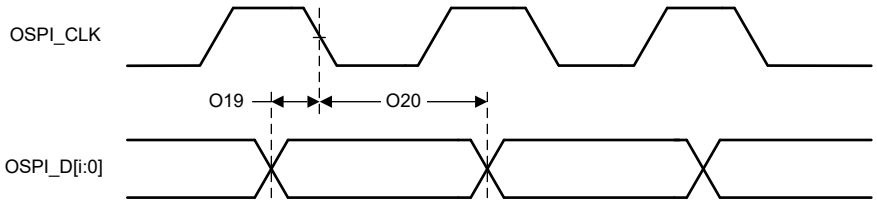


Figure 6-61. OSPI Timing Requirements – Tap SDR, No Loopback

6.11.5.13.3.1.2 OSPI Switching Characteristics - Tap SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI_CLK low		0.475P(1) - 0.3		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI_CLK high		0.475P(1) - 0.3		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI_CSn[1:0] active edge to OSPI_CLK rising edge		0.475P(1) + (0.975 × M(2) × R(4)) - 1	0.525P(1) + (1.025 × M(2) × R(4)) + 1	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI_CLK rising edge to OSPI_CSn[1:0] inactive edge		0.475P(1) + (0.975 × N(3) × R(4)) - 1	0.525P(1) + (1.025 × N(3) × R(4)) + 1	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI_CLK active edge to OSPI_D[7:0] transition		–4.25	7.25	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns

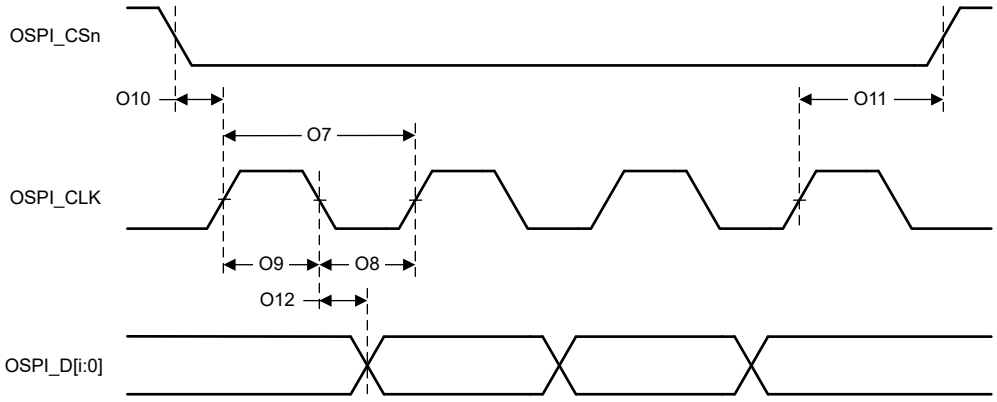


Figure 6-62. OSPI Switching Characteristics – Tap SDR, No Loopback

6.11.5.13.3.2 OSPI0 Tap DDR Timing

6.11.5.13.3.2.1 OSPI Timing Requirements - Tap DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_CLK edge	No Loopback	12.04 - (0.975 × T[1] × R[2])		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_CLK edge	No Loopback	1.84 + (0.975 × T[1] × R[2])		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = REFCLK cycle time in ns

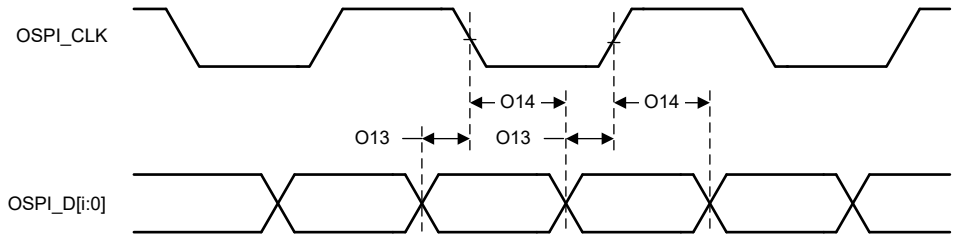


Figure 6-63. OSPI0 Timing Requirements – Tap DDR, No Loopback

6.11.5.13.3.2.2 OSPI Switching Characteristics - Tap DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI_CLK low		0.475P[1] - 0.3		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI_CLK high		0.475P[1] - 0.3		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI_CSn[1:0] active edge to OSPI_CLK rising edge		0.475P[1] + (0.975 × M[2] × R[4]) - 1	0.525P[1] + (1.025 × M[2] × R[4]) + 1	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI_CLK rising edge to OSPI_CSn[1:0] inactive edge		0.475P[1] + (0.975 × N[3] × R[4]) - 1	0.525P[1] + (1.025 × N[3] × R[4]) + 1	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI_CLK active edge to OSPI_D[7:0] transition		–17.94 + (0.975 × T[5] × R[4])	–1.56 + (1.025 × T[5] × R[4])	ns

(1) P = CLK cycle time = SCLK period in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = REFCLK cycle time in ns
(5) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]

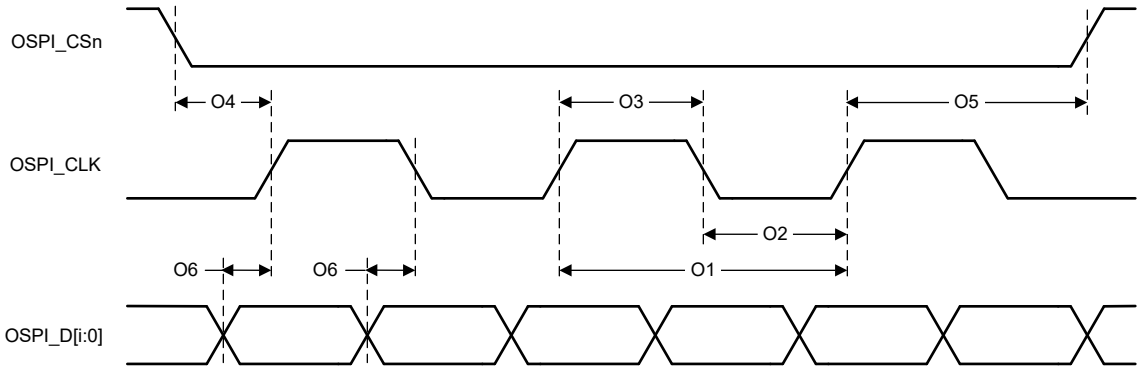


Figure 6-64. OSPI0 Switching Characteristics – Tap DDR, No Loopback

6.11.5.14 Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)

There are two unique Programmable Real-Time Unit and Industrial Communication Subsystems (PRU-ICSS0 and PRU-ICSS1) integrated into the device. The programmable nature of the PRU cores, along with enhanced GPIO access to device pins, system events, and other device resources, provides flexibility in implementing fast real-time responses, specialized data handling operations, custom peripheral interfaces, and offloading tasks from other processor cores in the device.

For more details about features and additional description information on the device PRU-ICSS, see the corresponding subsections within the device specific TRM.

Note

The PRU-ICSS requires a second layer of signal multiplexing in addition to the top-level device pin multiplexing. Refer to the Environment section of the PRU-ICSS TRM Chapter for additional details.

Note

The generic PRU-ICSS naming and PRU_ prefix is used to represent the signal names for all PRU-ICSS instances.

6.11.5.14.1 PRU-ICSS Programmable Real-Time Unit (PRU)

Note

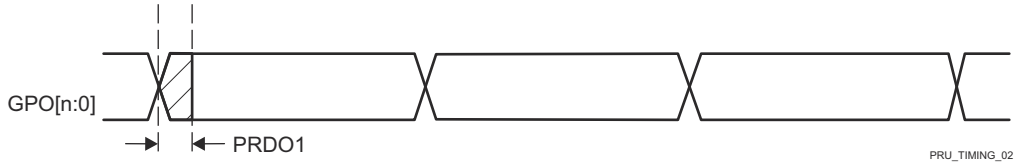
The PRU-ICSS PRU signals have different functionality depending on the mode of operation. The signal naming in this section matches the naming used in the *PRU Module Interface* section in the device TRM.

6.11.5.14.1.1 PRU-ICSS PRU Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	30	pF

6.11.5.14.1.2 PRU-ICSS PRU Switching Characteristics - Direct Output Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRDO1	$t_{sk(PRU\_GPO)}$	PRU_GPO (data out) skew		3	ns



A. n in GPO[n:0] = 19.

Figure 6-65. PRU-ICSS PRU Direct Output Timing

6.11.5.14.1.3 PRU-ICSS PRU Timing Requirements - Parallel Capture Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPC1	$t_{c(PRU\_CLOCK)}$	Cycle time, PRU_CLOCK	20		ns
PRPC2	$t_{w(PRU\_CLOCKL}$	Pulse duration, PRU_CLOCK Low	10		ns
PRPC3	$t_{w(PRU\_CLOCKH)}$	Pulse duration, PRU_CLOCK High	10		ns
PRPC4	$t_{su(PRU\_DATAIN-PRU\_CLK)}$	Setup time, PRU_DATAIN valid before PRU_CLOCK active edge	4		ns
PRPC5	$t_{th(PRU\_CLOCK-PRU\_DATAIN)}$	Hold time, PRU_DATAIN valid after PRU_CLOCK active edge	0		ns

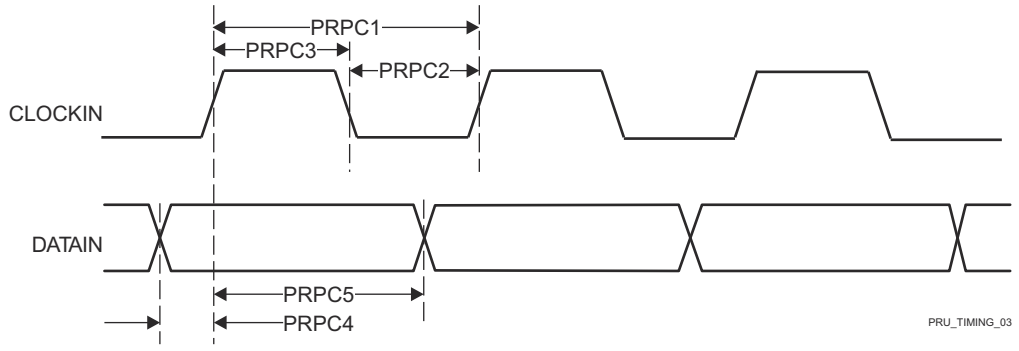


Figure 6-66. PRU-ICSS PRU Parallel Capture Timing Requirements – Rising Edge Mode

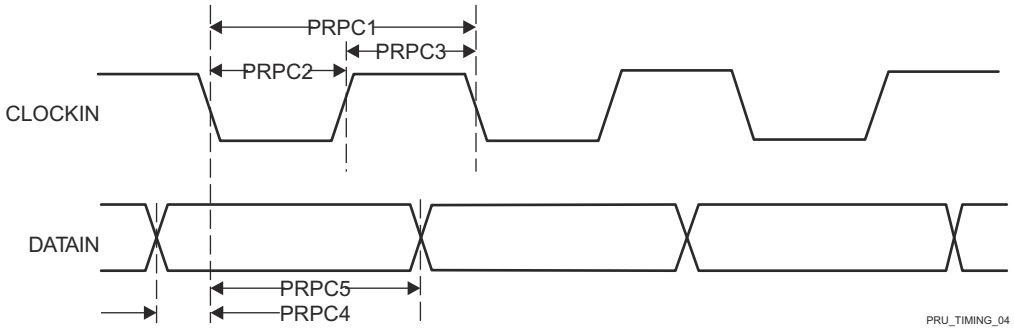


Figure 6-67. PRU-ICSS PRU Parallel Capture Timing Requirements – Falling Edge Mode

6.11.5.14.1.4 PRU-ICSS PRU Timing Requirements - Shift In Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSI1	$t_{w(PRU\_DATAINH)}$	Pulse duration, PRU_DATAIN High	2 + 2P(1)		ns
PRSI2	$t_{w(PRU\_DATAINL)}$	Pulse duration, PRU_DATAIN Low	2 + 2P(1)		ns

(1) P = Internal shift in clock period, defined by PRU_GPI_DIV0 and PRU0_GPI_DIV1 bit fields in the GPCFGn register.

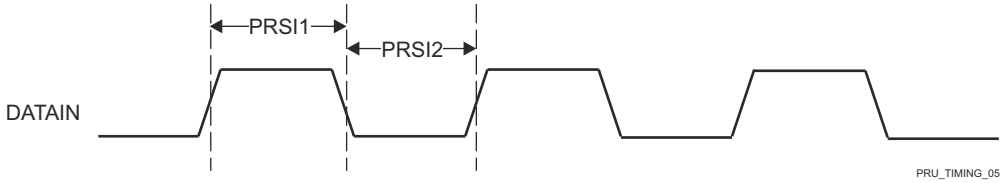


Figure 6-68. PRU-ICSS PRU Shift In Timing

6.11.5.14.1.5 PRU-ICSS PRU Switching Characteristics - Shift Out Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSO1	$t_{c(PRU\_CLOCKOUT)}$	Cycle time, PRU_CLOCKOUT	10		ns
PRSO2L	$t_{w(PRU\_CLOCKOUTL)}$	Pulse duration, PRU_CLOCKOUT Low	–0.3 + 0.475 × P(1) × Z(2)		ns
PRSO2H	$t_{w(PRU\_CLOCKOUTH)}$	Pulse duration, PRU_CLOCKOUT High	–0.3 + 0.475 × P(1) × Y(3)		ns
PRSO3	$t_{d(PRU\_CLOCKOUT-PRU\_DATAOUT)}$	Delay time, PRU_CLOCKOUT to PRU_DATAOUT Valid	0	3	ns

(1) P = Software programmable shift out clock period, defined by PRU0_GP0_Div0 and PRU0_GPO_DIV1 bit fields in the GPCFGn register.

(2) The Z parameter is defined as follows:
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are INTEGERS -or- if PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an EVEN INTEGER then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1).
If PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an ODD INTEGER then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.5).
If PRU0_GPI_DIV0 is an INTEGER and PRU0_GPI_DIV1 is a NON-INTEGER then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.5 * PRU0_GPI_DIV0).
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are NON-INTEGERS then,
Z equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.25 * PRU0_GPI_DIV0).

(3) The Y parameter is defined as follows:
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are INTEGERS -or- if PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an EVEN INTEGER then,
Y equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1).
If PRU0_GPI_DIV0 is a NON-INTEGER and PRU0_GPI_DIV1 is an ODD INTEGER then,
Y equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 - 0.5).
If PRU0_GPI_DIV0 is an INTEGER and PRU0_GPI_DIV1 is a NON-INTEGER then,
Y equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 - 0.5 * PRU0_GPI_DIV0).
If PRU0_GPI_DIV0 and PRU0_GPI_DIV1 are NON-INTEGERS then,
Y1 equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 - 0.25 * PRU0_GPI_DIV0) and

Y2 equals (PRU0_GPI_DIV0 * PRU0_GPI_DIV1 + 0.25 * PRU0_GPI_DIV0), where Y1 is the first high pulse and Y2 is the second high pulse.

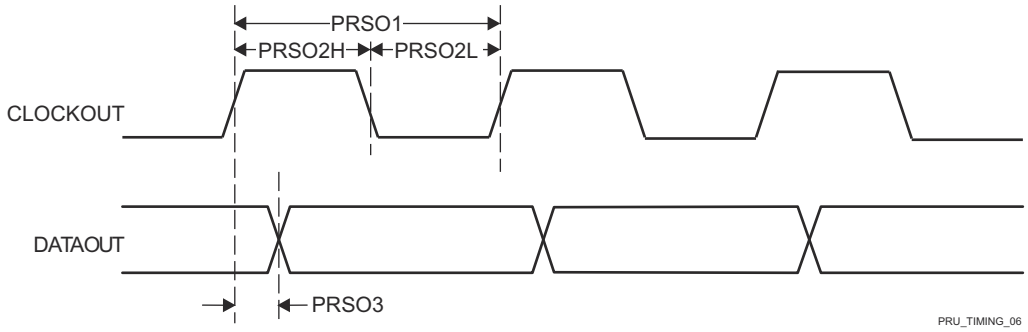


Figure 6-69. PRU-ICSS PRU Shift Out Timing

6.11.5.14.2 PRU-ICSS PRU Sigma Delta and Peripheral Interface

6.11.5.14.2.1 PRU-ICSS PRU Sigma Delta and Peripheral Interface Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	18	pF

6.11.5.14.2.2 PRU-ICSS PRU Timing Requirements - Sigma Delta Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRSD1	$t_{c(SD\_CLK)}$	Cycle time, SD_CLK	40		ns
PRSD2L	$t_{w(SD\_CLKL)}$	Pulse duration, SD_CLK Low	20		ns
PRSD2H	$t_{w(SD\_CLKH)}$	Pulse duration, SD_CLK High	20		ns
PRSD3	$t_{su(SD\_D-SDCLK)}$	Setup time, SD_D valid before SD_CLK active edge	10		ns
PRSD4	$t_{su(SDCLK-SD\_D)}$	Hold time, SD_D valid after SD_CLK active edge	5		ns

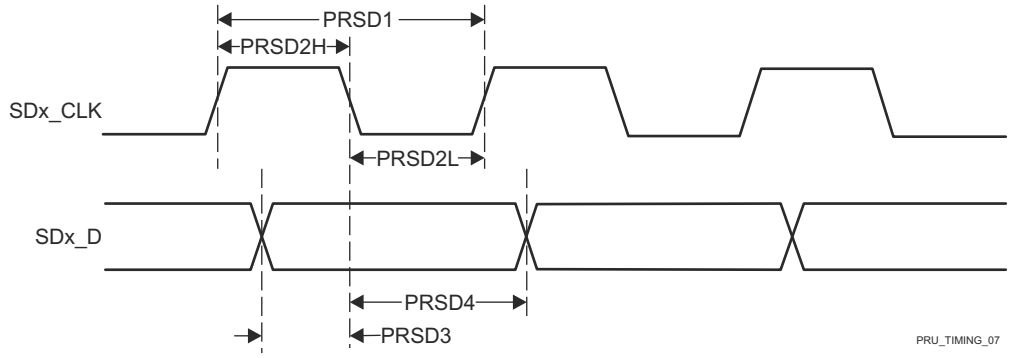


Figure 6-70. PRU-ICSS PRU SD_CLK Falling Active Edge

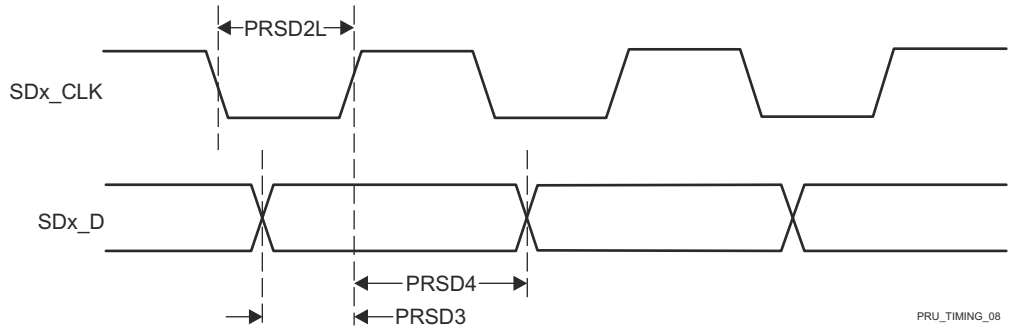


Figure 6-71. PRU-ICSS PRU SD_CLK Rising Active Edge

6.11.5.14.2.3 PRU-ICSS PRU Timing Requirements - Peripheral Interface Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF1	$t_{w(PIF\_DATA\_INH)}$	Pulse duration, PIF_DATA_IN High	2 + 0.475 × (4 × P(1))		ns

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF2	$t_{w(PIF\_DATA\_INL)}$	Pulse duration, PIF_DATA_IN Low	2 + 0.475 × (4 × P[(1)])		ns

(1) P = 1x (or TX) clock period, defined by TX_DIV_FACTOR and TX_DIV_FACTOR_FRAC in the CFG_ED_P<n>_TXCFG register.

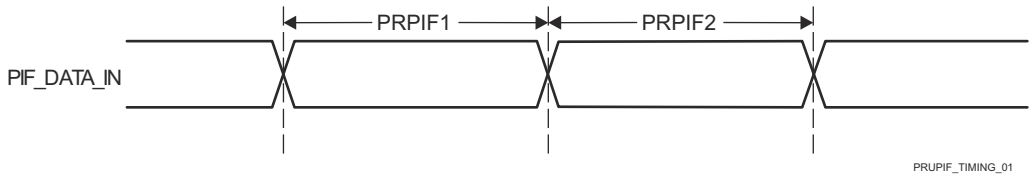


Figure 6-72. PRU-ICSS PRU Peripheral Interface Timing Requirements

6.11.5.14.2.4 PRU-ICSS PRU Switching Characteristics - Peripheral Interface Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPIF3	$t_{c(PIF\_CLK)}$	Cycle time, PIF_CLK	30		ns
PRPIF4	$t_{w(PIF\_CLKH)}$	Pulse duration, PIF_CLK High	0.475P[(1)]		ns
PRPIF5	$t_{w(PIF\_CLKL)}$	Pulse duration, PIF_CLK Low	0.475P[(1)]		ns
PRPIF6	$t_{d(PIF\_CLK-PIF\_DATA\_OUT)}$	Delay time, PIF_CLK fall to PIF_DATA_OUT	–5	5	ns
PRPIF7	$t_{d(PIF\_CLK-PIF\_DATA\_EN)}$	Delay time, PIF_CLK fall to PIF_DATA_EN	–5	5	ns

(1) P = 1x (or TX) clock period, defined by TX_DIV_FACTOR and TX_DIV_FACTOR_FRAC in the CFG_ED_P<n>_TXCFG register.

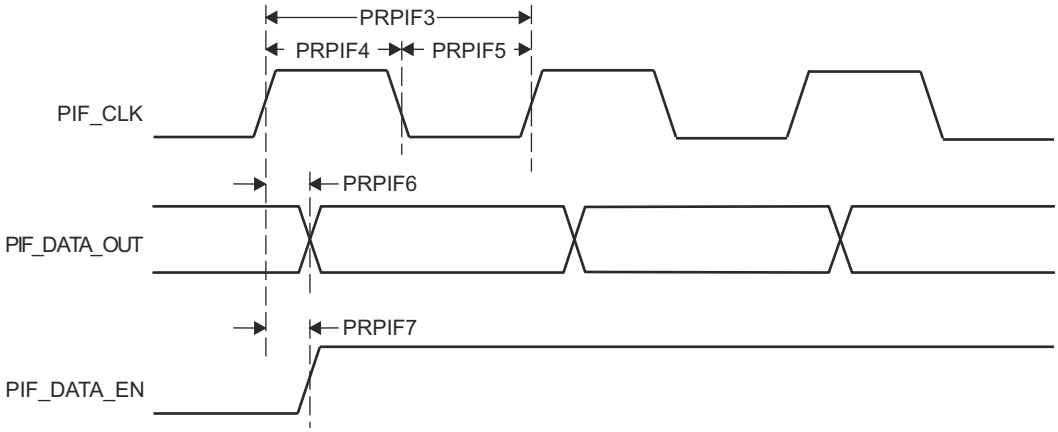


Figure 6-73. PRU-ICSS PRU Peripheral Interface Switching Characteristics

6.11.5.14.3 PRU-ICSS Pulse Width Modulation (PWM)

6.11.5.14.3.1 PRU-ICSS PWM Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.14.3.2 PRU-ICSS PWM Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRPWM1	$t_{sk(PWM\_A/B)}$	PWM_A/B skew		5	ns

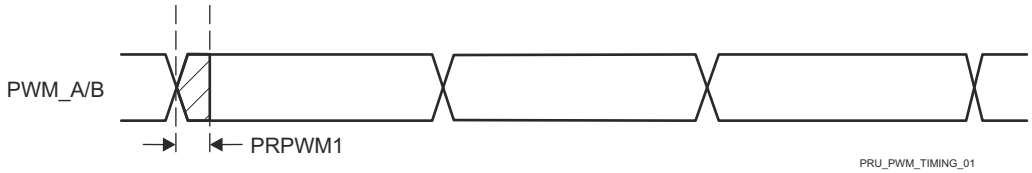


Figure 6-74. PRU-ICSS PWM Timing

6.11.5.14.4 PRU-ICSS Industrial Ethernet Peripheral (IEP)

6.11.5.14.4.1 PRU-ICSS IEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	7	pF

6.11.5.14.4.2 PRU-ICSS IEP Timing Requirements - Input Validated with SYNCx

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRIEP1	$t_{w(EDC\_SYNCx\_OUTL)}$	Pulse duration, EDC_SYNCx_OUT Low	–2 + 20P(1)		ns
PRIEP2	$t_{w(EDC\_SYNCx\_OUTH)}$	Pulse duration, EDC_SYNCx_OUT High	–2 + 20P(1)		ns
PRIEP3	$t_{su(EDIO\_DATA\_IN-EDC\_SYNCx\_OUT}$	Setup time, EDIO_DATA_IN valid before EDC_SYNCx_OUT active edge	20		ns
PRIEP4	$t_{h(EDC\_SYNCx\_OUT-EDIO\_DATA\_IN)}$	Hold time, EDIO_DATA_IN valid after EDC_SYNCx_OUT active edge	20		ns

(1) P = PRU-ICSS IEP clock source period.

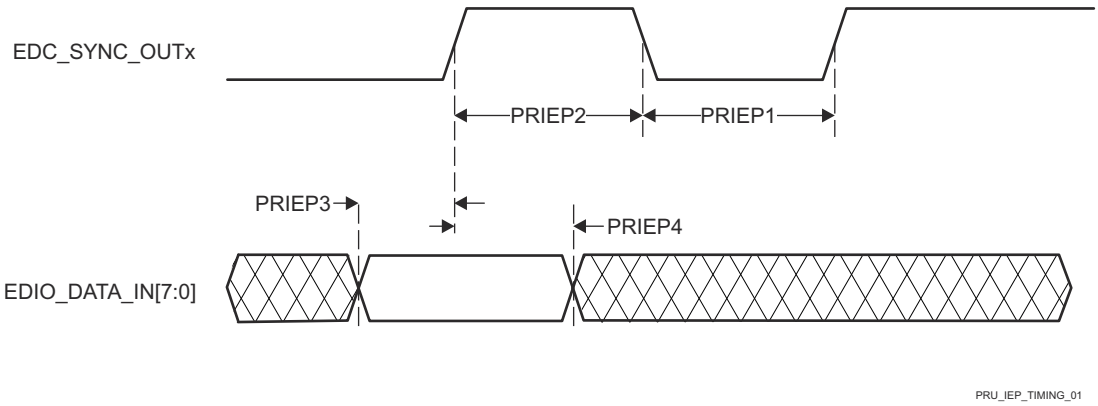


Figure 6-75. PRU-ICSS IEP SYNC Timing Requirements

6.11.5.14.4.3 PRU-ICSS IEP Timing Requirements - Digital IOs

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
IEPIO1	$t_{w(EDIO\_OUTVALIDL)}$	Pulse duration, EDIO_OUTVALID Low	–2 + 14P(1)		ns
IEPIO2	$t_{w(EDIO\_OUTVALIDH)}$	Pulse duration, EDIO_OUTVALID High	–2 + 32P(1)		ns
IEPIO3	$t_{d(EDIO\_OUTVALID-EDIO\_DATA\_OUT)}$	Delay time, EDIO_OUTVALID to EDIO_DATA OUT	0	18P(1)	ns
IEPIO4	$t_{sk(EDIO\_DATA\_OUT)}$	EDIO_DATA_OUT skew	6		ns

(1) P = PRU-ICSS IEP clock source period.

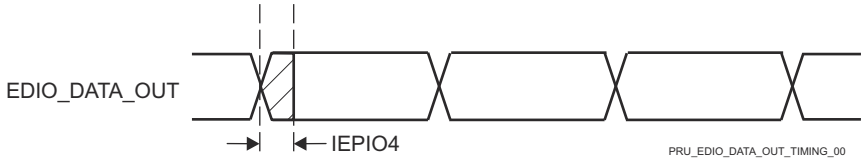


Figure 6-76. PRU-ICSS IEP Digital IOs Timing Requirements

6.11.5.14.4.4 PRU-ICSS IEP Timing Requirements - LATCHx_IN

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRLA1	$t_{w(EDC\_LATCHx\_INL)}$	Pulse duration, EDC_LATCHx_IN Low	2 + 3P(1)		ns
PRLA2	$t_{w(EDC\_LATCHx\_INH)}$	Pulse duration, EDC_LATCHx_IN High	2 + 3P(1)		ns

(1) P = PRU-ICSS IEP clock source period.

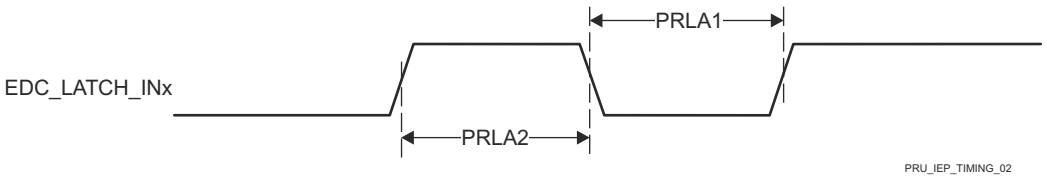


Figure 6-77. PRU-ICSS IEP LATCH_INx Timing Requirements

6.11.5.14.5 PRU-ICSS Universal Asynchronous Receiver Transmitter (UART)

6.11.5.14.5.1 PRU-ICSS UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.01	0.33	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	30	pF

6.11.5.14.5.2 PRU-ICSS UART Timing Requirements

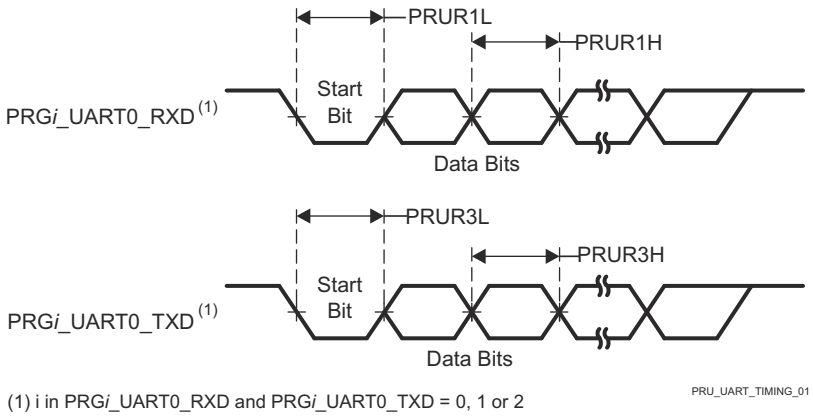
NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRUR1H	$t_{w(RXH)}$	Pulse duration, Receive start, stop, data bit High	U(1)		ns
PRUR1L	$t_{w(RXL)}$	Pulse duration, Receive start, stop, data bit Low	–2 + U(1)		ns

(1) U = UART baud time = 1/programmed baud rate.

6.11.5.14.5.3 PRU-ICSS UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PRUR2	$f_{(baud)}$	Maximum programmable baud rate	U(1)		ns
PRUR3H	$t_{w(TXH)}$	Pulse duration, Transmit start, stop, data bit High	–2 + U(1)		ns

(1) U = UART baud time = 1/programmed baud rate.



(1) i in PRG*i*_UART0_RXD and PRG*i*_UART0_TXD = 0, 1 or 2

Figure 6-78. PRU-ICSS UART Timing Requirements and Switching Characteristics

6.11.5.14.6 PRU-ICSS Enhanced Capture Peripheral (ECAP)

6.11.5.14.6.1 PRU-ICSS ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	1	3	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	7	pF

6.11.5.14.6.2 PRU-ICSS ECAP Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP1	$t_{w(CAP)}$	Pulse duration, Capture input (asynchronous)	2 + 2P(1)		ns
PREP2	$t_{w(SYNCI)}$	Pulse duration, Sync input (asynchronous)	2 + 2P(1)		ns

(1) P = CORE_CLK period in ns

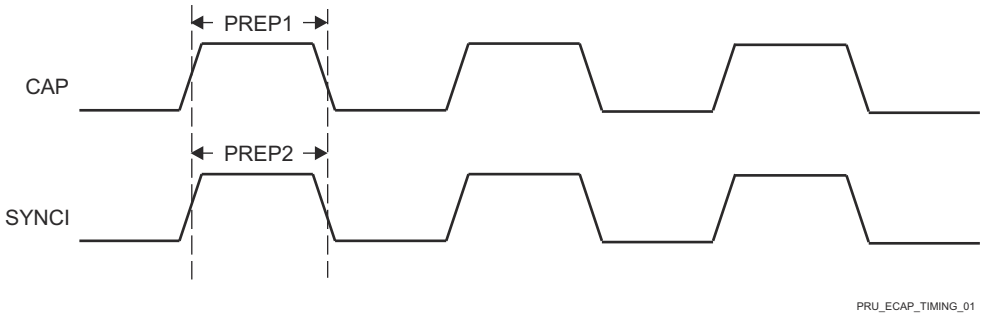


Figure 6-79. PRU-ICSS ECAP Timing

6.11.5.14.6.3 PRU-ICSS ECAP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PREP3	$t_{w(APWM)}$	Pulse duration, Auxiliary PWM (APWM) output high/low	2P(1)		ns
PREP4	$t_{w(SYNCO)}$	Pulse duration, Sync output (asynchronous)	P(1)		ns

(1) P = CORE_CLK period in ns

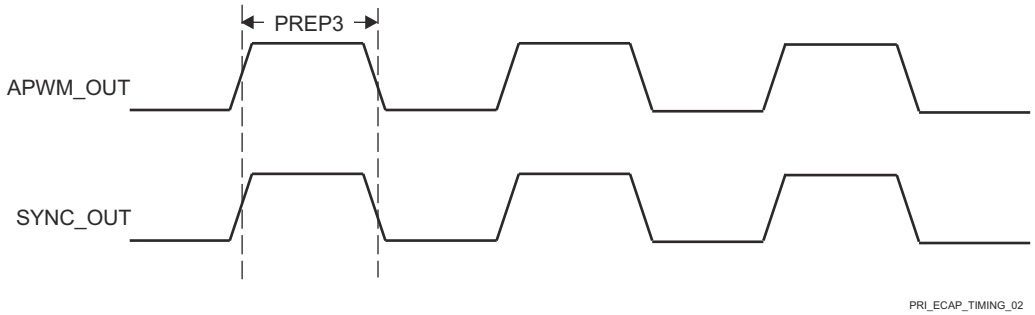


Figure 6-80. PRU-ICSS ECAP Switching Characteristics

6.11.5.14.7 PRU-ICSS MDIO and MII

6.11.5.14.7.1 PRU-ICSS MDIO Timing

6.11.5.14.7.1.1 PRU-ICSS MDIO Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	10	470	pF

6.11.5.14.7.1.2 PRU-ICSS MDIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO1	$t_{su(MDIO-MDC)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	$t_{h(MDC-MDIO)}$	Hold time, MDIO[x]_MDIO valid from MDIO[x]_MDC high	0		ns

6.11.5.14.7.1.3 PRU-ICSS MDIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
MDIO3	$t_{c(MDC)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(MDCH)}$	Pulse duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(MDCL)}$	Pulse duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(MDC-MDIO)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	–150	150	ns

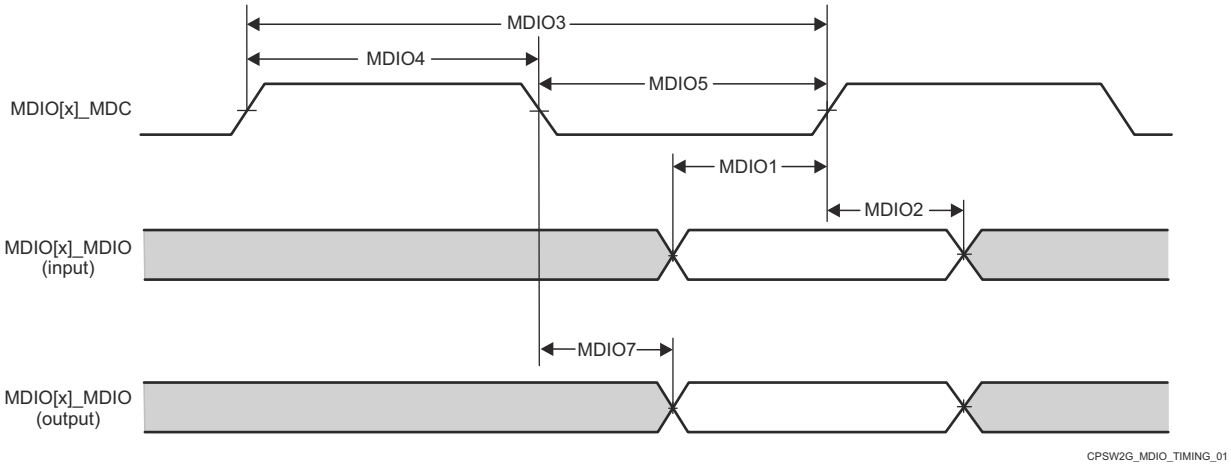


Figure 6-81. PRU-ICSS MDIO Timing Requirements and Switching Characteristics

6.11.5.14.7.2 PRU-ICSS MII Timing

6.11.5.14.7.2.1 PRU-ICSS MII Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				

PARAMETER		MIN	MAX	UNIT
C_L	Output Load Capacitance	2	20	pF

6.11.5.14.7.2.2 PRU-ICSS MII Timing Requirements - MII[x]_RX_CLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR1	$t_{c(RX\_CLK)}$	Cycle time, MII[x]_RX_CLK	10Mbps	399.96	400.04	ns
			100Mbps	39.996	40.004	ns
PMIR2	$t_{w(RX\_CLKH)}$	Pulse duration, MII[x]_RX_CLK high	10Mbps	140	260	ns
			100Mbps	14	26	ns
PMIR3	$t_{w(RX\_CLKL)}$	Pulse duration, MII[x]_RX_CLK low	10Mbps	140	260	ns
			100Mbps	14	26	ns

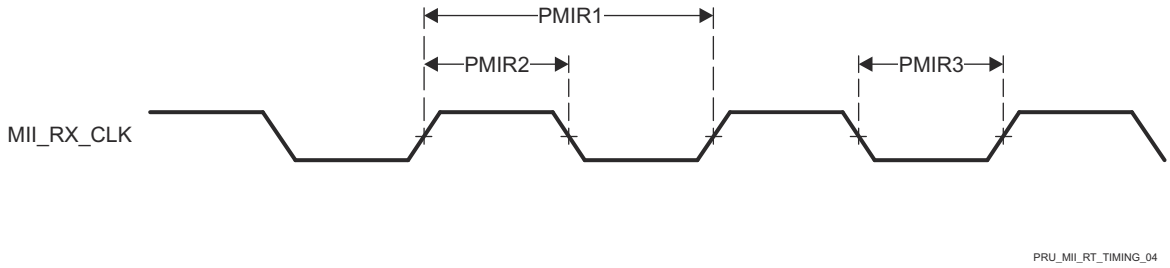


Figure 6-82. PRU-ICSS MII[x]_RX_CLK Timing

6.11.5.14.7.2.3 PRU-ICSS MII Timing Requirements - MII[x]_RXD[3:0], MII[x]_RX_DV, and MII[x]_RX_ER

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIR4	$t_{su(RXD-RX\_CLK)}$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	10Mbps	8		ns
	$t_{su(RX\_DV-RX\_CLK)}$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns
	$t_{su(RX\_ER-RX\_CLK)}$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns
	$t_{su(RXD-RX\_CLK)}$	Setup time, MII[x]_RXD[3:0] valid before MII[x]_RX_CLK	100Mbps	8		ns
	$t_{su(RX\_DV-RX\_CLK)}$	Setup time, MII[x]_RX_DV valid before MII[x]_RX_CLK		8		ns
	$t_{su(RX\_ER-RX\_CLK)}$	Setup time, MII[x]_RX_ER valid before MII[x]_RX_CLK		8		ns
PMIR5	$t_{h(RX\_CLK-RXD)}$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK	10Mbps	8		ns
	$t_{h(RX\_CLK-RX\_DV)}$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX\_CLK-RX\_ER)}$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX\_CLK-RXD)}$	Hold time, MII[x]_RXD[3:0] valid after MII[x]_RX_CLK	100Mbps	8		ns
	$t_{h(RX\_CLK-RX\_DV)}$	Hold time, MII[x]_RX_DV valid after MII[x]_RX_CLK		8		ns
	$t_{h(RX\_CLK-RX\_ER)}$	Hold time, MII[x]_RX_ER valid after MII[x]_RX_CLK		8		ns

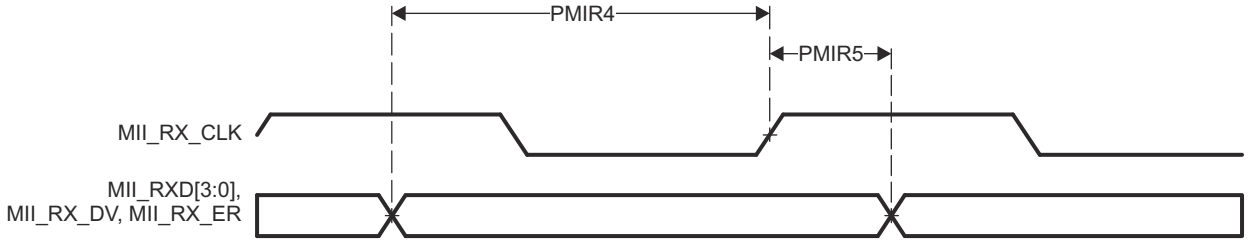


Figure 6-83. PRU-ICSS MII[x]_RXD[3:0], MII[x]_RX_DV, and MII[x]_RX_ER Timing

6.11.5.14.7.2.4 PRU-ICSS MII Switching Characteristics - MII[x]_TX_CLK

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT1	$t_{c(TX\_CLK)}$	Cycle time, MII[x]_TX_CLK	10Mbps	399.96	400.04	ns
			100Mbps	39.996	40.004	ns
PMIT2	$t_{w(TX\_CLKH)}$	Pulse duration, MII[x]_TX_CLK high	10Mbps	140	260	ns
			100Mbps	14	26	ns
PMIT3	$t_{w(TX\_CLKL)}$	Pulse duration, MII[x]_TX_CLK low	10Mbps	140	260	ns
			100Mbps	14	26	ns

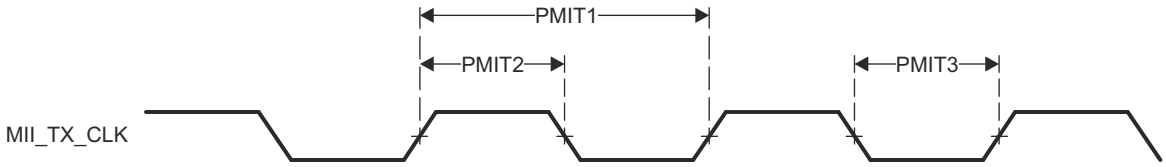


Figure 6-84. PRU-ICSS MII[x]_TX_CLK Timing

6.11.5.14.7.2.5 PRU-ICSS MII Switching Characteristics - MII[x]_TXD[3:0] and MII[x]_TXEN

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
PMIT4	$t_{d(TX\_CLK-TXD)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TXD[3:0] valid	10Mbps	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TX_EN valid		0	25	ns
	$t_{d(TX\_CLK-TXD)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TXD[3:0] valid	100Mbps	0	25	ns
	$t_{d(TX\_CLK-TX\_EN)}$	Delay time, MII[x]_TX_CLK high to MII[x]_TX_EN valid		0	25	ns

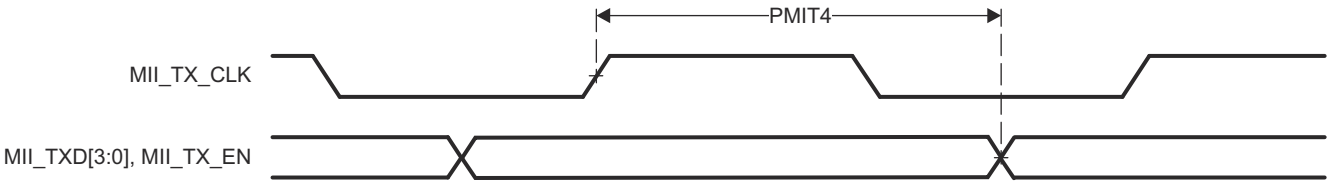


Figure 6-85. PRU-ICSS MII[x]_TXD[3:0], MII[x]_TX_EN Timing

6.11.5.15 Sigma Delta Filter Module (SDFM)

For more information, see *Sigma Delta Filter Module* section in the device TRM.

6.11.5.15.1 SDFM Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input Slew Rate	Mode 0	0.5	5	V/ns

6.11.5.15.2 SDFM Switching Characteristics

(2)

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
M0-1	$t_{c(SDC)}$	Cycle time, SDx_Cy	Mode 0	5P(1)	256P(1)	ns
M0-2	$t_{w(SDCHL)}$	Pulse duration, SDx_Cy (high/low)	Mode 0	2P(1)		ns
M0-3	$t_{sh(SDDV-SDCH)}$	Setup time, SDx_Dy valid before SDx_Cy high	Mode 0	2P(1)		ns
M0-4	$t_{h(SDCH-SDD)}$	Hold time, SDx_Dy wait after SDx_Cy high	Mode 0	2P(1)		ns

(1) P = SYSCLK period in ns.
(2) Some SDFM signals are pinmuxed with I2C0 SDA and SCL pins. These pins use an alternate open drain voltage buffer and may not meet the specified parameters. Values are pending additional post-silicon validation.

6.11.5.16 Universal Asynchronous Receiver/Transmitter (UART)

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding subsections within *Signal Descriptions* and *Detailed Description* sections.

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in the device TRM.

6.11.5.16.1 UART Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	1	30	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d\ (Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

6.11.5.16.2 UART Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
4	$t_{w(RX)}$	Pulse width, receive data bit, high or low	0.95U[1]	1.05U[1]	ns
5	$t_{w(CTS)}$	Pulse width, receive start bit, high or low	0.95U[1]		ns

(1) U = UART baud time = 1 / Programmed baud rate.

6.11.5.16.3 UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
	$f_{(baud)}$	Programmable baud rate	15pF		12	Mbps
			30pF		0.115	
2	$t_{w(TX)}$	Pulse width, transmit data bit, high or low		U[1] – 2.2	U[1] + 2.2	ns
3	$t_{w(RTS)}$	Pulse width, transmit start bit, high or low		U[1] – 2.2		ns
1	$t_{d(CTS-TX)}$	Delay time, receive CTS bit to transmit data		30		ns

(1) U = UART baud time = 1 / Programmed baud rate.

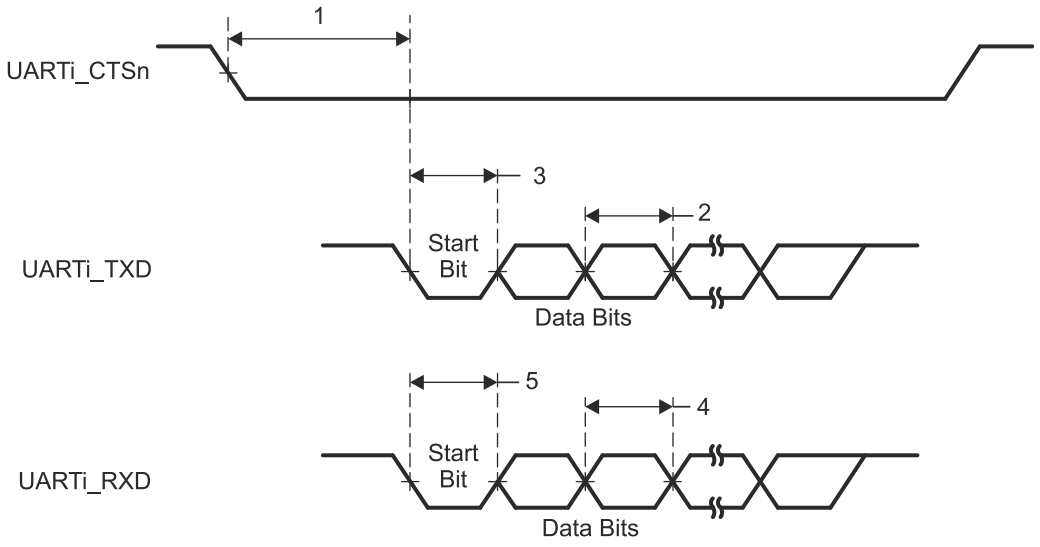


Figure 6-86. UART Timing Requirements and Switching Characteristics

6.11.5.17 Universal Serial Bus (USB)

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the *Universal Serial Bus* section in the device TRM

6.11.6 Emulation and Debug

For more details about features and additional description information on the device Trace and JTAG interfaces, see the *On-Chip Debug* section in the device TRM.

6.11.6.1 JTAG

The acronym stands for the **Joint Test Action Group**, the committee of engineers who defined the boundary-scan standard (IEEE std 1149.1). For more details about features and additional description information on the device JTAG interface, see the corresponding subsections within the device TRM.

6.11.6.1.1 JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input Slew Rate	0.5	2.00	V/ns
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	5	15	pF

6.11.6.1.2 JTAG Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time, TCK	40		ns
J2	$t_{w(TCKH)}$	Pulse width, TCK high	16		ns
J3	$t_{w(TCKL)}$	Pulse width, TCK low	16		ns
J4	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	2		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	2		
J5	$t_{h(TCK-TDI)}$	Input hold time, TDI valid from TCK high	15.9		ns
	$t_{h(TCK-TMS)}$	Input hold time, TMS valid from TCK high	15.9		

6.11.6.1.3 JTAG Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time, TCK low to TDO invalid	–0.067005		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time, TCK low to TDO valid		11.89594	ns

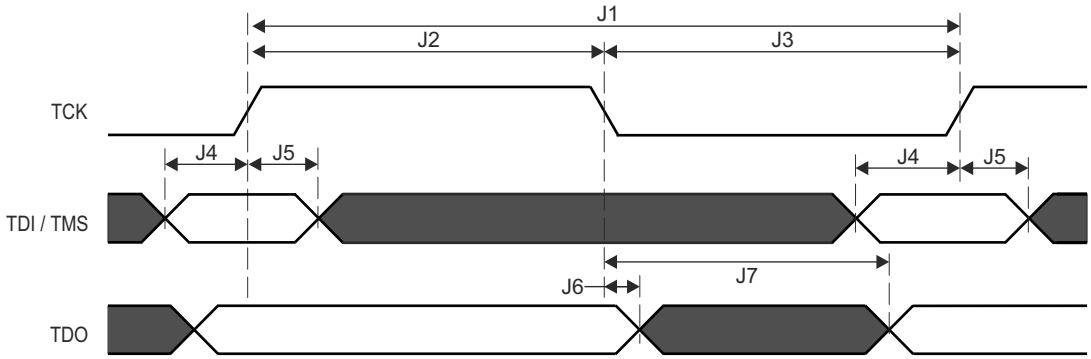


Figure 6-87. JTAG Timing Requirements and Switching Characteristics

6.11.6.2 Trace

6.11.6.2.1 Debug Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output Load Capacitance	2	5	pF
OUTPUT CONDITIONS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces.		200	ps

6.11.6.2.2 Debug Trace Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
DBTR1	$tc_{(TRC\_CLK)}$	Cycle time, TRC_CLK	9.75		ns
DBTR2	$t_{w(TRC\_CLKH)}$	Pulse width, TRC_CLK high	4.13		ns
DBTR3	$t_{w(TRC\_CLKL)}$	Pulse width, TRC_CLK low	4.13		ns
DBTR4	$t_{osu(TRC\_DATAV-TRC\_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.22		ns
DBTR5	$t_{oh(TRC\_CLK-TRC-DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.22		ns
DBTR6	$t_{osu(TRC\_CTLV-TRC\_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.22		ns
DBTR7	$t_{oh(TRC\_CLK-TRC\_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.22		ns

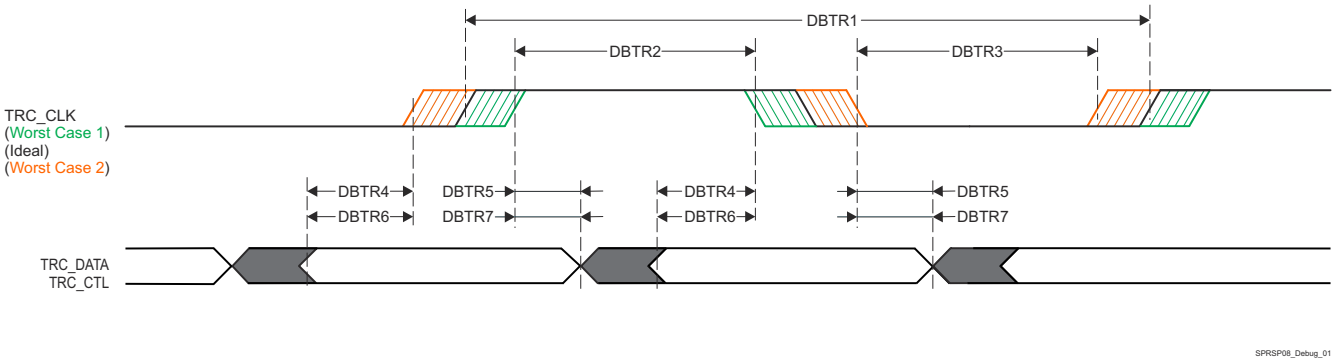


Figure 6-88. Trace Switching Characteristics

6.12 Decoupling Capacitor Requirements

6.12.1 Decoupling Capacitor Requirements

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
C_{VDD}	1.2V/1.25V VDD (Cap)		10		µF
C_{VDDS33}	3.3V VDDS (Cap)		10		µF
C_{VDDA33}	3.3V VDDA (Cap)		10		µF
C_{VDDS18}	1.8V VDDS (Cap)		0.1		µF
C_{VDDA18}	1.8V VDDA (Cap)		0.1		µF
C_{VDDA18}	1.8V VDDA (Cap)		4.7		µF
C_{VPP}	1.7V VPP (Cap)		0.1		µF
C_{VDDS18_LDO}	1.8V LDO VDDS (Cap)		3.3		µF
C_{ADC_VREF}	ADC VREFHI (Cap)		4.7		µF

7 Detailed Description

7.1 Overview

The AM261x Sitara Arm® Microcontrollers are built to meet the complex real-time processing and control needs of next generation industrial and automotive embedded projects. AM261x combines advanced computing with industry leading real-time control peripherals to meet the growing performance needs of applications such as HEV/EV (on-board chargers, DC-DC converters, Battery Management Systems), Two axis Servo drive, Industrial Digital Power control(energy storage, String Inverters), and other general real-time constrained systems. AM261x combines up to two Cortex-R5F MCUs, a real-time control subsystem (CONTROLSS), a Hardware Security Module (HSM), and two instances of Sitara's TSN-enabled PRU-ICSS, making AM261x designed for advanced motor control and digital power control applications.

The R5F cores are arranged in cluster with 512KB of shared tightly coupled memory (TCM) along with 1.5MB of shared SRAM. The Arm® cores can be optionally programmed to run in lock-step option for different functional safety configurations. Extensive ECC is included on on-chip memory, peripherals, and interconnect for enhanced reliability. Cryptographic acceleration and secure boot are also available on AM261x devices in addition to granular firewalls managed by the HSM for developers to design the most secure systems.

The Real-Time Control Subsystem (CONTROLSS) is a revolutionary subsystem integrated into the device. CONTROLSS contains multiple digital and analog control peripherals including: ADC, CMPSS, EPWM, ECAP, and EQEP, among others to enable efficient execution of critical sense/process/actuate real-time signal chain control loops. The integrated crossbar (XBAR) infrastructure enables flexible configuration and routing of external signals to internal ports and internal signals to external pins.

The PRU-ICSS in AM261x provides the flexible industrial communications capability necessary to run TSN, EtherCAT®, PROFINET®, Ethernet/IP™, or for standard Ethernet connectivity and custom I/O interfacing. The PRU also enables additional interfaces in the SoC including sigma delta decimation filters and absolute encoder interfaces. The CPSW interface also provides two standard Ethernet ports.

TI provides a complete set of microcontroller software and development tools for the AM261x family of microcontrollers in addition to multiple pin-to-pin compatible devices for scalability and ease of use.

7.2 Processor Subsystems

7.2.1 Arm Cortex-R5F Subsystem

The R5FSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for dual-core (split) or lockstep modes of operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC. The device has one R5FSS module for a total possible 2x functional cores (dual-core mode) or 1x functional cores (lockstep mode).

Note

The Arm® Cortex®-R5F processor is a Cortex-R5 processor that includes the optional Floating-point Unit (FPU) extension.

For more information, see *R5FSS* section in *Processors and Accelerators* chapter in the device TRM.

8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Device Connection and Layout Fundamentals

8.1.1 External Oscillator

For more information about External Oscillators, see the *Input Clocks/Oscillators* section.

8.1.2 JTAG, EMU, and TRACE

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For recommendations on JTAG, EMU, and TRACE routing, see the Emulation and Trace Headers Technical Reference Manual

8.1.3 Hardware Reference Design and Guidelines

For details regarding creating PCB systems based on the AM261x family of MCU devices, please see AM26x Hardware Design Guidelines. In addition, please see the AM26x Custom PCB System Getting Started Guide.

8.1.4 USB 2.0 Operation

AM261x devices are not compatible with the standard DFU-utility and require a custom TI version of the DFU-Utility provided in the AM261x MCU+ SDK. For more information and installation instructions, please see the dfu-util section of the AM261x MCU+ SDK.

8.2 OSPI Reset

For proper OSPI boot operation in AM261x system designs, it is recommended that the OSPI flash reset signal is generated from the output of an AND gate with PORz/WARMRSTn and OSPI0_RESET_OUT0 as inputs. This method allows the flash device to be reset when the AM261x device is power cycled or through a software reset command. During OSPI boot, the AM261x device boot ROM code configures the GPIO61 pin as OSPI0_RESET_OUT0 and drives the pin low to reset an external flash device. However, the OSPI controller configuration for GPIO61 does not drive the pin high once the flash device has been reset, thus holding the flash device in reset, preventing proper boot. This includes fallback modes of boot which will result in OSPI boot mode getting activated. For more information, refer to the AM261x Errata Document.

For software reset of the external flash device, any GPIO with a dedicated OSPI0_RESET_OUT mux mode can be used, including GPIO61. However, due to the ROM code configuration outlined above, the GPIO61 pin should be gated to prevent signal propagation to the reset logic on boot. AM261x OSPI Reset using Buffered GPIO61 and PORz/WARMRESETn showcases one application of this. For more details on design considerations, please see the AM26x Hardware Design Guide.

Note

Regardless of the GPIO pin used for OSPI0_RESET_OUT0 implementation, it is still recommended that the OSPI flash reset signal is generated from the output of an AND gate with PORz/WARMRSTn and OSPI0_RESET_OUT0 as inputs, such as in AM261x OSPI Reset using OSPI0_REST_OUT0 and PORz/WARMRESETn.

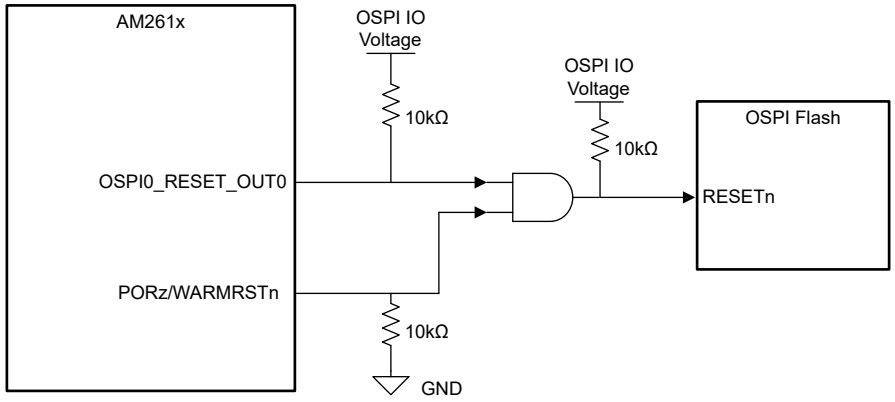


Figure 8-1. AM261x OSPI Reset using OSPI0_REST_OUT0 and PORz/WARMRESETn

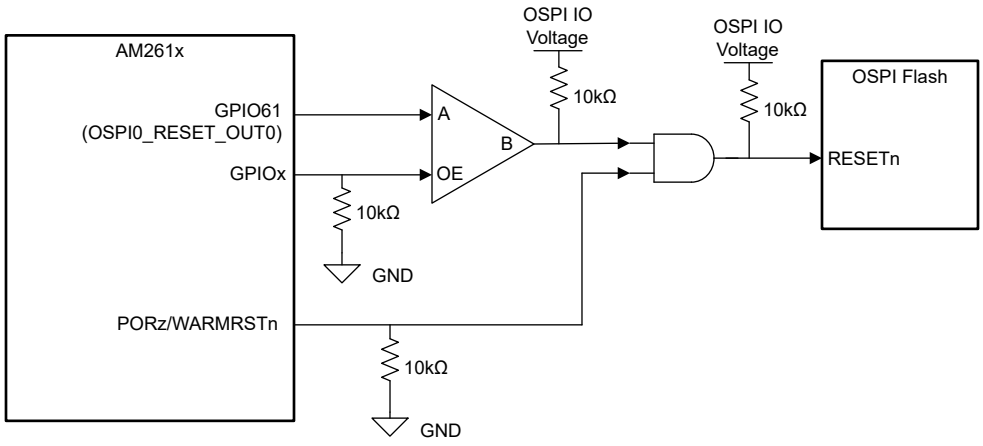


Figure 8-2. AM261x OSPI Reset using Buffered GPIO61 and PORz/WARMRESETn

9 Device and Documentation Support

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microcontrollers (MCUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, XAM2612AOFFHIZFB). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of AM261x devices , see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

9.1.1 Standard Package Symbolization

Note

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

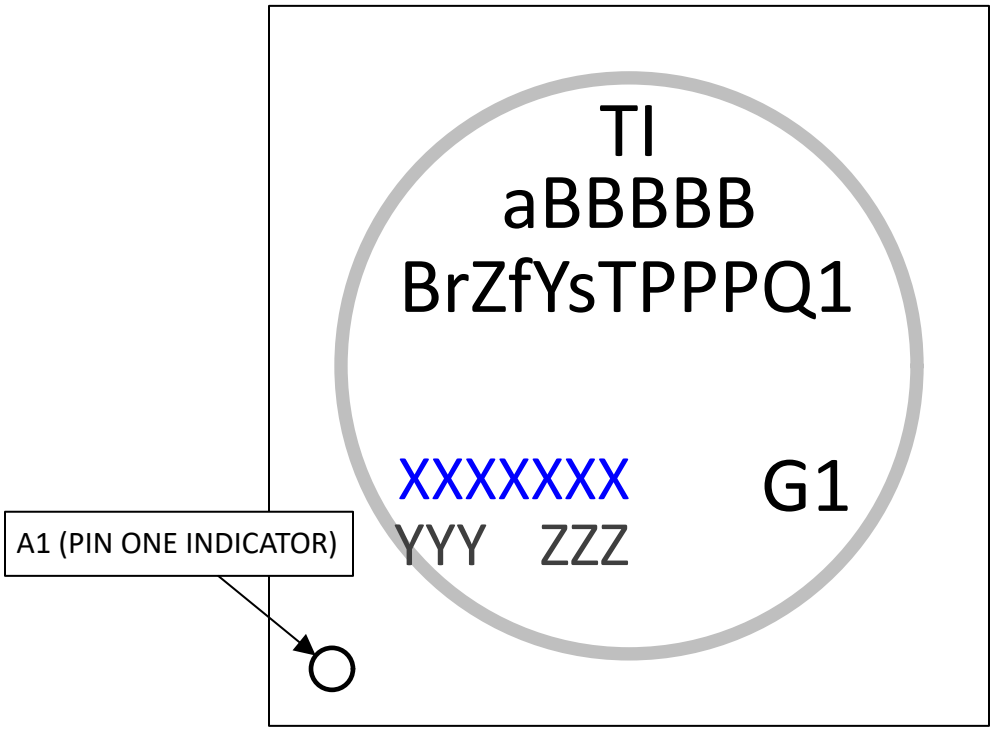


Figure 9-1. Printed Device Reference

9.1.2 Device Naming Convention

Table 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUE	DESCRIPTION
Field Parameter	Field Description	Value	Description
a	Device evolution stage	X	Prototype
		P	Preproduction (production test flow, no reliability data)
		BLANK	Production
BBBBBB	Base production part number	AM2612	2x R5F
		AM2611	1x R5F
r	Device revision	A	Silicon Revision 1.0
Z	Device Operating Performance Points	L	See *Operating Performance Points*.
		O	
		P	
f	Features(see Package Comparison)	D	PRU-ICSS + CAN-FD Supported
		E	PRU-ICSS + EtherCAT HW Accelerator + CAN-FD Supported
		F	PRU-ICSS + EtherCAT HW Accelerator + CAN-FD Supported + Pre-integrated Stacks Enabled
Y	Functional Safety	G	Non-Functional Safety
		F	Functional Safety
s	Security	G	Non-security
		1-9	Dummy key devices
		H-Z	Production key HS devices
T	Temp (Junction)	I	-40°C to 125°C (Extended Industrial)
		M	-40°C to 150°C (Extended Automotive)
PPP	Package Designator	ZCZ	ZCZ NFBGA-N324 (15mm × 15mm) Package
		ZFG	ZFG NFBGA-N304 (13.25mm × 13.25mm) Package
		ZEJ	ZEJ NFBGA-N256 (13mm × 13mm) Package
		ZNC	ZNC NFBGA-N293 (10mm × 10mm) Package
Q1	Automotive Designator and Max Junction Temperature	Q1	Auto Qualified (AEC-Q100)
		BLANK	Standard
XXXXXXX			Lot Trace Code (LTC)
YYY			Production Code; For TI use only
O			Pin one designator
G1			Green package designator

9.2 Tools and Software

The following products support development for AM261x platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

SysConfig-PinMux Tool The SysConfig-PinMux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI Embedded Processor devices. The tool can be used to automatically calculate the optimal pinmux configuration to satisfy entered system requirements. The tool will generate output C header/code files that can be imported into software development kits (SDKs) and used to configure customer's software to meet custom hardware requirements.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents are provided to describe the AM261x device.

AM261x Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the AM261x family of devices.

AM261x TRM Register Addendum Details the memory mapped register information for each peripheral and subsystem in the AM261x family of devices.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

Ethernet/IP™ is a trademark of ODVA, INC..
CoreSight™ is a trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
Code Composer Studio™ and TI E2E™ are trademarks of Texas Instruments.
Arm® and Cortex® are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.
EtherCAT® is a registered trademark of Beckhoff Automation GmbH.
PROFINET® is a registered trademark of PROFINET International.
IO-Link® is a registered trademark of PROFIBUS Nutzerorganisation e.V. eingetragener verein (e.v.) FED REP GERMANY.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from November 7, 2024 to April 30, 2025 (from Revision A (November 2024) to Revision B (April 2025)) **Page**

- (SDFM Signal Descriptions): Added table notes ... 75
- (SPI Signal Descriptions): Moved section below SDFM Signal Descriptions ... 76
- (SPI Signal Descriptions): Removed SOP pin notation from SPI0_CLK and SPI0_D0 signal descriptions ... 76
- (Boot Mode Signal Descriptions): Updated descriptions to reflect correct SOP pins ... 77
- (VMON Signal Description): Added table note ... 79
- (No Connection Description): Add table note ... 79
- (USB0 Signal Descriptions): Moved Section below UART Signal Descriptions ... 81
- (Pin Connectivity Requirements): Added Pin Connectivity Requirements for AM261x ... 83
- (Specifications): Added in Electrostatic Discharge, Power-On Hours, Operating Performance Points, VPP Specifications, Timing and Switching Characteristics, and Decoupling Capacitor Requirements sections ... 84
- (Recommended Operation Conditions): Update VDD, VDDAR1, VDDAR2, and VDDAR3 line items to reflect required voltages dependent on R5F core frequency ... 84
- (Electrical Characteristics): Added ADC, CMPSSA, DAC, PMU, and Safety Comparison sections ... 89
- (Thermal Resistance Characteristics): Added Thermal Resistance Characteristics for all four package types ... 97
- (Detailed Description - Overview): Changed shared TCM from "256KB" to "512KB" ... 186
- (Hardware Reference Design and Guidelines): Added link to Hardware Design Guide and Custom PCB System Getting Started Guide ... 188
- (USB 2.0 Operation): Added section ... 188
- (OSPI Reset): Added section for OSPI0_REST_OUT0 ... 189
- (Standard Package Symbolization): Added Standard Package Symbolization section ... 191
- (Device Naming Convention): Removed Special Features row ... 192
- (Device Naming Convention): Added 'L' and 'P' speed grades ... 192

Changes from September 1, 2024 to November 6, 2024 (from Revision * (September 2024) to Revision A (November 2024)) **Page**

- Added Specifications, Detailed description, Applications, Implementations and Layout sections ... 1
- Updated Features section to mention ECC for OCSRAM, EMAC support in PRU-ICSS, TSN in CPSW ... 1
- Updated Device Naming Convention and Package comparison tables ... 8
- Updated Device junction temperature for Extended Industrial Temperature ... 8

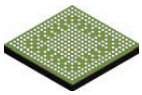
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the Packaging information website.

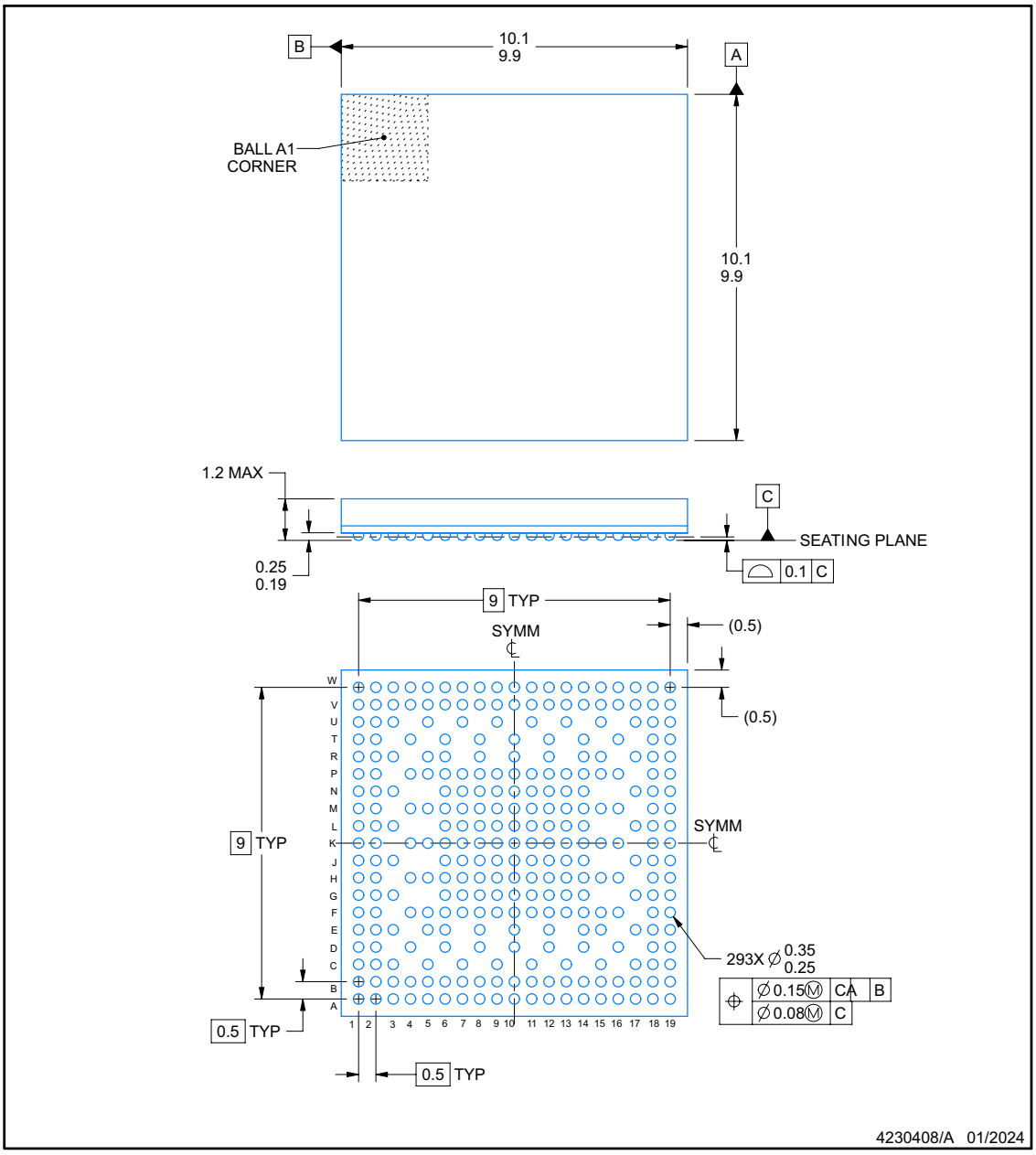
PACKAGE OUTLINE

ZNC0293A



NFBGA - 1.2 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

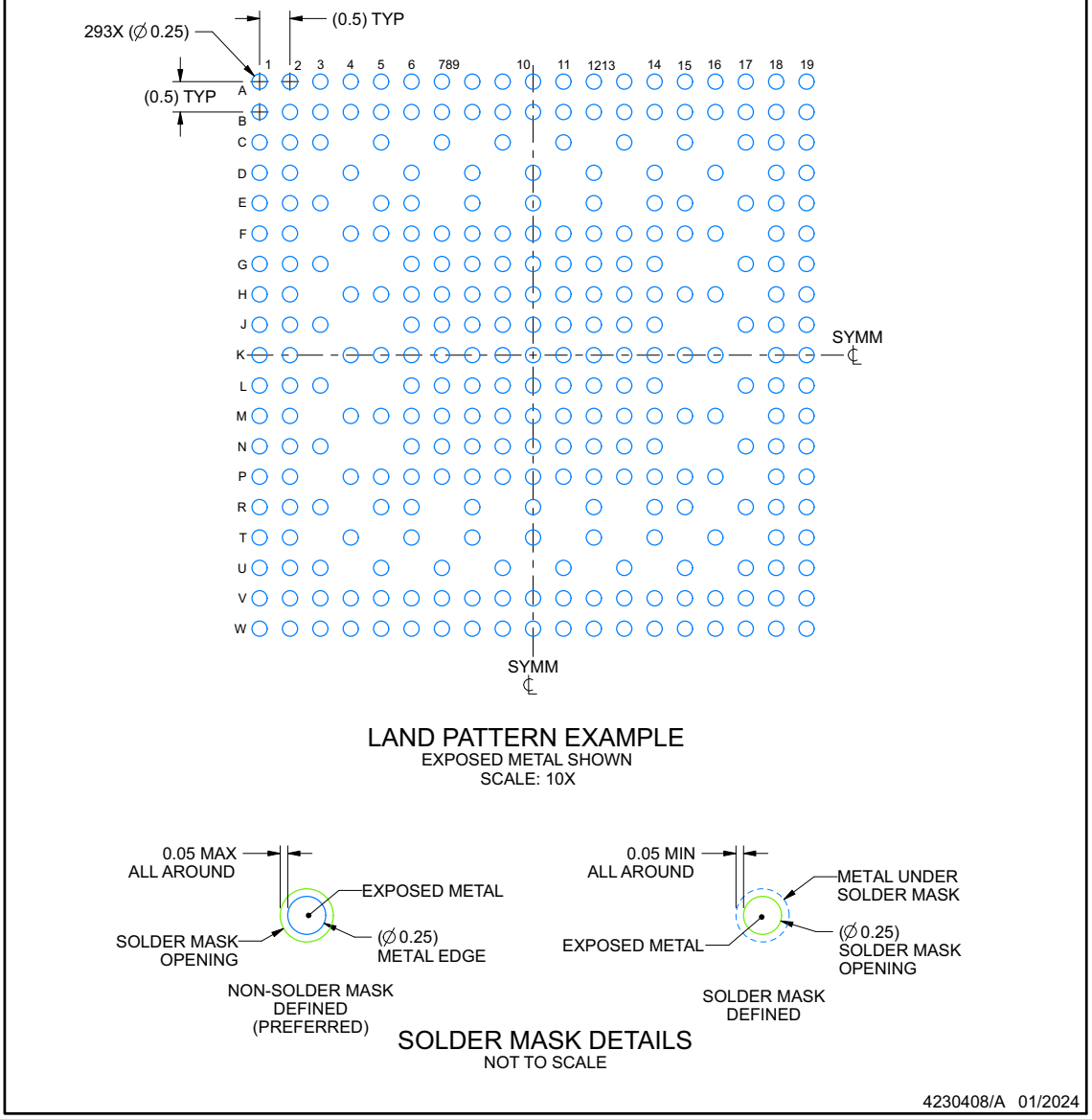
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ZNC0293A

NFBGA - 1.2 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

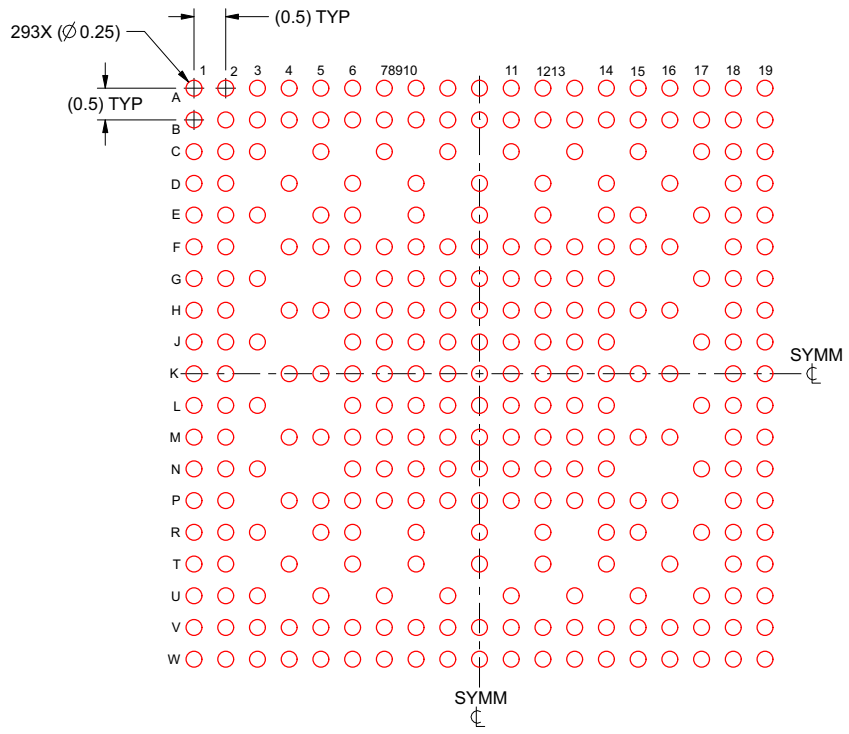
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZNC0293A

NFBGA - 1.2 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 10X

4230408/A 01/2024

NOTES: (continued)

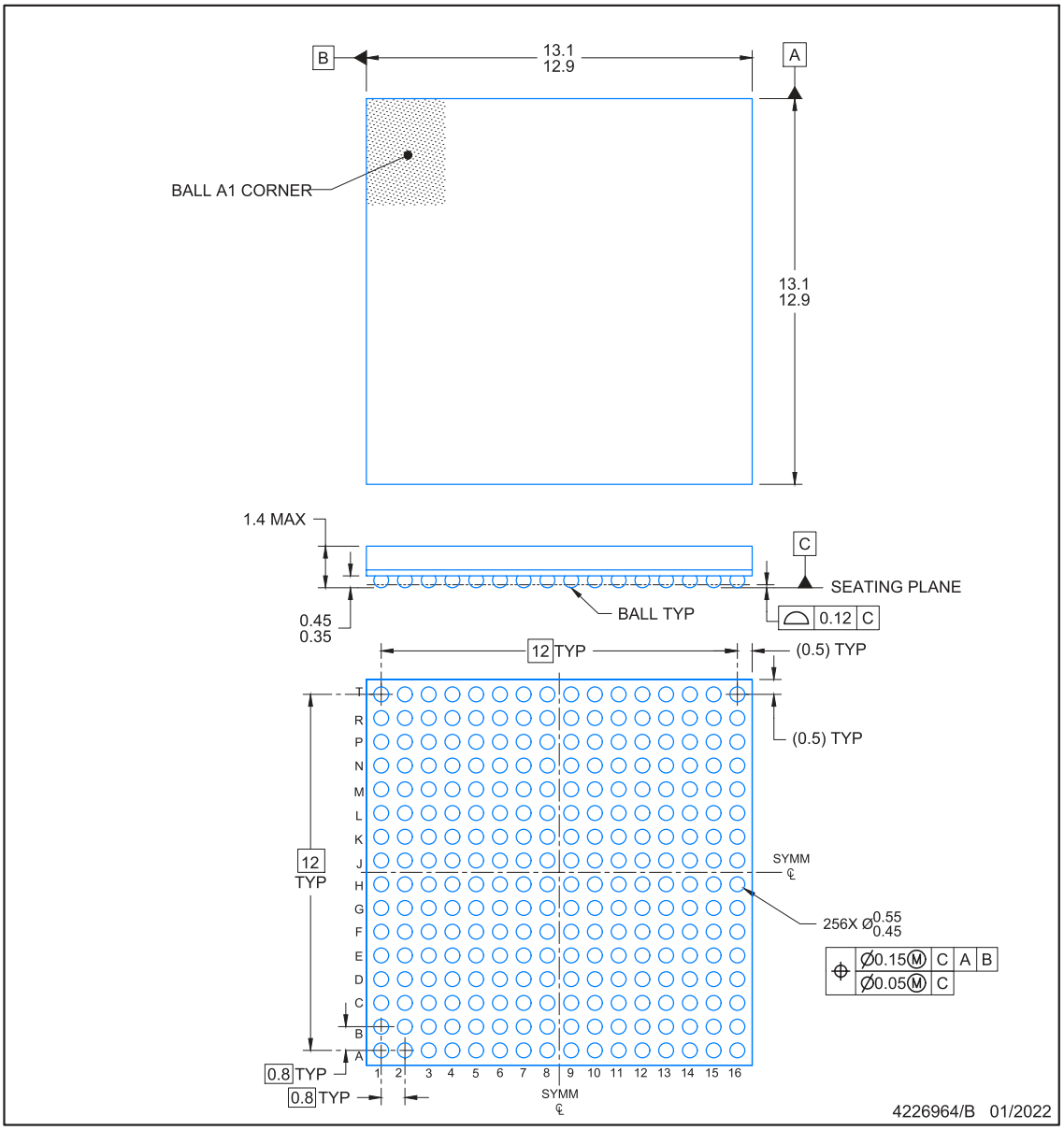
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZEJ0256A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

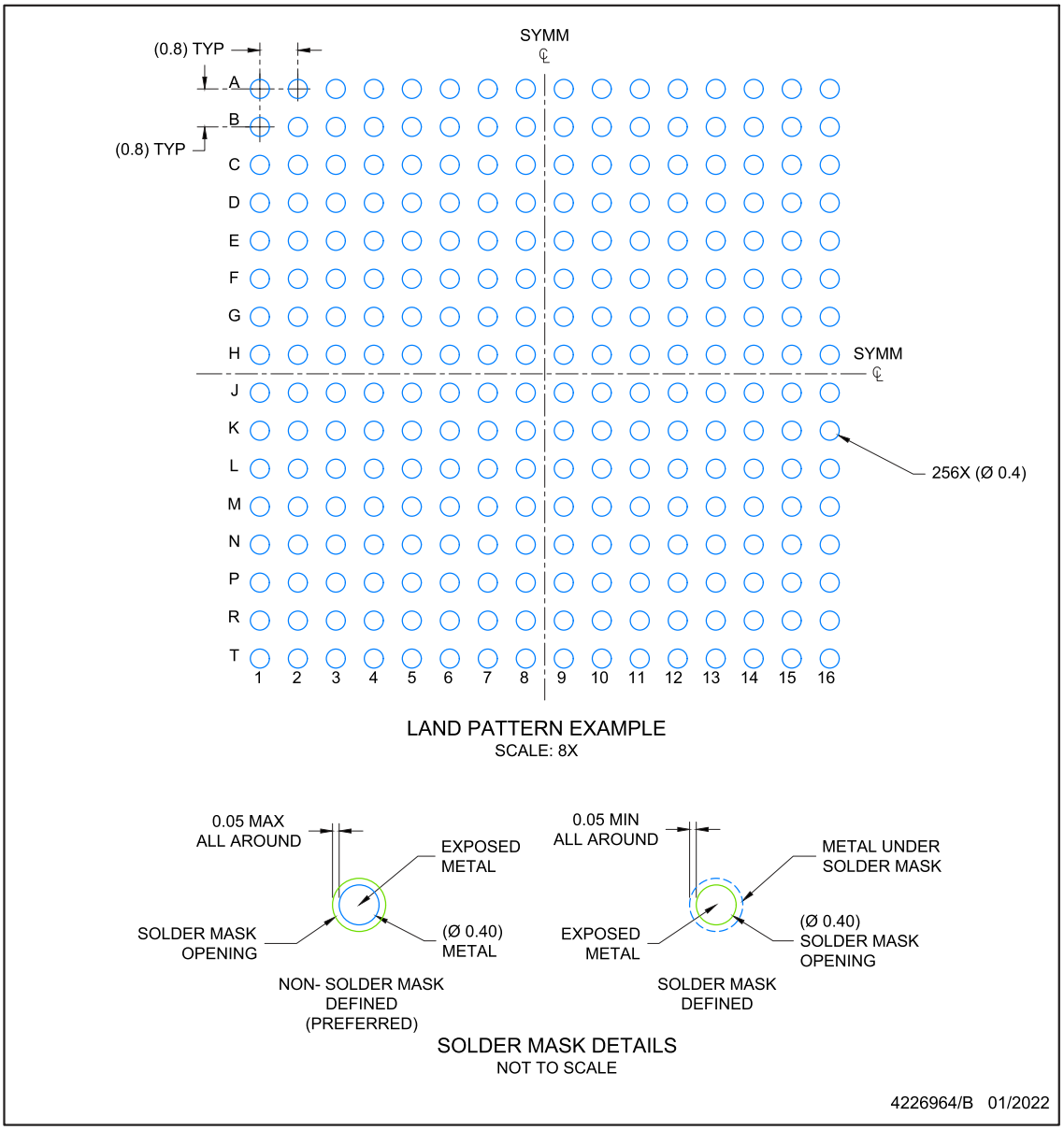
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ZEJ0256A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



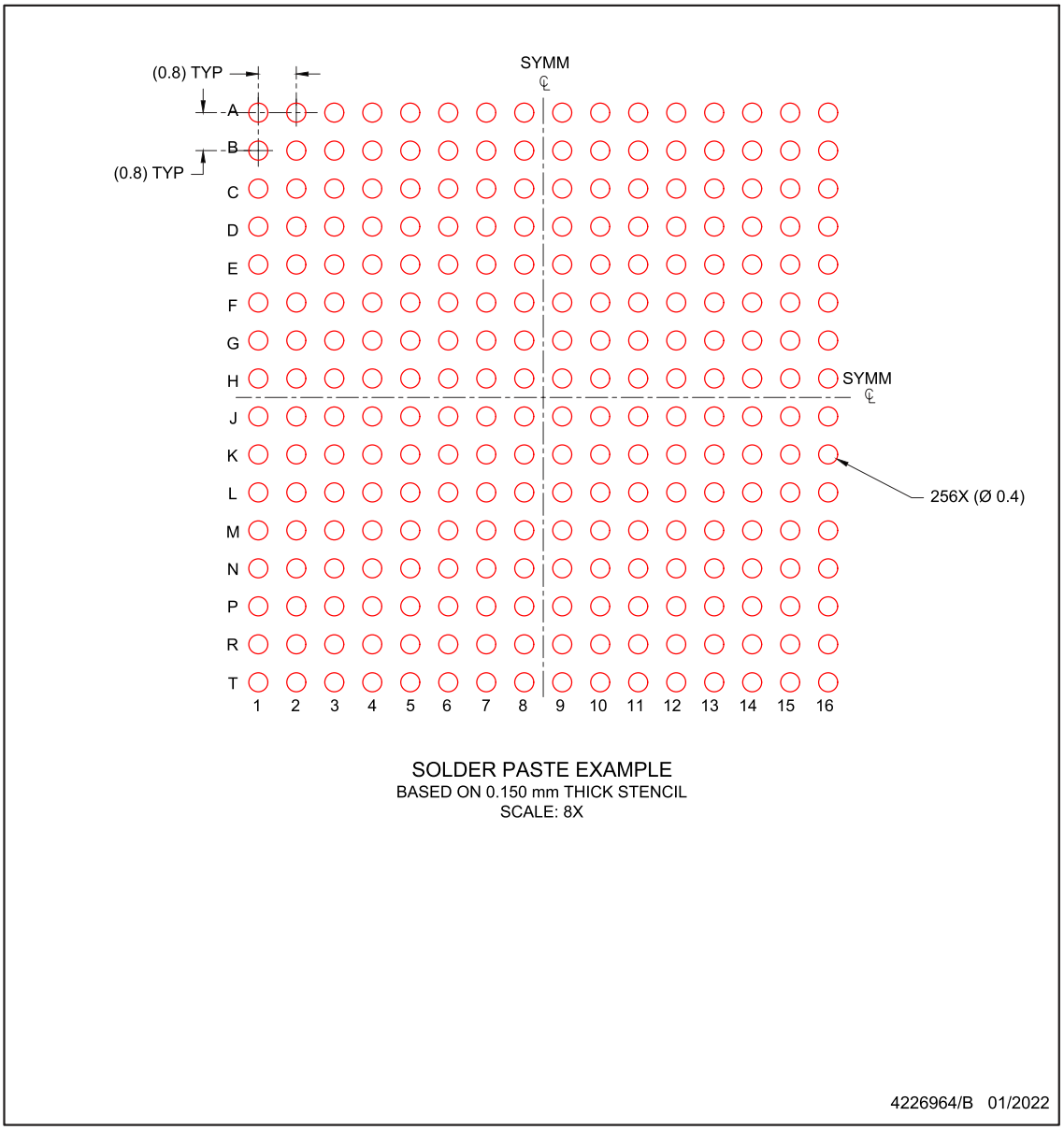
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

ZEJ0256A — **NFBGA - 1.4 mm max height**

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

4226964/B 01/2022

NOTES: (continued)

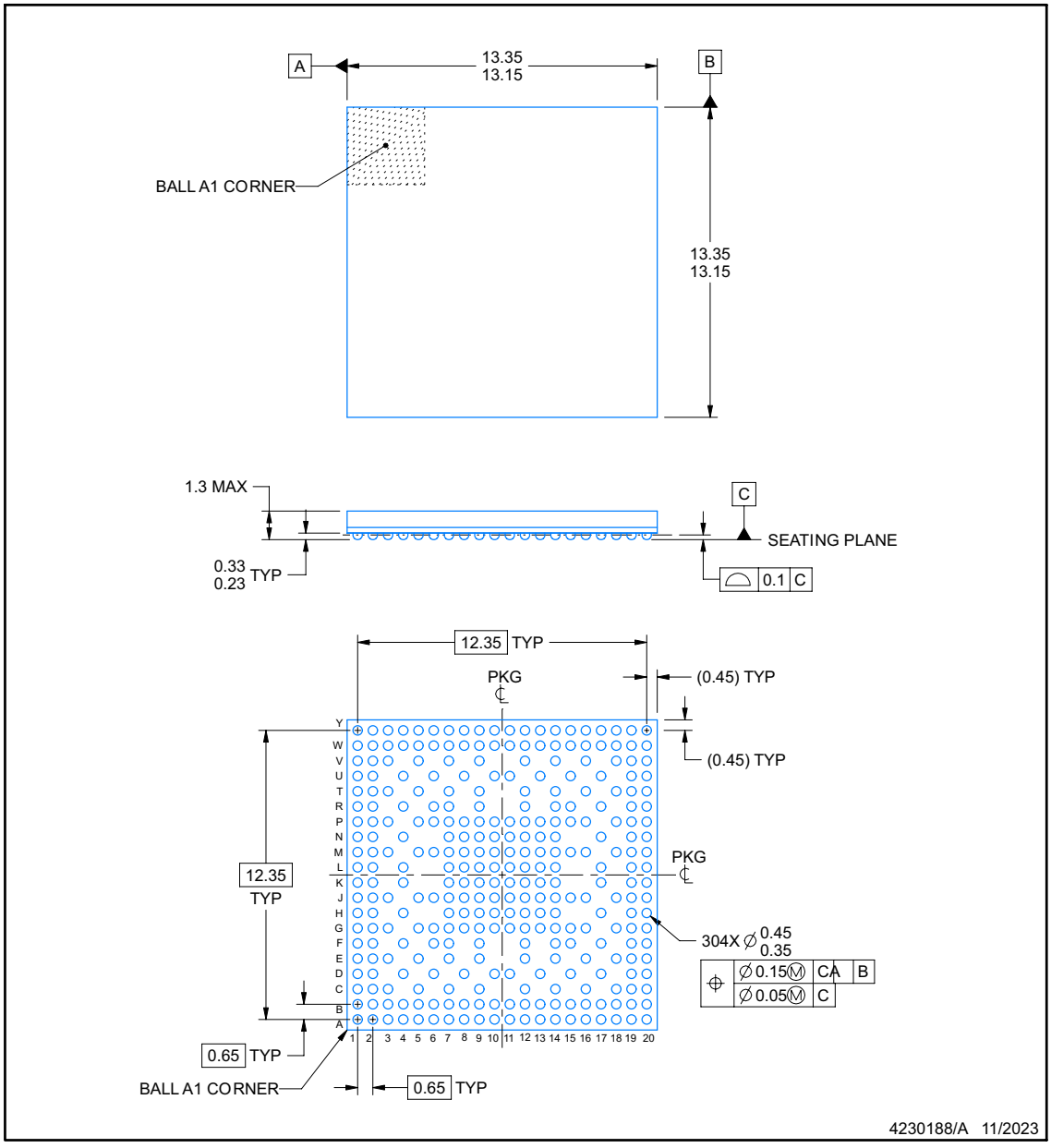
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZFG0304A

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

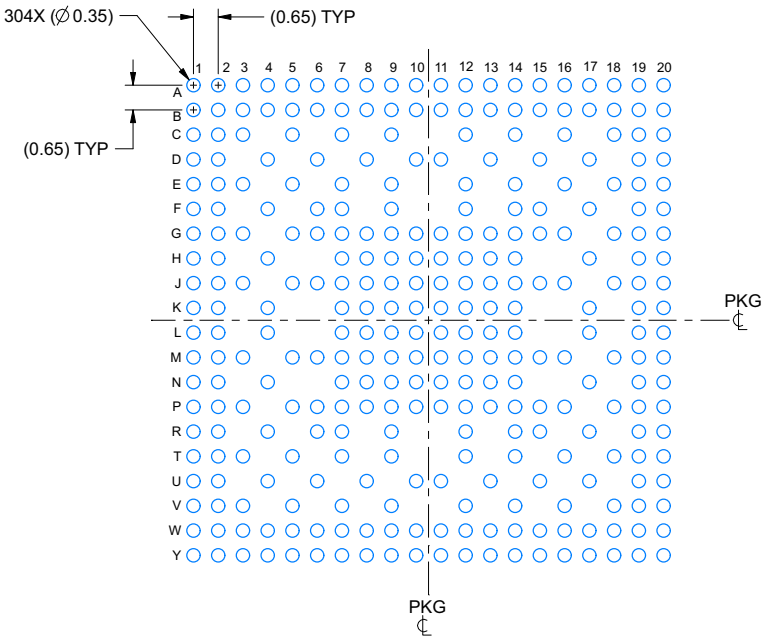
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

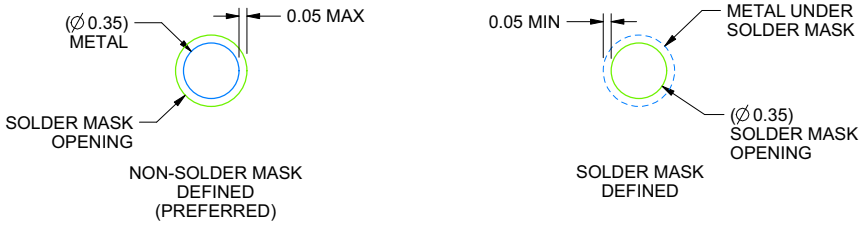
ZFG0304A

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

4230188/A 11/2023

NOTES: (continued)

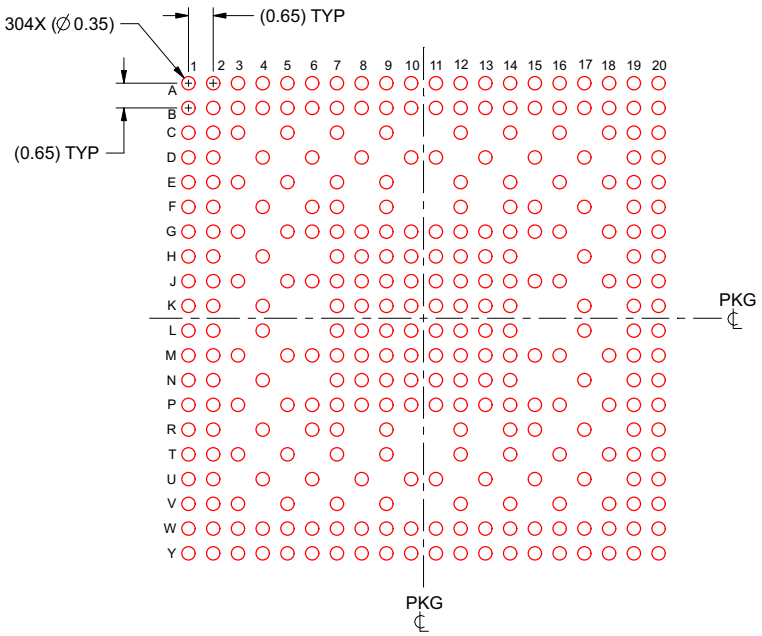
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZFG0304A

NFBGA - 1.3 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4230188/A 11/2023

NOTES: (continued)

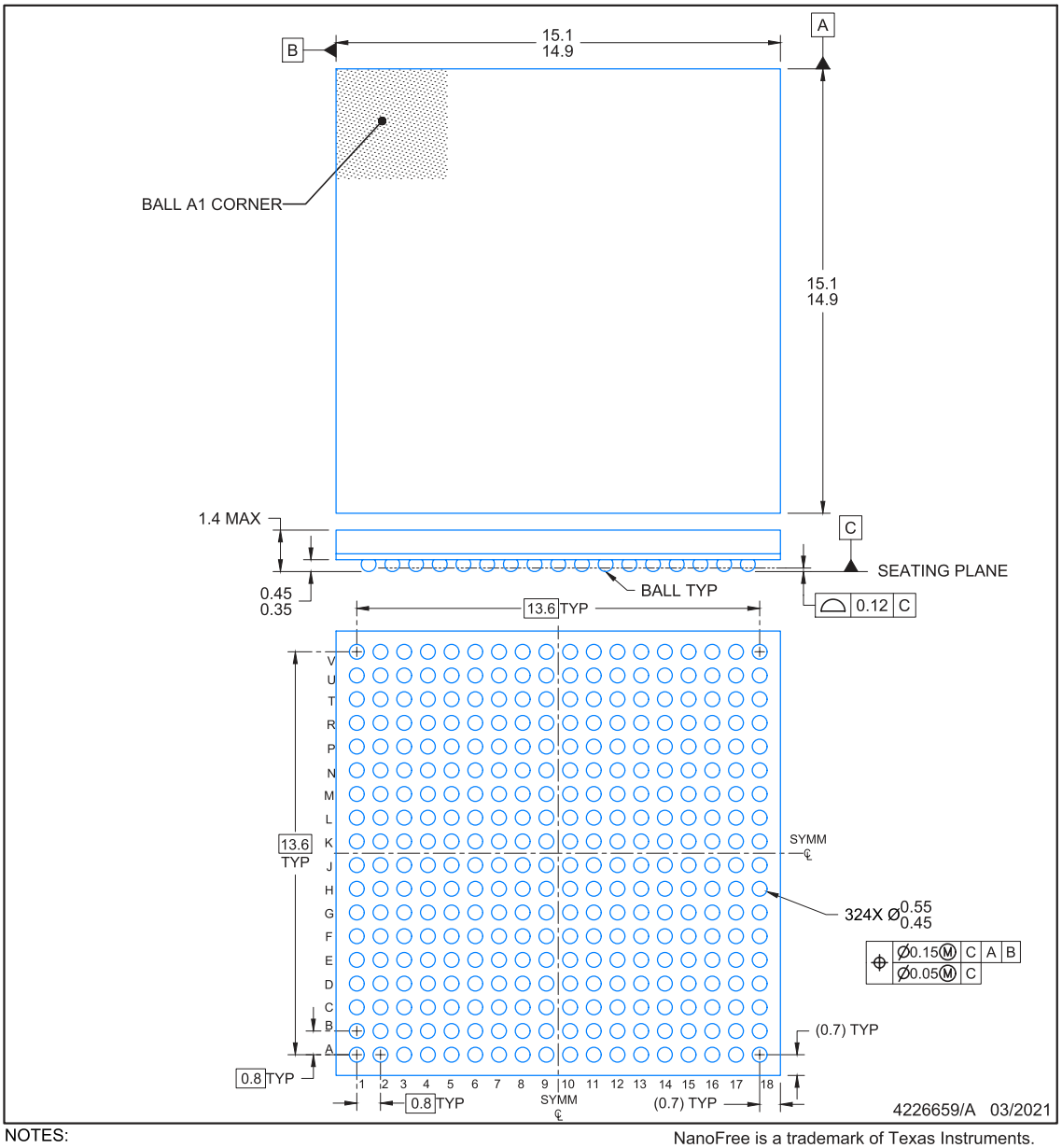
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ZCZ0324A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES:

NanoFree is a trademark of Texas Instruments.

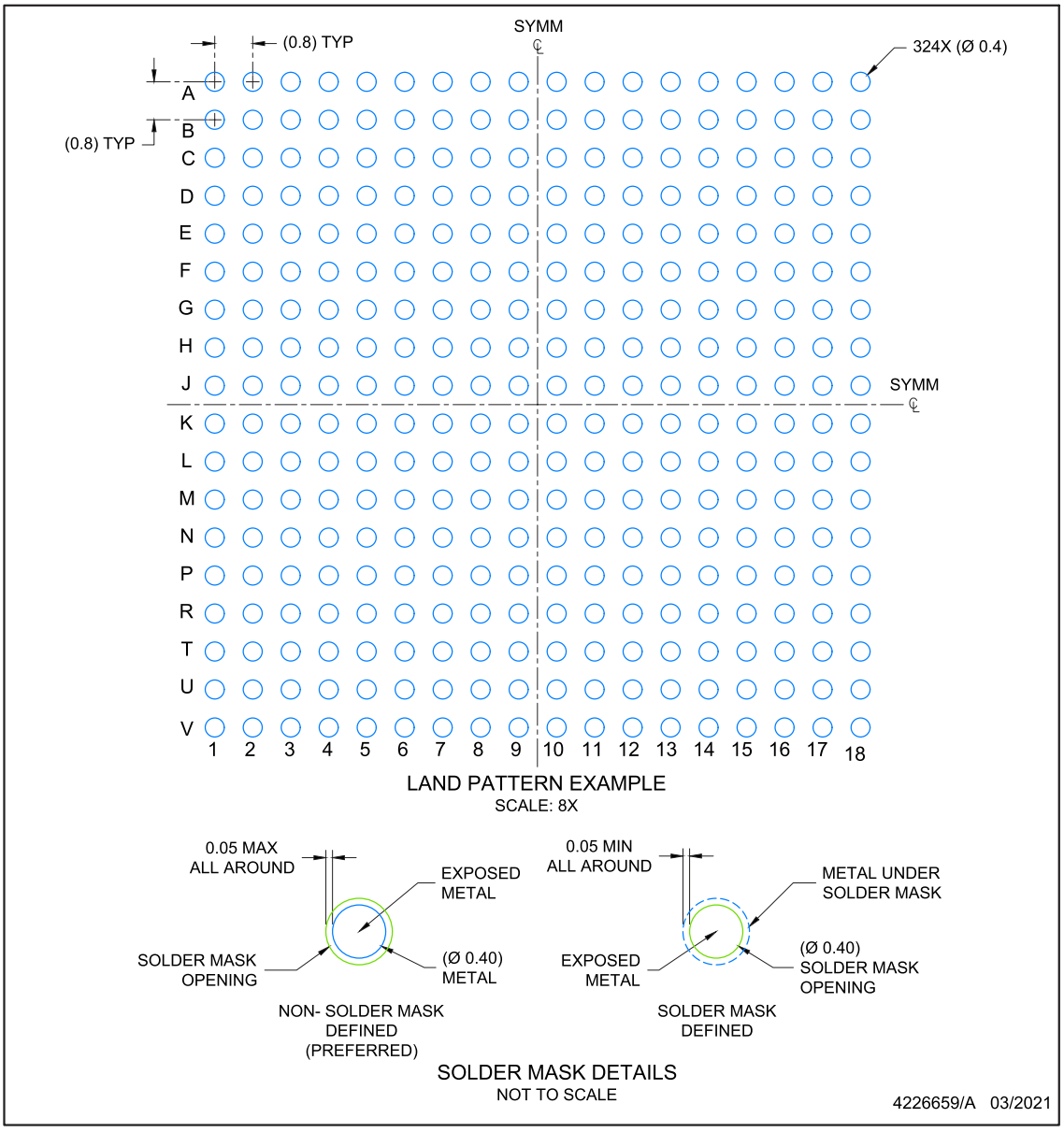
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

ZCZ0324A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

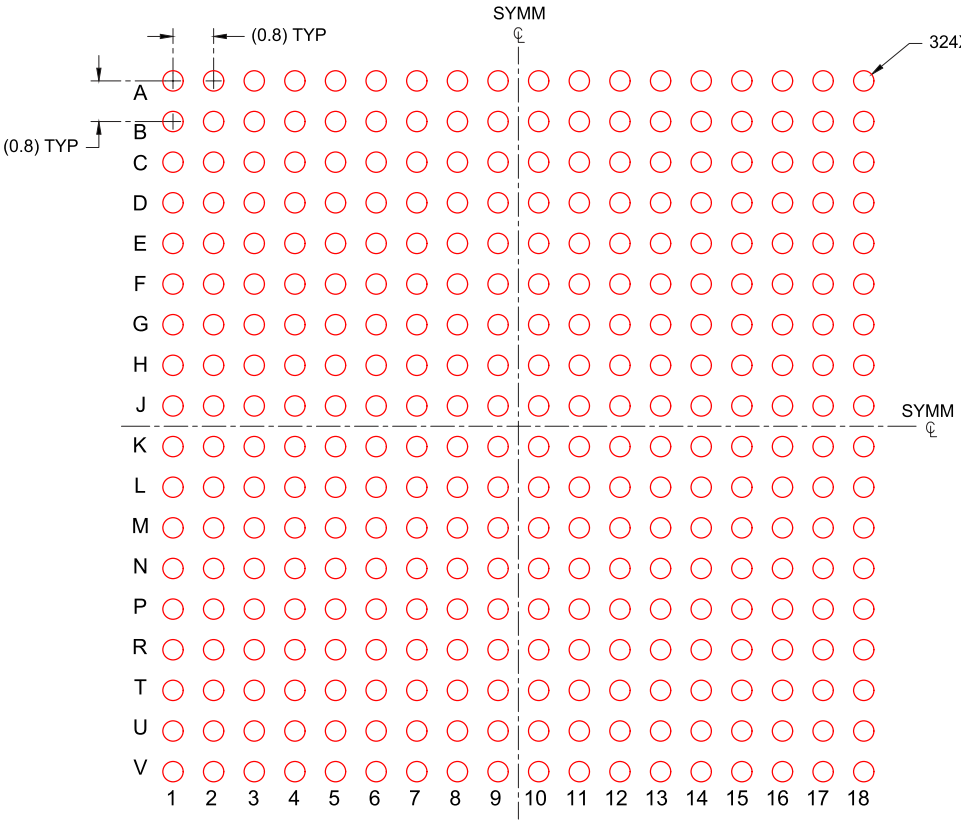
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

ZCZ0324A

NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.150 mm THICK STENCIL
SCALE: 8X

4226659/A 03/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AM2612AOFFHIZFGR	Active	Production	null (null) |	1000 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	AM261 2AOFFHIZFG 508
XAM2612AOFFHIZFG	Active	Preproduction	NFBGA (ZFG) | 304	119 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 125	
XAM2612AOFFHIZFG.A	Active	Preproduction	NFBGA (ZFG) | 304	119 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 125	
XAM2612AOFFHIZFG.B	Active	Preproduction	NFBGA (ZFG) | 304	119 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265