

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

High-speed backplane operation is a direct result of the improved OEC™ circuitry and high drive that has been designed and tested into the VME64x backplane model. The B-port I/Os are optimized for driving large capacitive loads and include pseudo-ETL input thresholds ($\frac{1}{2} V_{CC} \pm 50 \text{ mV}$) for increased noise immunity. These specifications support the 2eVME protocols in VME64x (ANSI/VITA 1.1) and 2eSST protocols in VITA 1.5. With proper design of a 21-slot VME system, a designer can achieve 320-Mbyte transfer rates on linear backplanes and, possibly, 1-Gbyte transfer rates on the VME320 backplane.

All inputs and outputs are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.

Active bus-hold circuitry holds unused or undriven 3A-port inputs at a valid logic state. Bus-hold circuitry is not provided on 1A or 2A inputs, any B-port input, or any control input. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for live-insertion applications using I_{off} , power-up 3-state, and BIAS V_{CC} . The I_{off} circuitry prevents damaging current to backflow through the device when it is powered off/on. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

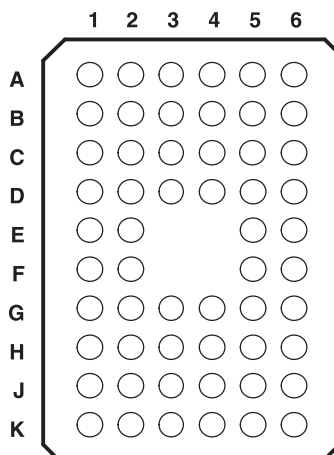
When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, output-enable (\overline{OE} and $\overline{OE}BY$) inputs should be tied to V_{CC} through a pullup resistor and output-enable (OEAB) inputs should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the drive capability of the device connected to this input.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------------|-----------------------------|---------------|-----------------------|------------------|
| 0°C to 85°C | BGA MicroStar™ Junior – ZQL | Tape and reel | SN74VMEH22501ZQLR | VK501 |
| | TSSOP – DGG | Tape and reel | SN74VMEH22501DGGR | VMEH22501 |
| | TVSOP – DGV | Tape and reel | SN74VMEH22501DGVR | VK501 |
| | VFBGA – GQL | Tape and reel | SN74VMEH22501GQLR | VK501 |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/sc/packaging.

**GQL OR ZQL PACKAGE
(TOP VIEW)**



TERMINAL ASSIGNMENTS⁽¹⁾

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|--------------------|--------------------|-----------------|-----------------|----------------------|-----------------|
| A | $\overline{1OEBY}$ | NC | NC | NC | NC | 1OEAB |
| B | 1Y | 1A | GND | GND | V _{CC} | 1B |
| C | 2Y | 2A | V _{CC} | V _{CC} | BIAS V _{CC} | 2B |
| D | 3A1 | $\overline{2OEBY}$ | GND | GND | 2OEAB | 3B1 |
| E | 3A2 | LE | | | V _{CC} | 3B2 |
| F | 3A3 | \overline{OE} | | | V _{CC} | 3B3 |
| G | 3A4 | CLKBA | GND | GND | CLKAB | 3B4 |
| H | 3A5 | 3A6 | V _{CC} | V _{CC} | 3B6 | 3B5 |
| J | 3A7 | 3A8 | GND | GND | 3B8 | 3B7 |
| K | DIR | NC | NC | NC | NC | V _{CC} |

(1) NC - No internal connection

FUNCTIONAL DESCRIPTION

The SN74VMEH22501 is a high-drive (–48/64 mA), 8-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or flip-flop modes. Data transmission is true logic. The device is uniquely partitioned as 8-bit UBT transceivers with two integrated 1-bit three-wire bus transceivers.

Functional Description for Two 1-Bit Bus Transceivers

The OEAB inputs control the activity of the 1B or 2B port. When OEAB is high, the B-port outputs are active. When OEAB is low, the B-port outputs are disabled.

Separate 1A and 2A inputs and 1Y and 2Y outputs provide a feedback path for control and diagnostics monitoring. The $\overline{\text{OEBY}}$ inputs control the 1Y or 2Y outputs. When $\overline{\text{OEBY}}$ is low, the Y outputs are active. When $\overline{\text{OEBY}}$ is high, the Y outputs are disabled.

The $\overline{\text{OEBY}}$ and OEAB inputs can be tied together to form a simple direction control where an input high yields A data to B bus and an input low yields B data to Y bus.

1-BIT BUS TRANSCEIVER FUNCTION TABLE

| INPUTS | | OUTPUT | MODE |
|--------|--------------------------|----------------------------------|--------------------------------|
| OEAB | $\overline{\text{OEBY}}$ | | |
| L | H | Z | Isolation |
| H | H | A data to B bus | True driver |
| L | L | B data to Y bus | |
| H | L | A data to B bus, B data to Y bus | True driver with feedback path |

Functional Description for 8-Bit UBT Transceiver

The 3A and 3B data flow in each direction is controlled by the $\overline{\text{OE}}$ and direction-control (DIR) inputs. When $\overline{\text{OE}}$ is low, all 3A- or 3B-port outputs are active. When $\overline{\text{OE}}$ is high, all 3A- or 3B-port outputs are in the high-impedance state.

FUNCTION TABLE

| INPUTS | | OUTPUT |
|------------------------|-----|-------------------|
| $\overline{\text{OE}}$ | DIR | |
| H | X | Z |
| L | H | 3A data to 3B bus |
| L | L | 3B data to 3A bus |

The UBT transceiver functions are controlled by latch-enable (LE) and clock (CLKAB and CLKBA) inputs. For 3A-to-3B data flow, the UBT operates in the transparent mode when LE is high. When LE is low, the 3A data is latched if CLKAB is held at a high or low logic level. If LE is low, the 3A data is stored in the latch/flip-flop on the low-to-high transition of CLKAB.

The UBT transceiver data flow for 3B to 3A is similar to that of 3A to 3B, but uses CLKBA.

Table 1. UBT TRANSCEIVER FUNCTION TABLE⁽¹⁾

| INPUTS | | | | OUTPUT 3B | MODE |
|-----------------|----|-------|----|-------------------------------|----------------------------|
| \overline{OE} | LE | CLKAB | 3A | | |
| H | X | X | X | Z | Isolation |
| L | L | H | X | B ₀ ⁽²⁾ | Latched storage of 3A data |
| L | L | L | X | B ₀ ⁽³⁾ | |
| L | H | X | L | L | True transparent |
| L | H | X | H | H | |
| L | L | ↑ | L | L | Clocked storage of 3A data |
| L | L | ↑ | H | H | |

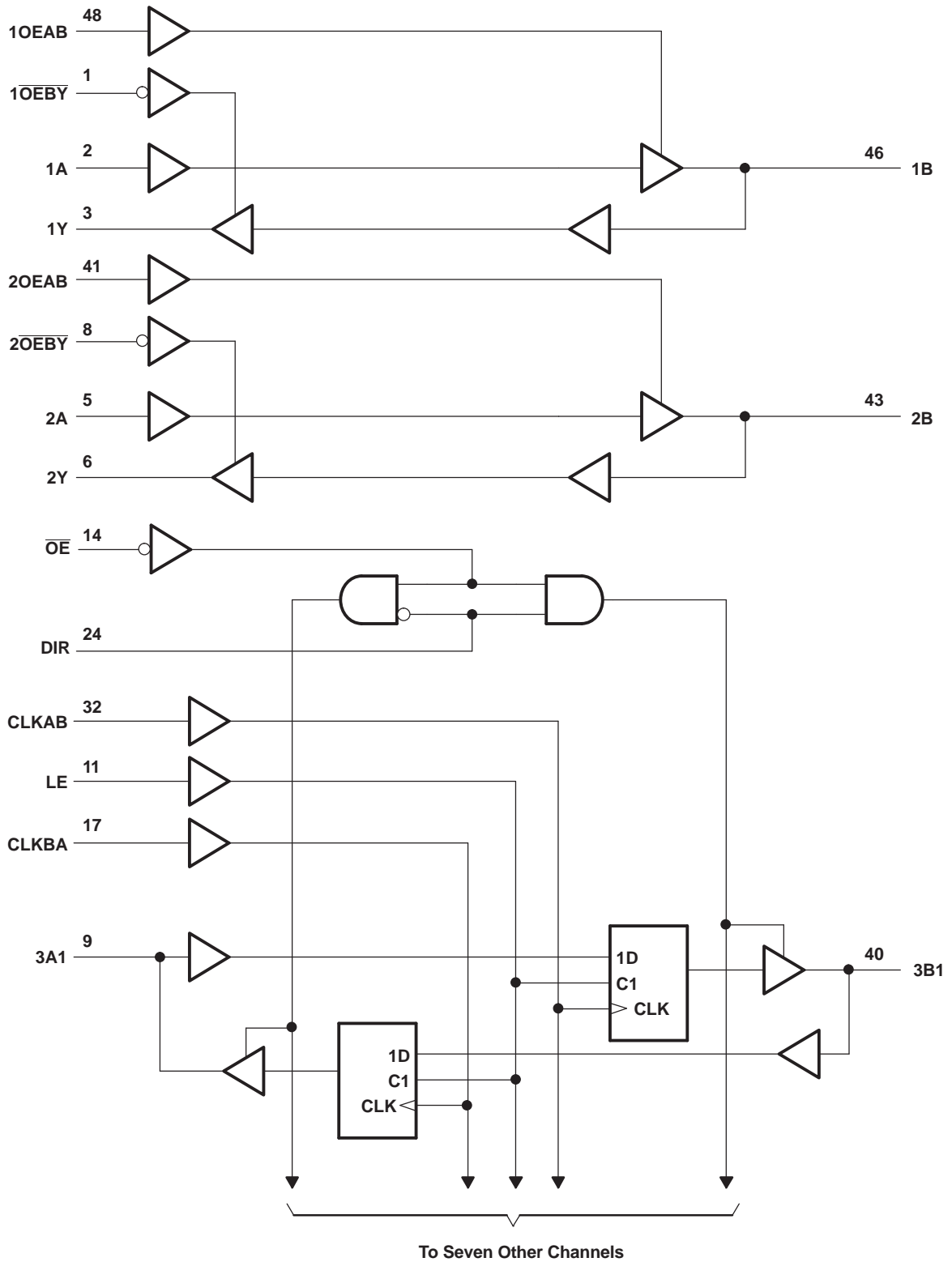
- (1) 3A-to-3B data flow is shown; 3B-to-3A data flow is similar, but uses CLKBA.
 (2) Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LE went low
 (3) Output level before the indicated steady-state input conditions were established

The UBT transceiver can replace any of the functions shown in [Table 2](#).

Table 2. SN74VMEH22501 UBT Transceiver Replacement Functions

| FUNCTION | 8 BIT |
|--|------------------|
| Transceiver | '245, '623, '645 |
| Buffer/driver | '241, '244, '541 |
| Latched transceiver | '543 |
| Latch | '373, '573 |
| Registered transceiver | '646, '652 |
| Flip-flop | '374, '574 |
| SN74VMEH22501 UBT transceiver replaces all above functions | |

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DGV packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|-----------------------------|---|--------------------------------------|------|----------------|------|
| V_{CC} , BIAS V_{CC} | Supply voltage range | -0.5 | 4.6 | V | |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 7 | V | |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 7 | V | |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾ | 3A port or Y output | -0.5 | $V_{CC} + 0.5$ | V |
| | | B port | -0.5 | 4.6 | |
| I_O | Output current in the low state | 3A port or Y output | | 50 | mA |
| | | B port | | 100 | |
| I_O | Output current in the high state | 3A port or Y output | | -50 | mA |
| | | B port | | -100 | |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$, B port | | -50 | mA |
| θ_{JA} | Package thermal impedance ⁽³⁾ | DGG package | | 70 | °C/W |
| | | DGV package | | 58 | |
| | | GQL/ZQL package | | 42 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions^{(1) (2)}

| | | MIN | NOM | MAX | UNIT |
|-----------------------------|------------------------------------|--------------------------|----------------------|----------------------|------|
| V_{CC} , BIAS V_{CC} | Supply voltage | 3.15 | 3.3 | 3.45 | V |
| V_I | Input voltage | Control inputs or A port | | V_{CC} | V |
| | | B port | | V_{CC} | |
| V_{IH} | High-level input voltage | Control inputs or A port | 2 | | V |
| | | B port | $0.5 V_{CC} + 50$ mV | | |
| V_{IL} | Low-level input voltage | Control inputs or A port | | 0.8 | V |
| | | B port | | $0.5 V_{CC} - 50$ mV | |
| I_{IK} | Input clamp current | | | -18 | mA |
| I_{OH} | High-level output current | 3A port and Y output | | -12 | mA |
| | | B port | | -48 | |
| I_{OL} | Low-level output current | 3A port and Y output | | 12 | mA |
| | | B port | | 64 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 20 | | | μs/V |
| T_A | Operating free-air temperature | 0 | | 85 | °C |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS $V_{CC} = 3.3$ V first, I/O second, and $V_{CC} = 3.3$ V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control inputs can be connected at any time, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.

Electrical Characteristics

over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--------------------------------|-------------------------------------|--|--------------------------------------|----------------|--------------------|----------|--|
| V_{IK} | | $V_{CC} = 3.15\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| V_{OH} | 3A port, any B ports, and Y outputs | $V_{CC} = 3.15\text{ V to }3.45\text{ V}$, | $I_{OH} = -100\text{ }\mu\text{A}$ | $V_{CC} - 0.2$ | | | V |
| | 3A port and Y outputs | $V_{CC} = 3.15\text{ V}$ | $I_{OH} = -6\text{ mA}$ | 2.4 | | | |
| | | | $I_{OH} = -12\text{ mA}$ | 2 | | | |
| | Any B port | $V_{CC} = 3.15\text{ V}$ | $I_{OH} = -24\text{ mA}$ | 2.4 | | | |
| | | | $I_{OH} = -48\text{ mA}$ | 2 | | | |
| V_{OL} | 3A port, any B ports, and Y outputs | $V_{CC} = 3.15\text{ V to }3.45\text{ V}$, | $I_{OL} = 100\text{ }\mu\text{A}$ | | | 0.2 | V |
| | 3A port and Y outputs | $V_{CC} = 3.15\text{ V}$ | $I_{OL} = 6\text{ mA}$ | | 0.55 | | |
| | | | $I_{OL} = 12\text{ mA}$ | | 0.8 | | |
| | Any B port | $V_{CC} = 3.15\text{ V}$ | $I_{OL} = 24\text{ mA}$ | | 0.4 | | |
| | | | $I_{OL} = 48\text{ mA}$ | | 0.55 | | |
| $I_{OL} = 64\text{ mA}$ | | 0.6 | | | | | |
| I_I | Control inputs, 1A and 2A | $V_{CC} = 3.45\text{ V}$, | $V_I = V_{CC}$ or GND | | | ± 1 | μA |
| | | $V_{CC} = 0$ or 3.45 V , | $V_I = 5.5\text{ V}$ | | | 5 | |
| I_{OZH} ⁽²⁾ | 3A port, any B port, and Y outputs | $V_{CC} = 3.45\text{ V}$, | $V_O = V_{CC}$ or 5.5 V | | | 5 | μA |
| I_{OZL} ⁽²⁾ | 3A port and Y outputs | $V_{CC} = 3.45\text{ V}$, | $V_O = \text{GND}$ | | | -5 | μA |
| | Any B port | | | | | -20 | |
| I_{off} | | $V_{CC} = 0$, BIAS $V_{CC} = 0$, | V_I or $V_O = 0$ to 5.5 V | | | ± 10 | μA |
| I_{BHL} ⁽³⁾ | 3A port | $V_{CC} = 3.15\text{ V}$, | $V_I = 0.8\text{ V}$ | 75 | | | μA |
| I_{BHH} ⁽⁴⁾ | 3A port | $V_{CC} = 3.15\text{ V}$, | $V_I = 2\text{ V}$ | -75 | | | μA |
| I_{BHLO} ⁽⁵⁾ | 3A port | $V_{CC} = 3.45\text{ V}$, | $V_I = 0$ to V_{CC} | 500 | | | μA |
| I_{BHHO} ⁽⁶⁾ | 3A port | $V_{CC} = 3.45\text{ V}$, | $V_I = 0$ to V_{CC} | -500 | | | μA |
| $I_{OZ(PU/PD)}$ ⁽⁷⁾ | | $V_{CC} \leq 1.5\text{ V}$, $V_O = 0.5\text{ V to }V_{CC}$, $V_I = \text{GND}$ or V_{CC} , $\overline{OE} = \text{don't care}$ | | | | ± 10 | μA |
| I_{CC} | | $V_{CC} = 3.45\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND | Outputs high | | | 30 | mA |
| | | | Outputs low | | | 30 | |
| | | | Outputs disabled | | | 30 | |
| I_{CCD} | | $V_{CC} = 3.45\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND, One data input switching at one-half clock frequency, 50% duty cycle | Outputs enabled | | 76 | | $\mu\text{A}/$ clock MHz/ input |
| | | | Outputs disabled | | 19 | | |
| ΔI_{CC} ⁽⁸⁾ | | $V_{CC} = 3.15\text{ V to }3.45\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND | | | | 750 | μA |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.

(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND, then raising it to V_{IL} max.

(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} , then lowering it to V_{IH} min.

(5) An external driver must source at least I_{BHLO} to switch this node from low to high.

(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

(7) High-impedance state during power up or power down

(8) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Electrical Characteristics (continued)

over recommended operating free-air temperature range for A and B ports (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------------|------------------|--|---------|--------------------|-----|------|
| C _i | 1A and 2A inputs | V _I = 3.15 V or 0 | 2.8 | | | pF |
| | Control inputs | | 2.6 | | | |
| C _o | 1Y or 2Y outputs | V _O = 3.15 V or 0 | 5.6 | | | pF |
| C _{io} | 3A port | V _{CC} = 3.3 V, V _O = 3.3 V or 0 | 7.9 | | | pF |
| | Any B port | | 11 12.5 | | | |

Live-Insertion Specifications

over recommended operating free-air temperature range for B port

| PARAMETER | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|---|---|---|-------------------------------|--------------------|-----|------|----|
| I _{CC} (BIAS V _{CC}) | V _{CC} = 0 to 3.15 V, | BIAS V _{CC} = 3.15 V to 3.45 V, I _{O(DC)} = 0 | 5 | | | mA | |
| | V _{CC} = 3.15 V to 3.45 V ⁽²⁾ , | BIAS V _{CC} = 3.15 V to 3.45 V, I _{O(DC)} = 0 | 10 | | | μA | |
| V _O | V _{CC} = 0, | BIAS V _{CC} = 3.15 V to 3.45 V | 1.3 | 1.5 | 1.7 | V | |
| I _O | V _{CC} = 0 | V _O = 0, | BIAS V _{CC} = 3.15 V | | -20 | -100 | μA |
| | | V _O = 3 V, | BIAS V _{CC} = 3.15 V | | 20 | 100 | |

 (1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

 (2) V_{CC} - 0.5 V < BIAS V_{CC}

Timing Requirements for UBT Transceiver

 over recommended operating conditions (unless otherwise noted) (see [Figure 1](#) and [Figure 2](#))

| | | MIN | MAX | UNIT | |
|--------------------|-----------------|-----------------|-----------|------|----|
| f _{clock} | Clock frequency | 120 | | MHz | |
| t _w | Pulse duration | LE high | | 2.5 | ns |
| | | CLK high or low | | 3 | |
| t _{su} | Setup time | 3A before CLK↑ | Data high | 2.1 | ns |
| | | | Data low | 2.2 | |
| | | 3A before LE↓ | CLK high | 2 | |
| | | | CLK low | 2 | |
| | | 3B before CLK↑ | Data high | 2.5 | |
| | | | Data low | 2.7 | |
| 3B before LE↓ | CLK high | 2 | | | |
| | CLK low | 2 | | | |
| t _h | Hold time | 3A after CLK↑ | Data high | 0 | ns |
| | | | Data low | 0 | |
| | | 3A after LE↓ | CLK high | 1 | |
| | | | CLK low | 1 | |
| | | 3B after CLK↑ | Data high | 0 | |
| | | | Data low | 0 | |
| 3B after LE↓ | CLK high | 1 | | | |
| | CLK low | 1 | | | |

Switching Characteristics for Bus Transceiver Function

over recommended operating conditions (unless otherwise noted) (see [Figure 1](#) and [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------|----------------|-----|-----|------|------|
| t_{PLH} | 1A or 2A | 1B or 2B | 5.1 | | 8.9 | ns |
| t_{PHL} | | | 4.5 | | 7.8 | |
| t_{PLH} | 1A or 2A | 1Y or 2Y | 7.2 | | 14.5 | ns |
| t_{PHL} | | | 6.1 | | 13 | |
| t_{PZH} | OEAB | 1B or 2B | 4.6 | | 8.1 | ns |
| t_{PZL} | | | 3.7 | | 7.4 | |
| t_{PHZ} | OEAB | 1B or 2B | 3.3 | | 9.7 | ns |
| t_{PLZ} | | | 1.8 | | 4.8 | |
| t_r | Transition time, B port (10%–90%) | | | 4.3 | | ns |
| t_f | Transition time, B port (90%–10%) | | | 4.3 | | ns |
| t_{PLH} | 1B or 2B | 1Y or 2Y | 1.6 | | 5.6 | ns |
| t_{PHL} | | | 1.6 | | 5.6 | |
| t_{PZH} | \overline{OEBY} | 1Y or 2Y | 1.2 | | 5.6 | ns |
| t_{PZL} | | | 1.8 | | 4.9 | |
| t_{PHZ} | \overline{OEBY} | 1Y or 2Y | 1.4 | | 5.4 | ns |
| t_{PLZ} | | | 1.7 | | 4.5 | |

Switching Characteristics for UBT Transceiver

over recommended operating conditions (unless otherwise noted) (see [Figure 1](#) and [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|-----------|-----------------------------------|----------------|-----|-----|------|------|
| f_{max} | | | 120 | | | MHz |
| t_{PLH} | 3A | 3B | 5.5 | | 9.3 | ns |
| t_{PHL} | | | 4.7 | | 8.3 | |
| t_{PLH} | LE | 3B | 6 | | 10.6 | ns |
| t_{PHL} | | | 4.9 | | 8.7 | |
| t_{PLH} | CLKAB | 3B | 5.8 | | 10.1 | ns |
| t_{PHL} | | | 4.6 | | 8.4 | |
| t_{PZH} | \overline{OE} | 3B | 4.6 | | 9.3 | ns |
| t_{PZL} | | | 3.5 | | 8.5 | |
| t_{PHZ} | \overline{OE} | 3B | 4.8 | | 9.3 | ns |
| t_{PLZ} | | | 2.4 | | 5.7 | |
| t_r | Transition time, B port (10%–90%) | | | 4.3 | | ns |
| t_f | Transition time, B port (90%–10%) | | | 4.3 | | ns |
| t_{PLH} | 3B | 3A | 1.7 | | 5.9 | ns |
| t_{PHL} | | | 1.7 | | 5.9 | |
| t_{PLH} | LE | 3A | 1.7 | | 5.9 | ns |
| t_{PHL} | | | 1.7 | | 5.9 | |
| t_{PLH} | CLKBA | 3A | 1.4 | | 5.5 | ns |
| t_{PHL} | | | 1.4 | | 5.5 | |
| t_{PZH} | \overline{OE} | 3A | 1.5 | | 6.2 | ns |
| t_{PZL} | | | 2.1 | | 5.5 | |
| t_{PHZ} | \overline{OE} | 3A | 1.8 | | 6.2 | ns |
| t_{PLZ} | | | 2.3 | | 5.6 | |

Skew Characteristics for Bus Transceiver

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see [Figure 1](#) and [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|-------------------|--------------|-------------|-----|-----|------|
| $t_{sk(LH)}$ | 1A or 2A | 1B or 2B | | 0.8 | ns |
| $t_{sk(HL)}$ | | | | 0.7 | |
| $t_{sk(LH)}$ | 1B or 2B | 1Y or 2Y | | 0.7 | ns |
| $t_{sk(HL)}$ | | | | 0.6 | |
| $t_{sk(t)}^{(1)}$ | 1A or 2A | 1B or 2B | | 1.7 | ns |
| | 1B or 2B | 1Y or 2Y | | 1.2 | |
| $t_{sk(pp)}$ | 1A or 2A | 1B or 2B | | 2.8 | ns |
| | 1B or 2B | 1Y or 2Y | | 1.4 | |

- (1) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

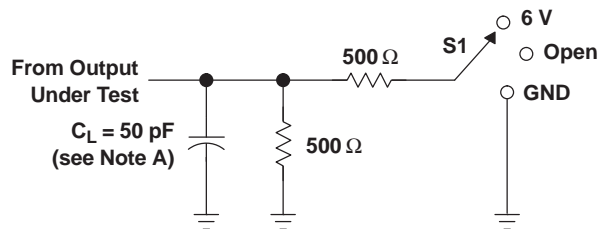
Skew Characteristics for UBT

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see [Figure 1](#) and [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | MAX | UNIT |
|-------------------|--------------|-------------|-----|-----|------|
| $t_{sk(LH)}$ | 3A | 3B | | 1.3 | ns |
| $t_{sk(HL)}$ | | | | 1.1 | |
| $t_{sk(LH)}$ | CLKAB | 3B | | 0.8 | ns |
| $t_{sk(HL)}$ | | | | 0.8 | |
| $t_{sk(LH)}$ | 3B | 3A | | 0.7 | ns |
| $t_{sk(HL)}$ | | | | 0.6 | |
| $t_{sk(LH)}$ | CLKBA | 3A | | 0.7 | ns |
| $t_{sk(HL)}$ | | | | 0.6 | |
| $t_{sk(t)}^{(1)}$ | 3A | 3B | | 1.9 | ns |
| | CLKAB | 3B | | 2.1 | |
| | 3B | 3A | | 1.2 | |
| | CLKBA | 3A | | 1 | |
| $t_{sk(pp)}$ | 3A | 3B | | 2.8 | ns |
| | CLKAB | 3B | | 2.7 | |
| | 3B | 3A | | 1.3 | |
| | CLKBA | 3A | | 1.2 | |

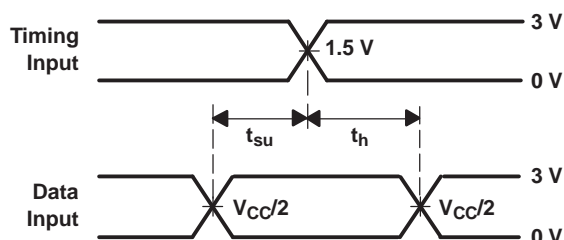
- (1) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

PARAMETER MEASUREMENT INFORMATION
A PORT

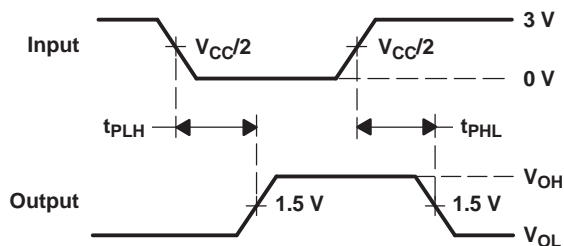


LOAD CIRCUIT

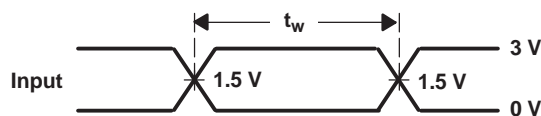
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |
| B-to-A Skew | Open |



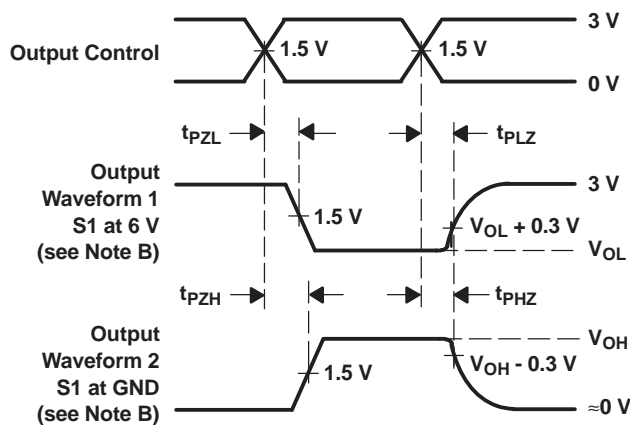
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

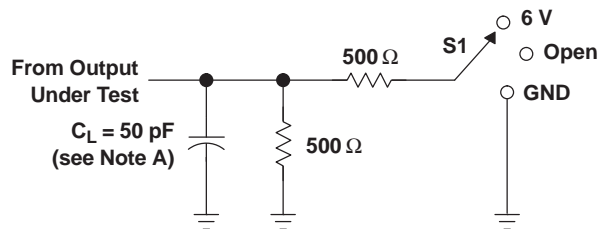


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR $\approx 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \approx 2 \text{ ns}$, $t_f \approx 2 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

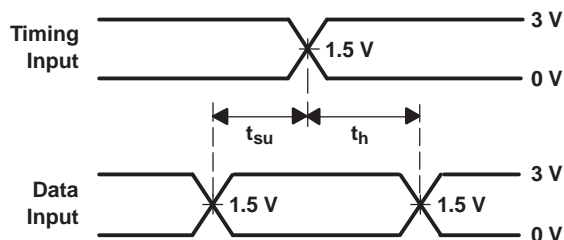
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION B PORT

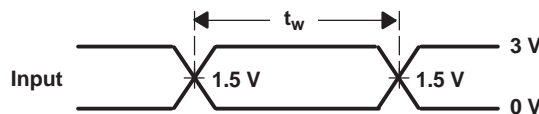


LOAD CIRCUIT

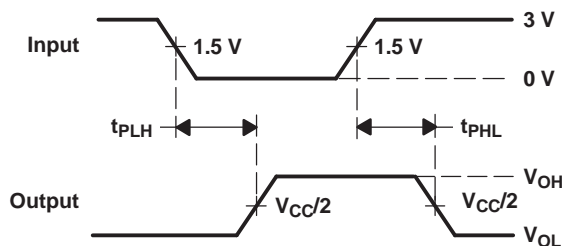
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |
| A-to-B Skew | Open |



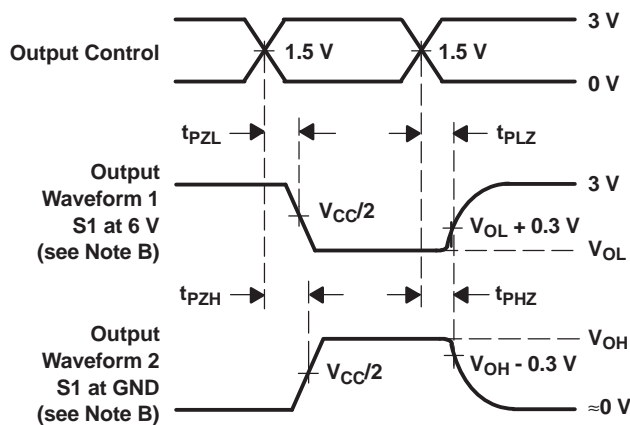
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



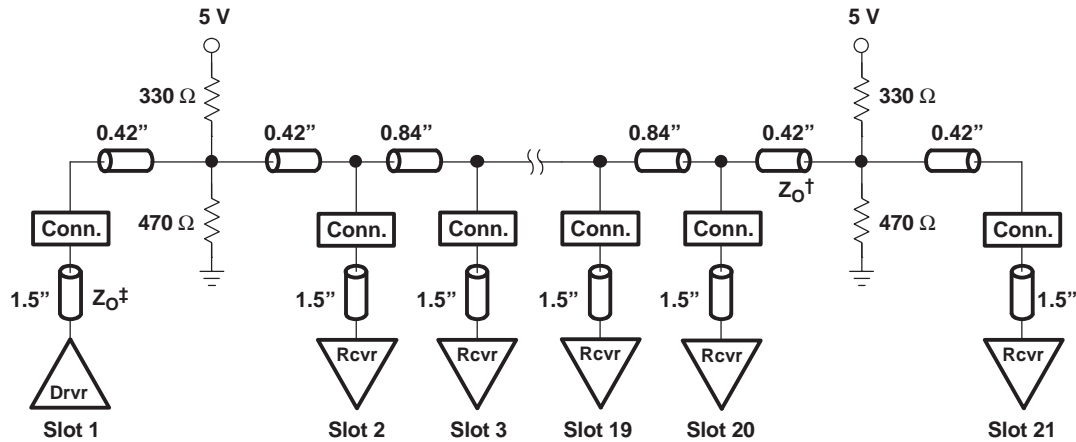
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \approx 10 MHz, $Z_O = 50 \Omega$, $t_r \approx 2$ ns, $t_f \approx 2$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics tables show the switching characteristics of the device into the lumped load shown in the parameter measurement information (PMI) (see Figure 1 and Figure 2). All logic devices currently are tested into this type of load. However, the designer's backplane application probably is a distributed load. For this reason, this device has been designed for optimum performance in the VME64x backplane as shown in Figure 3.



† Unloaded backplane trace natural impedance (Z_0) is 45 Ω . 45 Ω to 60 Ω is allowed, with 50 Ω being ideal.
‡ Card stub natural impedance (Z_0) is 60 Ω .

Figure 3. VME64x Backplane

The following switching characteristics tables derived from TI-SPICE models show the switching characteristics of the device into the backplane under full and minimum loading conditions, to help the designer better understand the performance of the VME device in this typical backplane. See www.ti.com/sc/etl for more information.

Driver in Slot 11, With Receiver Cards in All Other Slots (Full Load)

Switching Characteristics for Bus Transceiver Function

over recommended operating conditions (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-------------|-----------------------------------|-------------|-----|--------------------|------|------|
| t_{PLH} | 1A or 2A | 1B or 2B | 5.9 | | 8.5 | ns |
| t_{PHL} | | | 5.5 | | 8.7 | |
| $t_r^{(2)}$ | Transition time, B port (10%–90%) | | 9 | 8.6 | 11.4 | ns |
| $t_f^{(2)}$ | Transition time, B port (90%–10%) | | 8.9 | 9 | 10.8 | ns |

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.
(2) All t_r and t_f times are taken at the first receiver.

Switching Characteristics for UBT

over recommended operating conditions (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|-----------------------------------|-------------|-----|--------------------|------|------|
| t_{PLH} | 3A | 3B | 6.2 | | 8.9 | ns |
| t_{PHL} | | | 5.6 | | 9 | |
| t_{PLH} | LE | 3B | 6.1 | | 9.1 | ns |
| t_{PHL} | | | 5.6 | | 9 | |
| t_{PLH} | CLKAB | 3B | 6.2 | | 9.1 | ns |
| t_{PHL} | | | 5.7 | | 9 | |
| t_r ⁽²⁾ | Transition time, B port (10%–90%) | | 9 | 8.6 | 11.4 | ns |
| t_f ⁽²⁾ | Transition time, B port (90%–10%) | | 8.9 | 9 | 10.8 | ns |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

(2) All t_r and t_f times are taken at the first receiver.

Skew Characteristics for Bus Transceiver

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------------|--------------|-------------|-----|--------------------|-----|------|
| $t_{sk(LH)}$ | 1A or 2A | 1B or 2B | | | 2.5 | ns |
| $t_{sk(HL)}$ | | | | | 3 | |
| $t_{sk(t)}$ ⁽²⁾ | 1A or 2A | 1B or 2B | | | 1 | ns |
| $t_{sk(pp)}$ | 1A or 2A | 1B or 2B | | 0.5 | 3.4 | ns |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

Skew Characteristics for UBT

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------------|--------------|-------------|-----|--------------------|-----|------|
| $t_{sk(LH)}$ | 3A | 3B | | | 2.4 | ns |
| $t_{sk(HL)}$ | | | | | 3.4 | |
| $t_{sk(LH)}$ | CLKAB | 3B | | | 2.7 | ns |
| $t_{sk(HL)}$ | | | | | 3.4 | |
| $t_{sk(t)}$ ⁽²⁾ | 3A | 3B | | | 1 | ns |
| | CLKAB | 3B | | | 1 | |
| $t_{sk(pp)}$ | 3A | 3B | | 0.5 | 3.4 | ns |
| | CLKAB | 3B | | 0.6 | 3.5 | |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

Driver in Slot 1, With One Receiver in Slot 21 (Minimum Load)

Switching Characteristics for Bus Transceiver Function

over recommended operating conditions (unless otherwise noted) (see [Figure 3](#))

Switching Characteristics for Bus Transceiver Function (continued)

over recommended operating conditions (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|-----------------------------------|-------------|-----|--------------------|-----|------|
| t_{PLH} | 1A or 2A | 1B or 2B | 5.5 | | 7.4 | ns |
| t_{PHL} | | | 5.3 | | 7.4 | |
| t_r ⁽²⁾ | Transition time, B port (10%–90%) | | 3.9 | 3.4 | 4.4 | ns |
| t_f ⁽²⁾ | Transition time, B port (90%–10%) | | 3.7 | 3.4 | 4.8 | ns |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

(2) All t_r and t_f times are taken at the first receiver.

Switching Characteristics for UBT

over recommended operating conditions (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|-----------------------------------|-------------|-----|--------------------|-----|------|
| t_{PLH} | 3A | 3B | 5.8 | | 7.9 | ns |
| t_{PHL} | | | 5.5 | | 7.7 | |
| t_{PLH} | LE | 3B | 5.9 | | 8 | ns |
| t_{PHL} | | | 5.5 | | 7.8 | |
| t_{PLH} | CLKAB | 3B | 5.9 | | 8.1 | ns |
| t_{PHL} | | | 5.5 | | 7.7 | |
| t_r ⁽²⁾ | Transition time, B port (10%–90%) | | 3.9 | 3.4 | 4.4 | ns |
| t_f ⁽²⁾ | Transition time, B port (90%–10%) | | 3.7 | 3.4 | 4.8 | ns |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

(2) All t_r and t_f times are taken at the first receiver.

Skew Characteristics for Bus Transceiver

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------------|--------------|-------------|-----|--------------------|-----|------|
| $t_{sk(LH)}$ | 1A or 2A | 1B or 2B | | | 1.7 | ns |
| $t_{sk(HL)}$ | | | | | 2.1 | |
| $t_{sk(t)}$ ⁽²⁾ | 1A or 2A | 1B or 2B | | | 1 | ns |
| $t_{sk(pp)}$ | 1A or 2A | 1B or 2B | | 0.2 | 2.1 | ns |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

Skew Characteristics for UBT

for specific worst-case V_{CC} and temperature within the recommended ranges of supply voltage and operating free-air temperature (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------------|--------------|-------------|-----|--------------------|-----|------|
| $t_{sk(LH)}$ | 3A | 3B | | | 2 | ns |
| $t_{sk(HL)}$ | | | | | 2.3 | |
| $t_{sk(LH)}$ | CLKAB | 3B | | | 2.1 | ns |
| $t_{sk(HL)}$ | | | | | 2.4 | |
| $t_{sk(t)}$ ⁽²⁾ | 3A | 3B | | | 1 | ns |
| | CLKAB | 3B | | | 1 | |
| $t_{sk(pp)}$ | 3A | 3B | | 0.2 | 2.5 | ns |
| | CLKAB | 3B | | 0.2 | 2.9 | |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

(2) $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs of the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature and apply to any outputs switching in opposite directions, both low to high (LH) and high to low (HL) [$t_{sk(t)}$].

By simulating the performance of the device using the VME64x backplane (see [Figure 3](#)), the maximum peak current in or out of the B-port output, as the devices switch from one logic state to another, was found to be equivalent to driving the lumped load shown in [Figure 4](#).

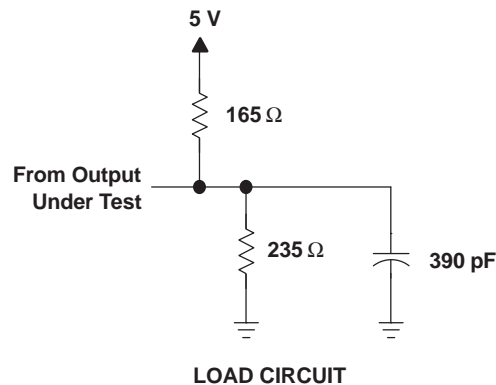


Figure 4. Equivalent AC Peak Output-Current Lumped Load

In general, the rise- and fall-time distribution is shown in [Figure 5](#). Since VME devices were designed for use into distributed loads like the VME64x backplane (B/P), there are significant differences between low-to-high (LH) and high-to-low (HL) values in the lumped load shown in the PMI (see [Figure 1](#) and [Figure 2](#)).

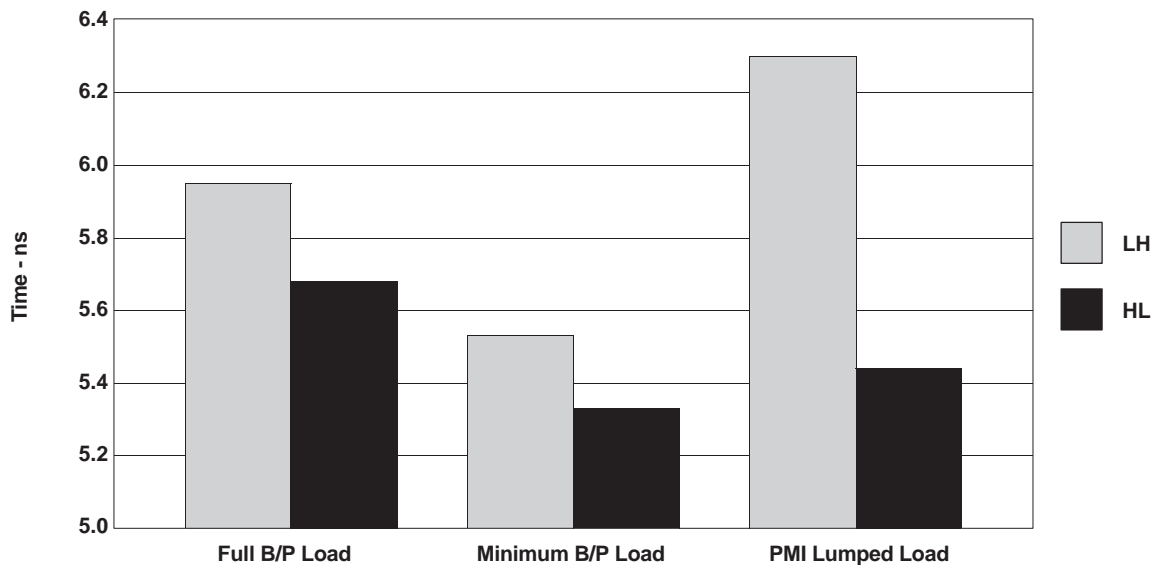


Figure 5.

Characterization-laboratory data in Figure 6 and Figure 7 show the absolute ac peak output current, with different supply voltages, as the devices change output logic state. A typical nominal process is shown to demonstrate the devices' peak ac output drive capability.

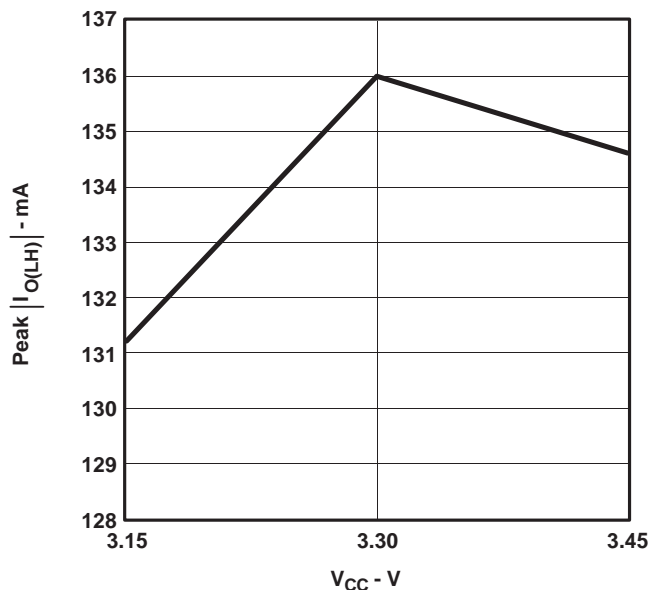


Figure 6.

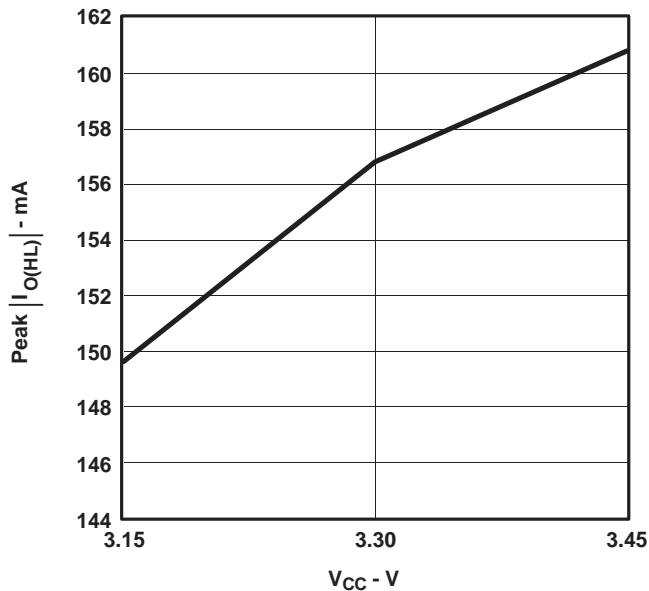


Figure 7.

TYPICAL CHARACTERISTICS

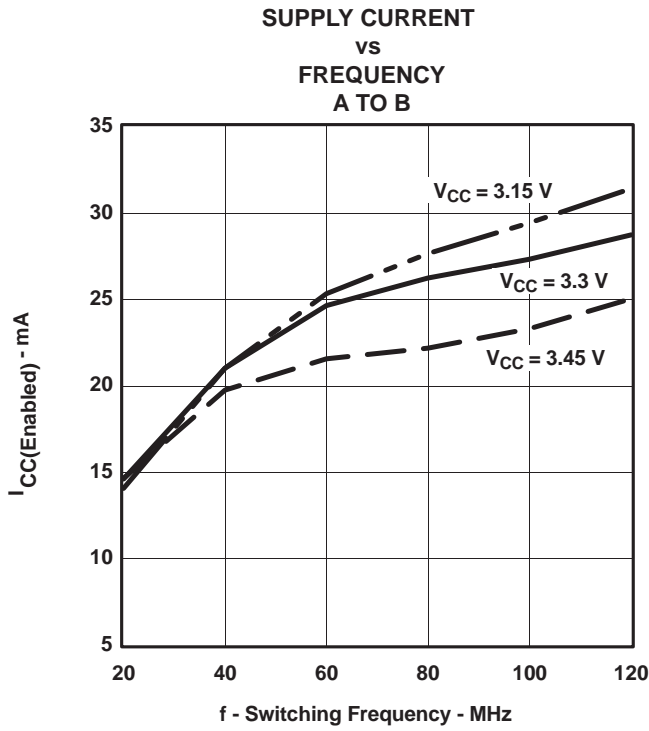


Figure 8.

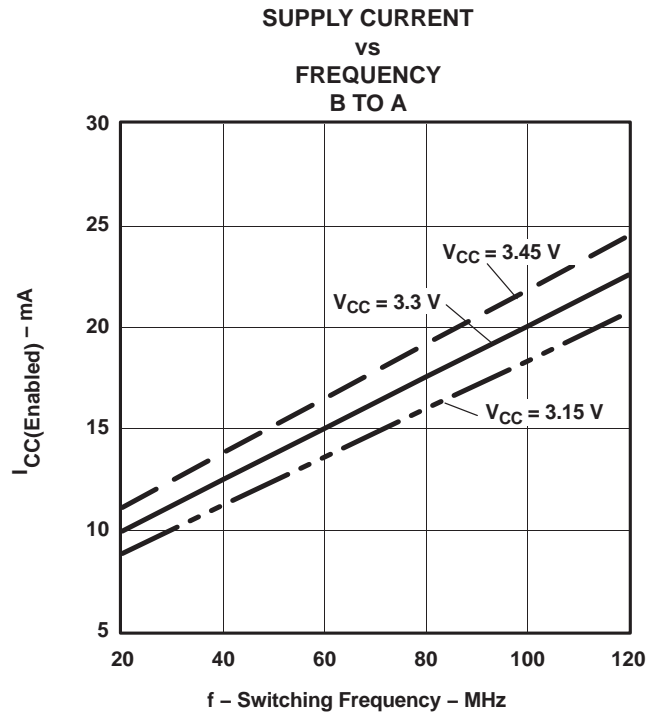


Figure 9.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

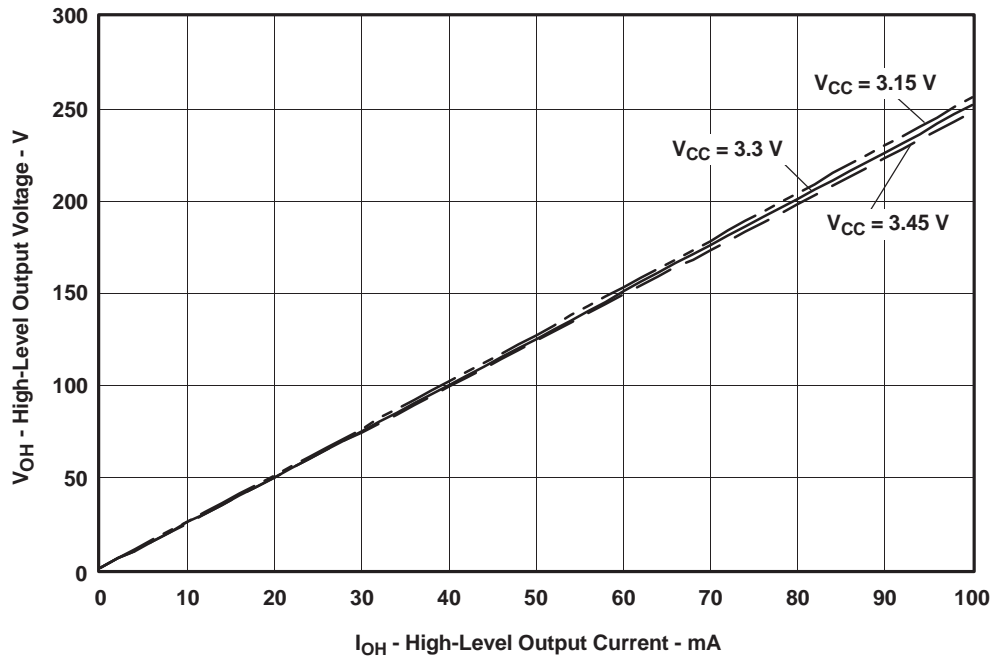


Figure 10. V_{OL} vs I_{OL}

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

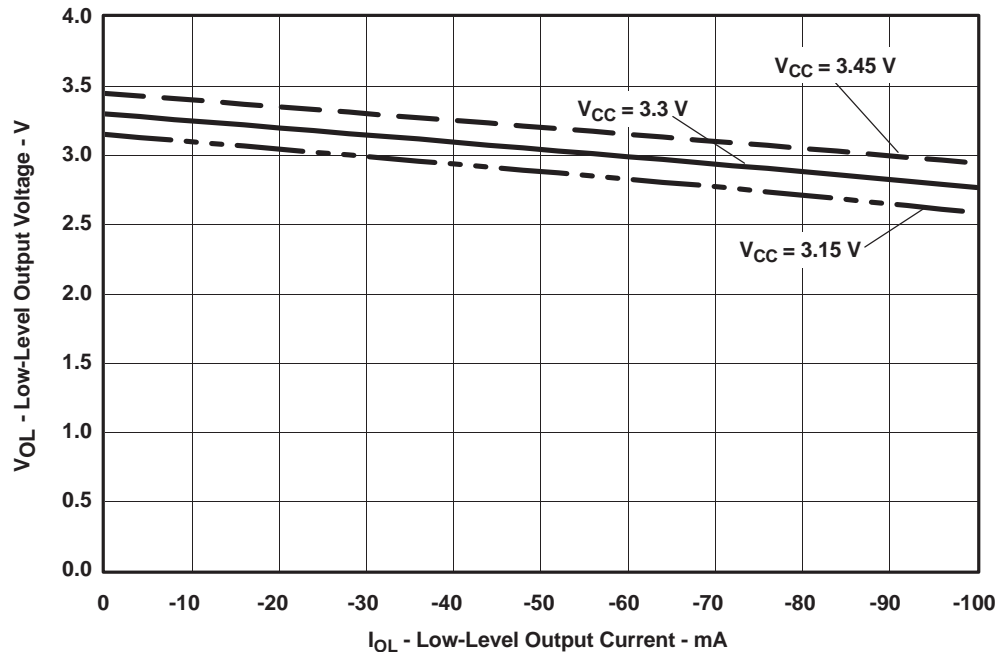


Figure 11. V_{OH} vs I_{OH}

VMEbus Summary

In 1981, the VMEbus was introduced as a backplane bus architecture for industrial and commercial applications. The data-transfer protocols used to define the VMEbus came from the Motorola™ VERSA bus architecture that owed its heritage to the then recently introduced Motorola 68000 microprocessor. The VMEbus, when introduced, defined two basic data-transfer operations: single-cycle transfers consisting of an address and a data transfer, and a block transfer (BLT) consisting of an address and a sequence of data transfers. These transfers were asynchronous, using a master-slave handshake. The master puts address and data on the bus and waits for an acknowledgment. The selected slave either reads or writes data to or from the bus, then provides a data-acknowledge (DTACK*) signal. The VMEbus system data throughput was 40 Mbyte/s. Previous to the VMEbus, it was not uncommon for the backplane buses to require elaborate calculations to determine loading and drive current for interface design. This approach made designs difficult and caused compatibility problems among manufacturers. To make interface design easier and to ensure compatibility, the developers of the VMEbus architecture defined specific delays based on a 21-slot terminated backplane and mandated the use of certain high-current TTL drivers, receivers, and transceivers.

In 1989, multiplexing block transfer (MBLT) effectively increased the number of bits from 32 to 64, thereby doubling the transfer rate. In 1995, the number of handshake edges was reduced from four to two in the double-edge transfer (2eVME) protocol, doubling the data rate again. In 1997, the VMEbus International Trade Association (VITA) established a task group to specify a synchronous protocol to increase data-transfer rates to 320 Mbyte/s, or more. The unreleased specification, VITA 1.5 [double-edge source synchronous transfer (2eSST)], is based on the asynchronous 2eVME protocol. It does not wait for acknowledgement of the data by the receiver and requires incident-wave switching. Sustained data rates of 1 Gbyte/s, more than ten times faster than traditional VME64 backplanes, are possible by taking advantage of 2eSST and the 21-slot VME320 star-configuration backplane. The VME320 backplane approximates a lumped load, allowing substantially higher-frequency operation over the VME64x distributed-load backplane. Traditional VME64 backplanes with no changes theoretically can sustain 320 Mbyte/s.

From BLT to 2eSST – A Look at the Evolution of VMEbus Protocols by John Rynearson, Technical Director, VITA, provides additional information on VMEbus and can be obtained at www.vita.com.

Maximum Data Transfer Rates

| DATE | TOPOLOGY | PROTOCOL | DATA BITS PER CYCLE | DATA TRANSFERS PER CLOCK CYCLE | PER SYSTEM (Mbyte/s) | FREQUENCY (MHz) | |
|------|------------------|----------|---------------------|--------------------------------|----------------------|-----------------|--------|
| | | | | | | BACKPLANE | CLOCK |
| 1981 | VMEbus IEEE-1014 | BLT | 32 | 1 | 40 | 10 | 10 |
| 1989 | VME64 | MBLT | 64 | 1 | 80 | 10 | 10 |
| 1995 | VME64x | 2eVME | 64 | 2 | 160 | 10 | 20 |
| 1997 | VME64x | 2eSST | 64 | 2-No Ack | 160–320 | 10–20 | 20–40 |
| 1999 | VME320 | 2eSST | 64 | 2-No Ack | 320–1000 | 20–62.5 | 40–125 |

Applicability

Target applications for VME backplanes include industrial controls, telecommunications, simulation, high-energy physics, office automation, and instrumentation systems.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| 74VMEH22501DGGRG4 | Active | Production | TSSOP (DGG) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VMEH22501 |
| 74VMEH22501DGGRG4.B | Active | Production | TSSOP (DGG) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VMEH22501 |
| 74VMEH22501DGVRG4 | Active | Production | TVSOP (DGV) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VK501 |
| 74VMEH22501DGVRG4.B | Active | Production | TVSOP (DGV) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VK501 |
| SN74VMEH22501DGGR | Active | Production | TSSOP (DGG) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VMEH22501 |
| SN74VMEH22501DGGR.B | Active | Production | TSSOP (DGG) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VMEH22501 |
| SN74VMEH22501DGVR | Active | Production | TVSOP (DGV) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VK501 |
| SN74VMEH22501DGVR.B | Active | Production | TVSOP (DGV) 48 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 85 | VK501 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74VMEH22501DGGRG4 | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| 74VMEH22501DGVRG4 | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |
| SN74VMEH22501DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| SN74VMEH22501DGV | TVSOP | DGV | 48 | 2000 | 330.0 | 16.4 | 7.1 | 10.2 | 1.6 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

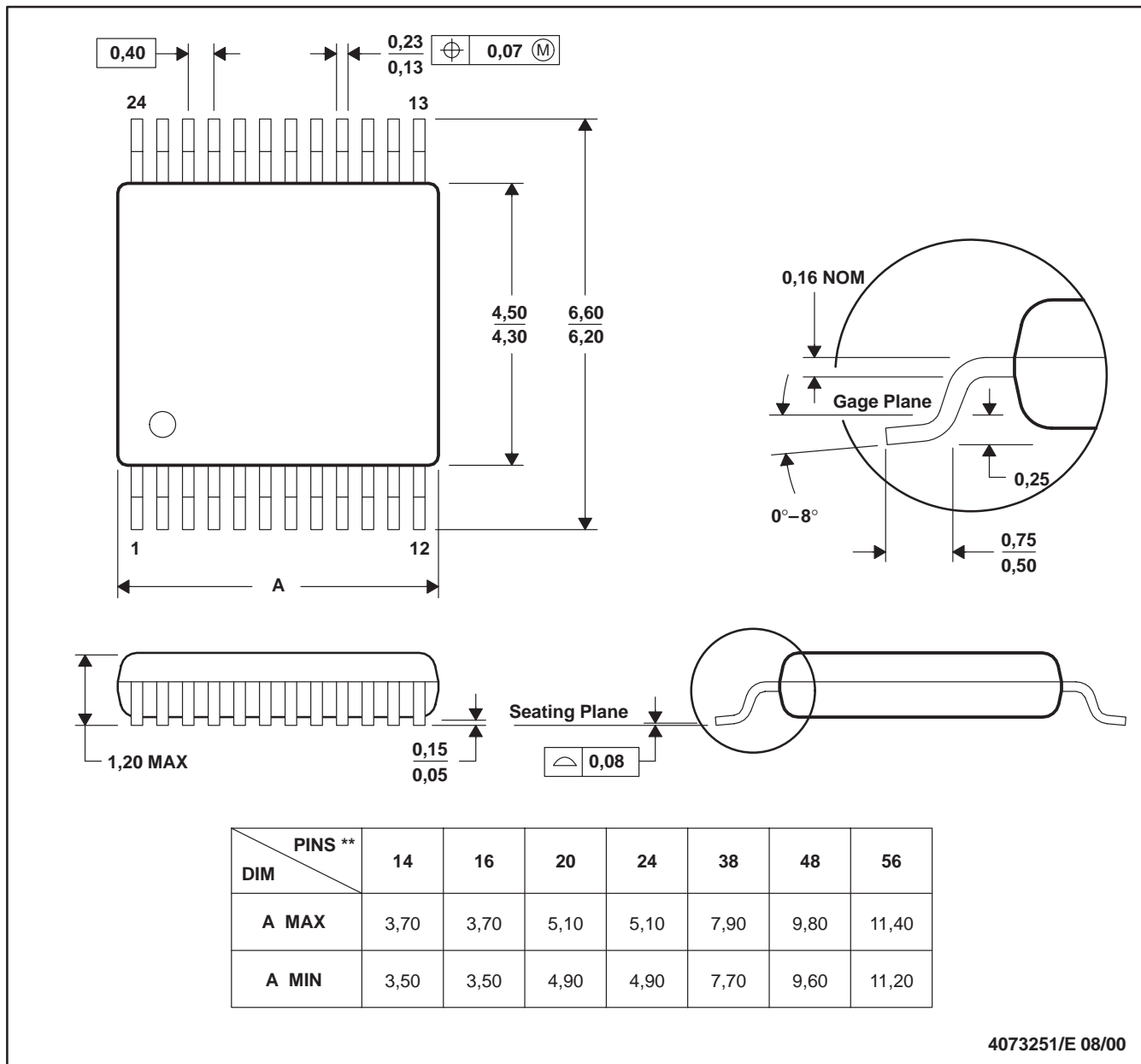

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74VMEH22501DGGRG4 | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| 74VMEH22501DGVRG4 | TVSOP | DGV | 48 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74VMEH22501DGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74VMEH22501DGVR | TVSOP | DGV | 48 | 2000 | 356.0 | 356.0 | 35.0 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



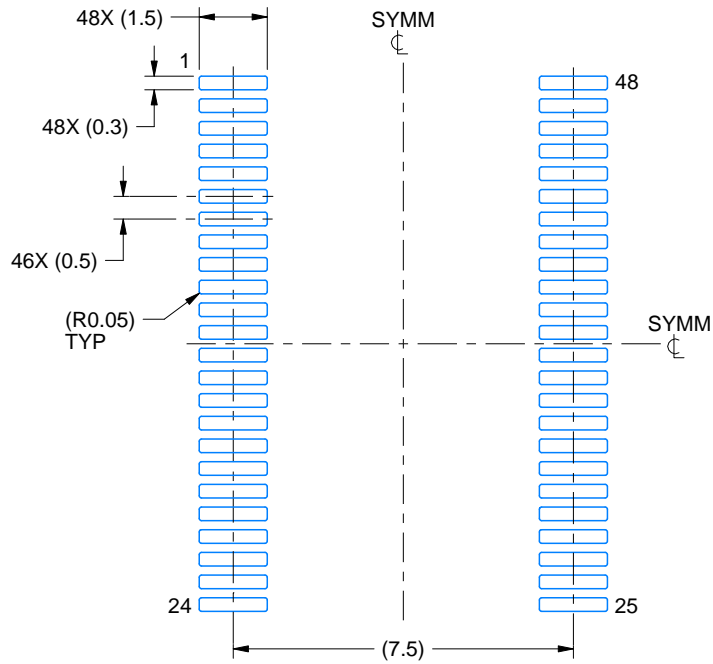
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

EXAMPLE BOARD LAYOUT

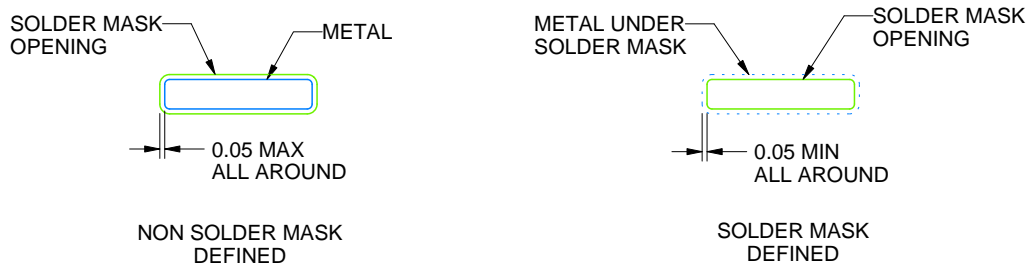
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

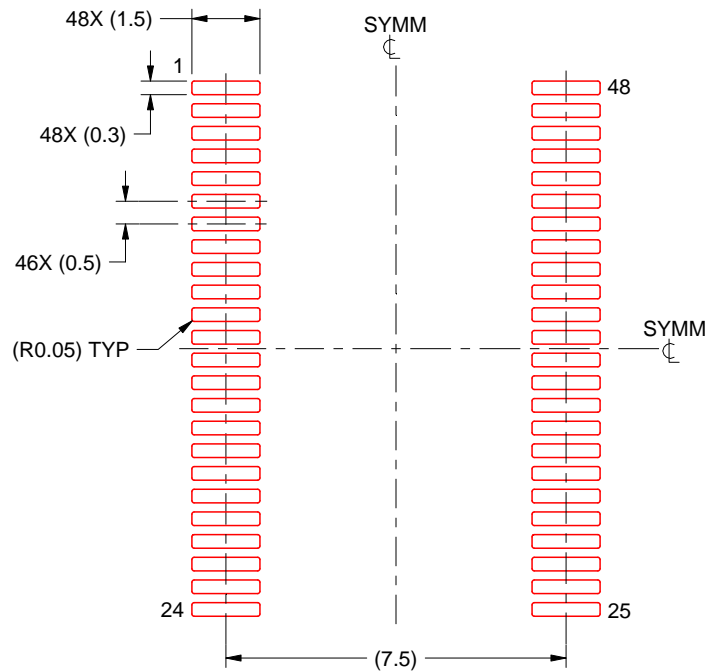
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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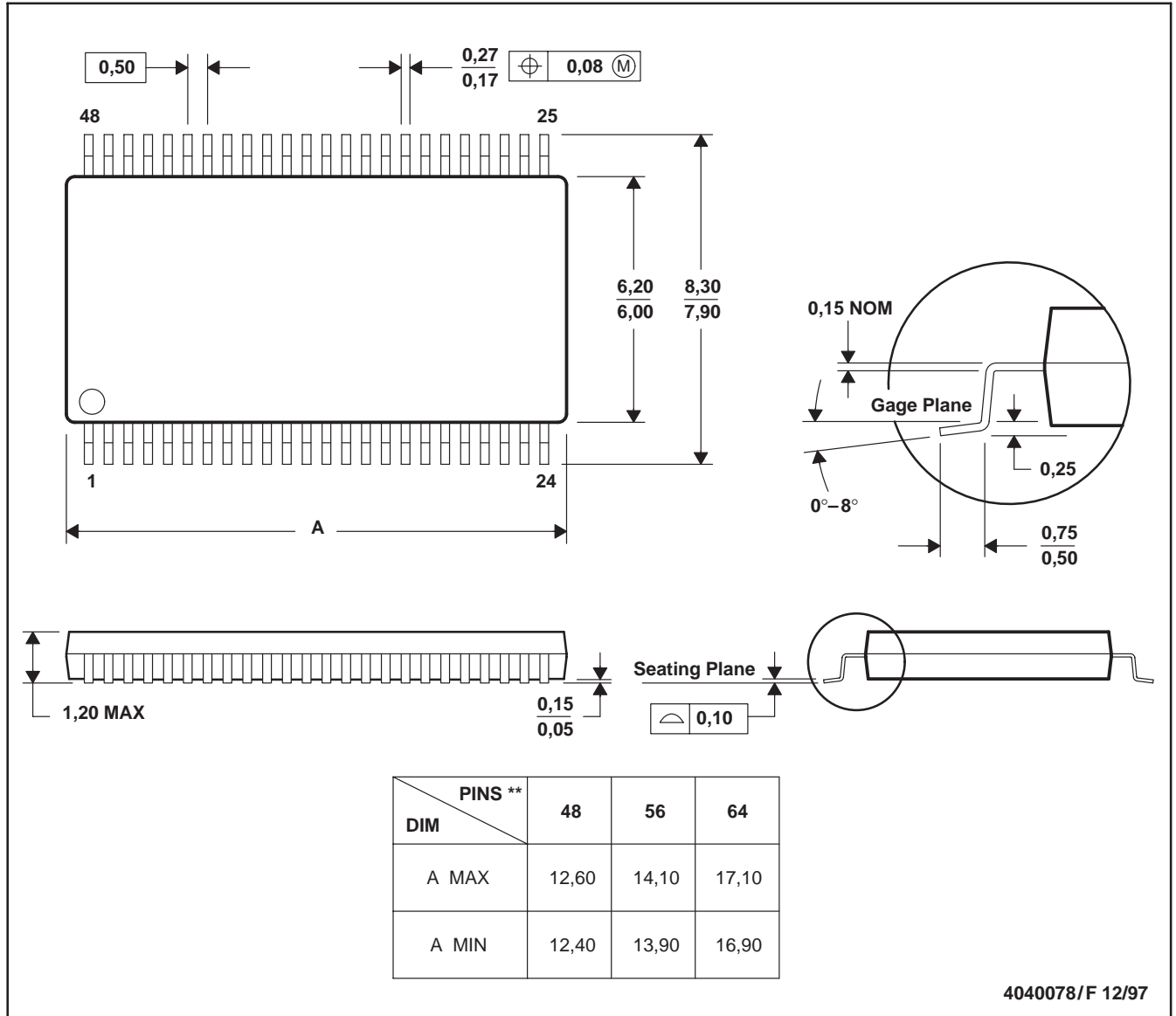
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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