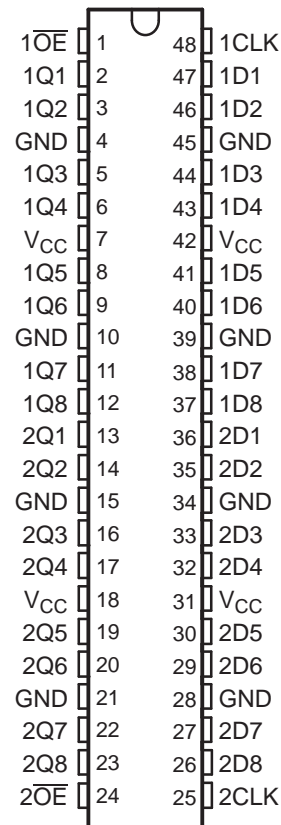


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH16374 . . . WD PACKAGE  
SN74LVTH16374 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The 'LVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145R–MAY 1992–REVISED AUGUST 2007

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

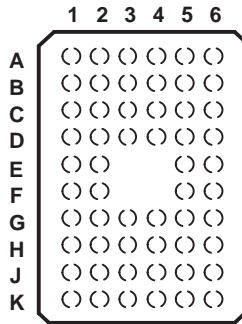
### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVTH16374GRDR	LL374
	FBGA – ZRD (Pb-free)		SN74LVTH16374ZRDR	
	SSOP – DL	Tube of 25	SN74LVTH16374DL 74LVTH16374DLG4	LVTH16374
		Reel of 1000	SN74LVTH16374DLR 74LVTH16374DLRG4	
			TSSOP – DGG	
	VFBGA – GQL	Reel of 1000	SN74LVTH16374KR	LL374
	VFBGA – ZQL (Pb-free)		SN74LVTH16374ZQLR	
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16374WD	SNJ54LVTH16374WD

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**GQL OR ZQL PACKAGE  
(TOP VIEW)**

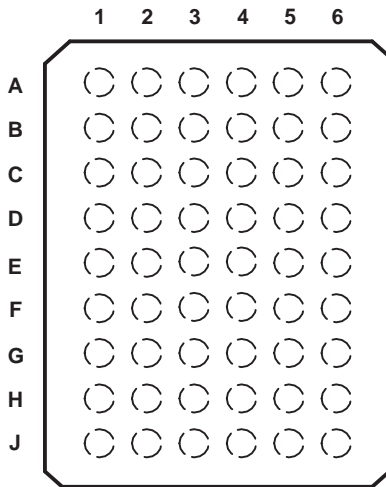


**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(56-Ball GQL/ZQL Package)**

	1	2	3	4	5	6
<b>A</b>	1 $\overline{OE}$	NC	NC	NC	NC	1CLK
<b>B</b>	1Q2	1Q1	GND	GND	1D1	1D2
<b>C</b>	1Q4	1Q3	V <sub>CC</sub>	V <sub>CC</sub>	1D3	1D4
<b>D</b>	1Q6	1Q5	GND	GND	1D5	1D6
<b>E</b>	1Q8	1Q7			1D7	1D8
<b>F</b>	2Q1	2Q2			2D2	2D1
<b>G</b>	2Q3	2Q4	GND	GND	2D4	2D3
<b>H</b>	2Q5	2Q6	V <sub>CC</sub>	V <sub>CC</sub>	2D6	2D5
<b>J</b>	2Q7	2Q8	GND	GND	2D8	2D7
<b>K</b>	2 $\overline{OE}$	NC	NC	NC	NC	2CLK

(1) NC – No internal connection

**GRD OR ZRD PACKAGE  
(TOP VIEW)**



**TERMINAL ASSIGNMENTS<sup>(1)</sup>  
(54-Ball GRD/ZRD Package)**

	1	2	3	4	5	6
<b>A</b>	1Q1	NC	1 $\overline{OE}$	1CLK	NC	1D1
<b>B</b>	1Q3	1Q2	NC	NC	1D2	1D3
<b>C</b>	1Q5	1Q4	V <sub>CC</sub>	V <sub>CC</sub>	1D4	1D5
<b>D</b>	1Q7	1Q6	GND	GND	1D6	1D7
<b>E</b>	2Q1	1Q8	GND	GND	1D8	2D1
<b>F</b>	2Q3	2Q2	GND	GND	2D2	2D3
<b>G</b>	2Q5	2Q4	V <sub>CC</sub>	V <sub>CC</sub>	2D4	2D5
<b>H</b>	2Q7	2Q6	NC	NC	2D6	2D7
<b>J</b>	2Q8	NC	2 $\overline{OE}$	2CLK	NC	2D8

(1) NC – No internal connection

**FUNCTION TABLE  
(EACH FLIP-FLOP)**

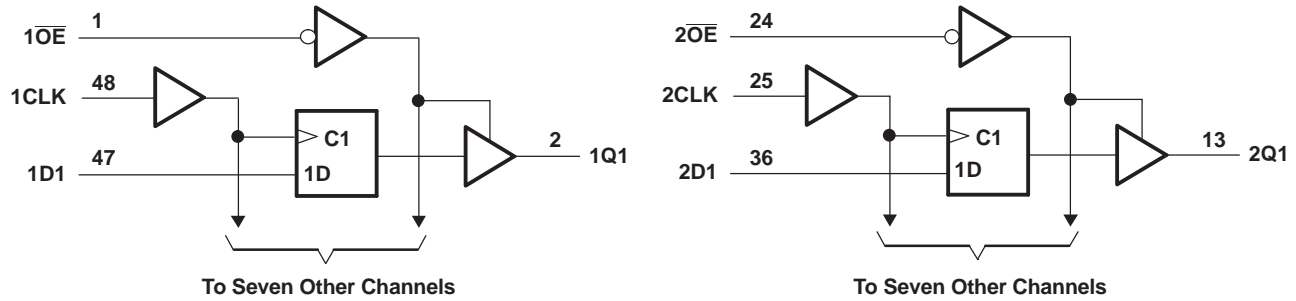
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub>
H	X	X	Z

# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145R–MAY 1992–REVISED AUGUST 2007

### LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state	SN54LVTH16374	96	mA
		SN74LVTH16374	128	
$I_O$	Current into any output in the high state <sup>(3)</sup>	SN54LVTH16374	48	mA
		SN74LVTH16374	64	
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		SN54LVTH16374		SN74LVTH16374		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	2.7	3.6	2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage		5.5		5.5	V
I <sub>OH</sub>	High-level output current		–24		–32	mA
I <sub>OL</sub>	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate	200		200		μs/V
T <sub>A</sub>	Operating free-air temperature	–55	125	–40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS145R–MAY 1992–REVISED AUGUST 2007

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH16374			SN74LVTH16374			UNIT	
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX		
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2			-1.2	V	
$V_{OH}$	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V	
	$V_{CC} = 2.7\text{ V}$ ,	$I_{OH} = -8\text{ mA}$	2.4			2.4				
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2							
$I_{OH} = -32\text{ mA}$					2					
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$				0.2			V	
		$I_{OL} = 24\text{ mA}$				0.5				
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$				0.4				
		$I_{OL} = 32\text{ mA}$				0.5				
		$I_{OL} = 48\text{ mA}$				0.55				
		$I_{OL} = 64\text{ mA}$				0.55				
$I_I$	$V_{CC} = 0\text{ or } 3.6\text{ V}$ , $V_I = 5.5\text{ V}$					10			$\mu\text{A}$	
	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$					$\pm 1$			
		Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$		1				1
$V_I = 0$				-5			-5			
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$					$\pm 100$			$\mu\text{A}$	
$I_{I(\text{hold})}$	Data inputs	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75			75	$\mu\text{A}$	
			$V_I = 2\text{ V}$		-75			-75		
		$V_{CC} = 3.6\text{ V}$ , <sup>(2)</sup>		$V_I = 0\text{ to } 3.6\text{ V}$						500 -750
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$					5			$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$					-5			$\mu\text{A}$	
$I_{OZPU}$	$V_{CC} = 0\text{ to } 1.5\text{ V}$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $\overline{OE} = \text{don't care}$					$\pm 100$ <sup>(3)</sup>			$\mu\text{A}$	
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to } 0$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $\overline{OE} = \text{don't care}$					$\pm 100$ <sup>(3)</sup>			$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high		0.19			0.19			mA
		Outputs low		5			5			
		Outputs disabled		0.19			0.19			
$\Delta I_{CC}$ <sup>(4)</sup>	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$					0.2			0.2	mA
$C_I$	$V_I = 3\text{ V or } 0$					3			3	pF
$C_O$	$V_O = 3\text{ V or } 0$					9			9	pF

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

## Timing Requirements

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		SN54LVTH16374				SN74LVTH16374				UNIT
		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	160		160		160		160		MHz
$t_w$	Pulse duration, CLK high or low	3		3		3		3		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	2.9		3.3		1.8		2		ns
$t_h$	Hold time, data after CLK $\uparrow$	0.8		0.2		0.8		0.1		ns

## Switching Characteristics

 over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16374				SN74LVTH16374				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$	
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	
$f_{\text{max}}$			160		160		160			160	MHz
$t_{\text{PLH}}$	CLK	Q	1.4 5.6		6.2		1.9 3 4.5			5.2	ns
$t_{\text{PHL}}$			1.7 4.8		5		2.1 2.9 4			4.2	
$t_{\text{PZH}}$	$\overline{\text{OE}}$	Q	1 5.6		6.4		1.5 2.8 4.5			5.4	ns
$t_{\text{PZL}}$			1.4 5.5		6.2		1.5 2.8 4.4			5	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	Q	1 6.4		6.9		2.4 3.5 5			5.4	ns
$t_{\text{PLZ}}$			1.7 5		5.2		2 3.2 4.6			4.8	
$t_{\text{sk(LH)}}$							0.5			ns	
$t_{\text{sk(HL)}}$							0.5				

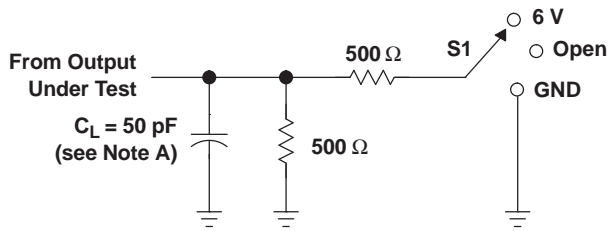
 (1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

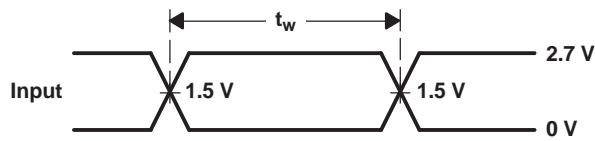
SCBS145R—MAY 1992—REVISED AUGUST 2007

### PARAMETER MEASUREMENT INFORMATION

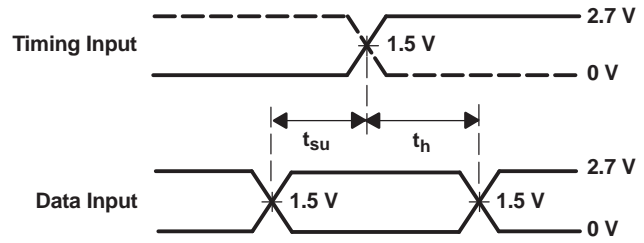


LOAD CIRCUIT

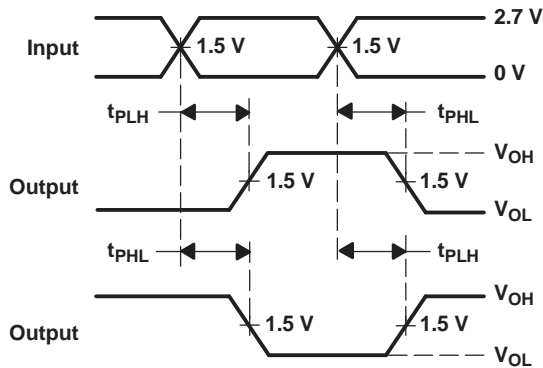
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



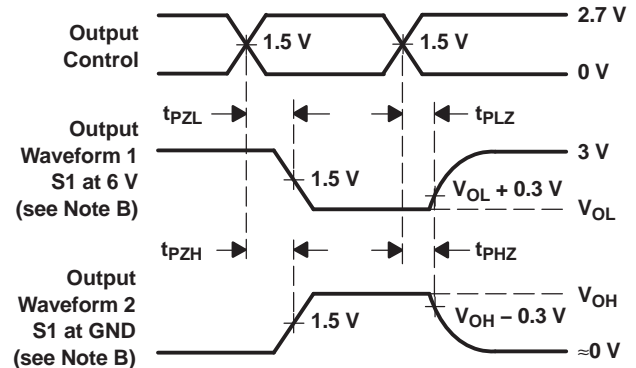
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVTH16374DGGR1G4	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
74LVTH16374DGGR1G4.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
<a href="#">SN74LVTH16374DGGR</a>	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DGGR.B	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
<a href="#">SN74LVTH16374DL</a>	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DL.B	Active	Production	SSOP (DL)   48	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
<a href="#">SN74LVTH16374DLR</a>	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DLR.B	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DLRG4	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374
SN74LVTH16374DLRG4.B	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16374

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVTH16374 :**

- Enhanced Product : [SN74LVTH16374-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVTH16374DGGR1G4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16374DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16374DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVTH16374DLRG4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVTH16374DGGR1G4	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH16374DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH16374DLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVTH16374DLRG4	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVTH16374DL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVTH16374DL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87



# EXAMPLE BOARD LAYOUT

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

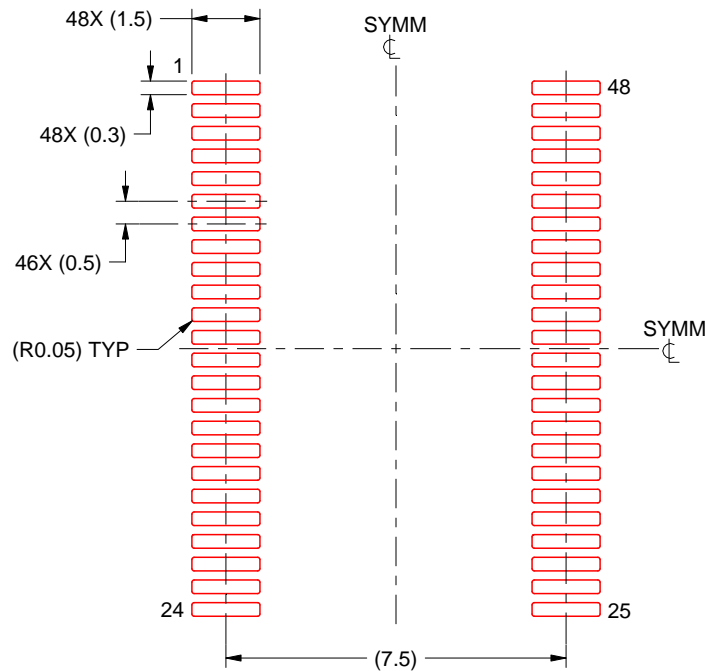
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

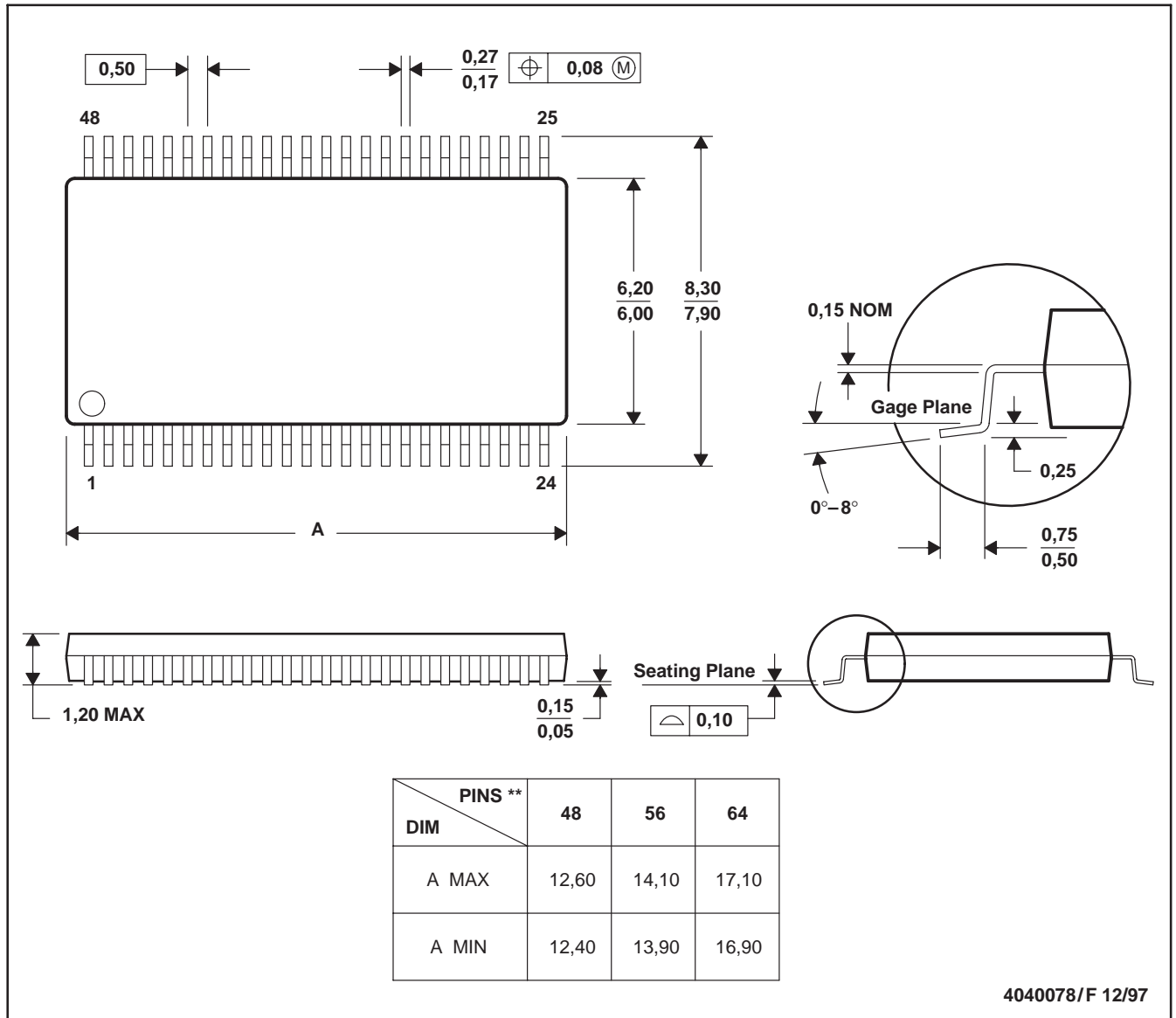
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

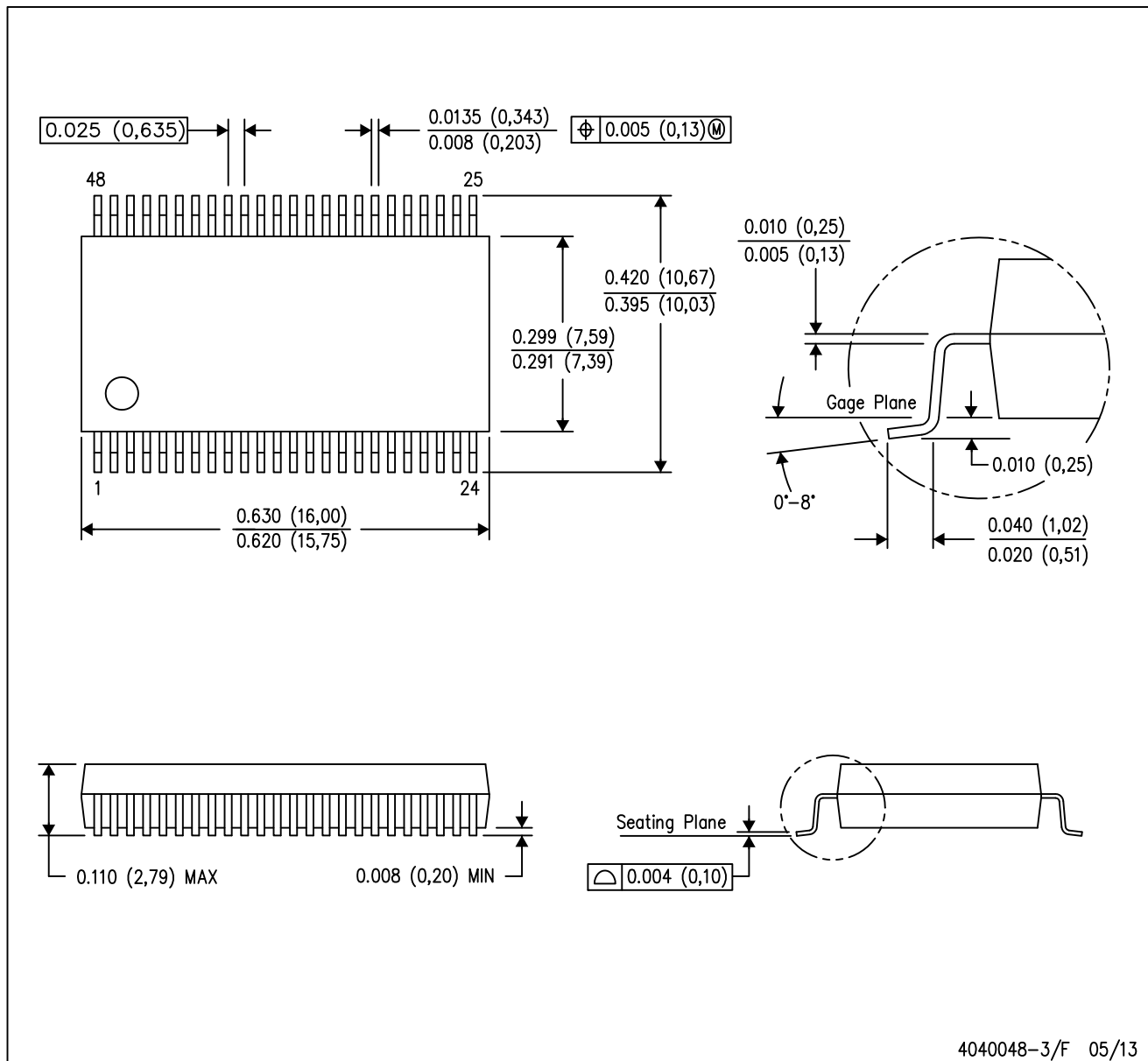


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated