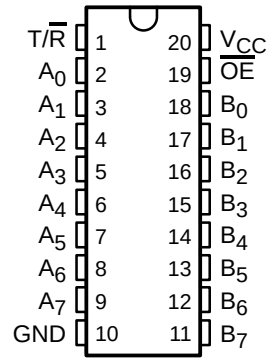
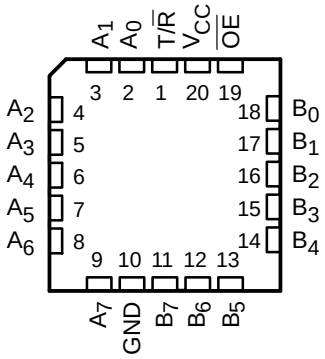
- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **CY54FCT245T**
  - **48-mA Output Sink Current**
    12-mA Output Source Current
- **CY74FCT245T**
  - **64-mA Output Sink Current**
    32-mA Output Source Current
- **3-State Outputs**

CY54FCT245T . . . D PACKAGE
CY74FCT245T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT245T . . . L PACKAGE
(TOP VIEW)



description

The ’FCT245T devices contain eight noninverting bidirectional buffers with 3-state outputs and are intended for bus-oriented applications.

The transmit/receive (T/$\overline{R}$) input determines the direction of data flow through these bidirectional transceivers. Transmit (active high) enables data from A ports to B ports. The output enable ($\overline{OE}$), when high, disables both the A and B ports by putting them in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	3.8	CY74FCT245DTQCT	FCT245D
	QSOP – Q	Tape and reel	4.1	CY74FCT245CTQCT	FCT245C
	SOIC – SO	Tube	4.1	CY74FCT245CTSOC	FCT245C
		Tape and reel	4.1	CY74FCT245CTSOCT	
	DIP – P	Tube	4.6	CY74FCT245ATPC	CY74FCT245ATPC
	QSOP – Q	Tape and reel	4.6	CY74FCT245ATQCT	FCT245A
	SOIC – SO	Tube	4.6	CY74FCT245ATSOC	FCT245A
		Tape and reel	4.6	CY74FCT245ATSOCT	
	QSOP – Q	Tape and reel	7	CY74FCT245TQCT	FCT245
	SOIC – SO	Tube	7	CY74FCT245TSOC	FCT245
		Tape and reel	7	CY74FCT245TSOCT	
–55°C to 125°C	CDIP – D	Tube	4.5	CY54FCT245CTDMB	
	LCC – L	Tube	4.5	CY54FCT245CTLMB	
	CDIP – D	Tube	4.9	CY54FCT245ATDMB	
	LCC – L	Tube	4.9	CY54FCT245ATLMB	
	CDIP – D	Tube	7.5	CY54FCT245TDMB	
	LCC – L	Tube	7.5	CY54FCT245TLMB	

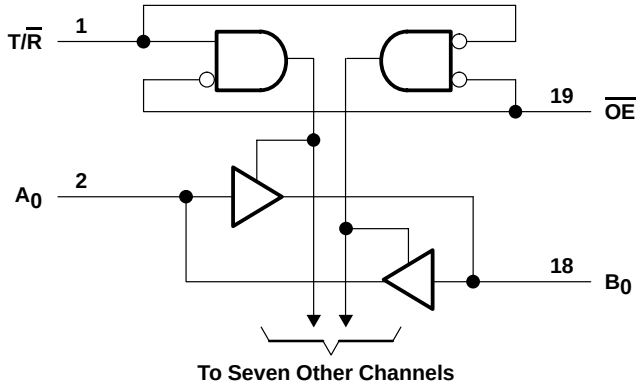
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	T/$\overline{R}$	
L	L	B data to bus A
L	H	A data to bus B
H	X	Z

H = High logic level, L = Low logic level, X = Don't care, Z = High-impedance state

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package . . . . . 69°C/W
Q package . . . . . 68°C/W
SO package . . . . . 58°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		CY54FCT245T			CY74FCT245T CY74FCT245AT CY74FCT245CT CY74FCT245DT			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–32	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY54FCT245T			CY74FCT245T			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = –18 mA		–0.7	–1.2				V
	V_{CC} = 4.75 V,	I_{IN} = –18 mA					–0.7	–1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –12 mA	2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = –32 mA				2			
		I_{OH} = –15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.3	0.55	
V_{hys}	All inputs			0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}			5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}						5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						±1	
I_{OZH}	V_{CC} = 5.5 V,	V_{OUT} = 2.7 V			10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V						10	
I_{OZL}	V_{CC} = 5.5 V,	V_{OUT} = 0.5 V			–10				µA
	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V						–10	
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V	–60	–120	–225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V				–60	–120	–225	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V			±1			±1	µA
I_{CC}	V_{CC} = 5.5 V,	V_{IN} ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2				mA
	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open			0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open						0.5	2	
I_{CCD}¶	V_{CC} = 5.5 V, One input switching at 50% duty cycle, Outputs open, T/$\overline{R}$ or $\overline{OE}$ = GND and V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V			0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, One input switching at 50% duty cycle, Outputs open, T/$\overline{R}$ or $\overline{OE}$ = GND and V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V						0.06	0.12	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

¶ This parameter is derived for use in total power-supply calculations.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT245T			CY74FCT245T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_C#	V_{CC} = 5.5 V, Outputs open, T/$\overline{R}$ or $\overline{OE}$ = GND	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$V or $V_{IN} \ge V_{CC} - 0.2$ V		1.3	2.6‖				
			V_{IN} = 3.4 V or GND		3.3	10.6‖				
	V_{CC} = 5.25 V, Outputs open, T/$\overline{R}$ or $\overline{OE}$ = GND	One bit switching at f_1 = 10 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					0.7	1.4	
			V_{IN} = 3.4 V or GND					1.2	3.4	
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$V or $V_{IN} \ge V_{CC} - 0.2$ V					1.3	2.6‖	
			V_{IN} = 3.4 V or GND					3.3	10.6‖	
C_i					5	10		5	10	pF
C_o					9	12		9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

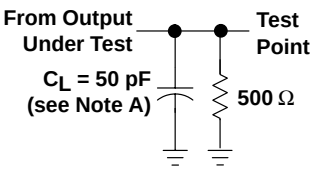
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT245T		CY54FCT245AT		CY54FCT245CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	7.5	1.5	4.9	1.5	4.5	ns
t_{PHL}			1.5	7.5	1.5	4.9	1.5	4.5	
t_{PZH}	$\overline{OE}$ or T/$\overline{R}$	A or B	1.5	10	1.5	6.5	1.5	6.2	ns
t_{PZL}			1.5	10	1.5	6.5	1.5	6.2	
t_{PHZ}	$\overline{OE}$ or T/$\overline{R}$	A or B	1.5	10	1.5	6	1.5	5.2	ns
t_{PLZ}			1.5	10	1.5	6	1.5	5.2	

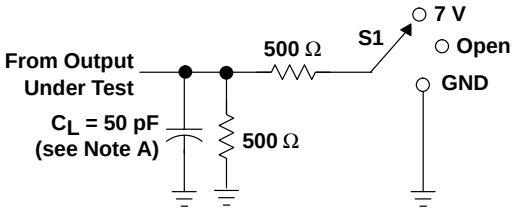
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT245T		CY74FCT245AT		CY74FCT245CT		CY74FCT245DT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.5	7	1.5	4.6	1.5	4.1	1.5	3.8	ns
t_{PHL}			1.5	7	1.5	4.6	1.5	4.1	1.5	3.8	
t_{PZH}	$\overline{OE}$ or T/$\overline{R}$	A or B	1.5	9.5	1.5	6.2	1.5	5.8	1.5	5	ns
t_{PZL}			1.5	9.5	1.5	6.2	1.5	5.8	1.5	5	
t_{PHZ}	$\overline{OE}$ or T/$\overline{R}$	A or B	1.5	7.5	1.5	5	1.5	4.8	1.5	4.3	ns
t_{PLZ}			1.5	7.5	1.5	5	1.5	4.8	1.5	4.3	

PARAMETER MEASUREMENT INFORMATION

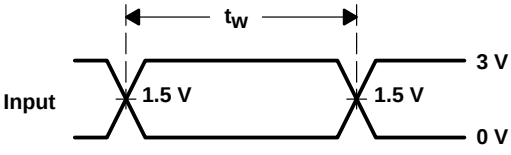


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

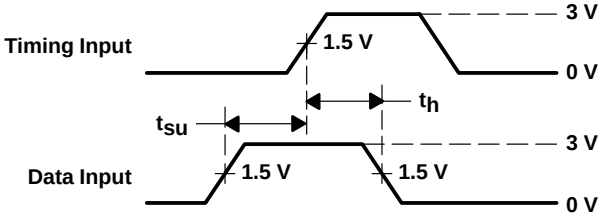


LOAD CIRCUIT FOR
3-STATE OUTPUTS

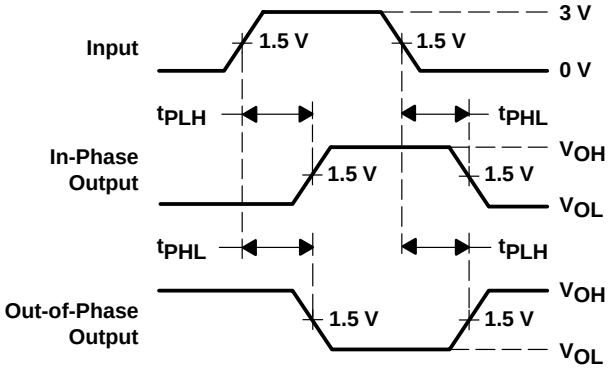
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



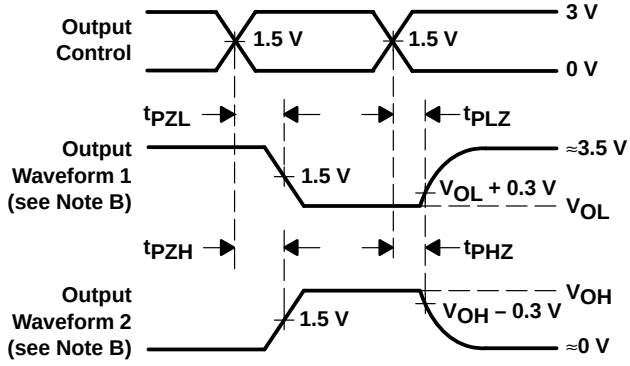
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9221401M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221401M2A CY54FCT 245TLMB
5962-9221401MRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221401MRA
5962-9221403M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221403M2A
5962-9221403MRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221403MRA CY54FCT245ATDMB
5962-9221405M2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221405M2A CY54FCT 245CTLMB
5962-9221405MRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221405MRA
CY54FCT245ATDMB	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221403MRA CY54FCT245ATDMB
CY54FCT245CTLMB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221405M2A CY54FCT 245CTLMB
CY54FCT245TLMB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9221401M2A CY54FCT 245TLMB
CY74FCT245ATPC	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT245ATPC
CY74FCT245ATPC.B	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	CY74FCT245ATPC
CY74FCT245ATQCT	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245A
CY74FCT245ATQCT.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CY74FCT245ATQCTG4	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245A
CY74FCT245ATQCTG4.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245A
CY74FCT245ATSOC	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245A
CY74FCT245ATSOC.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245A
CY74FCT245ATSOCT	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245A
CY74FCT245ATSOCT.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245A
CY74FCT245CTQCT	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245C
CY74FCT245CTQCT.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245C
CY74FCT245CTSOC	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245C
CY74FCT245CTSOC.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245C
CY74FCT245TQCT	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245
CY74FCT245TQCT.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245
CY74FCT245TQCTG4	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245
CY74FCT245TQCTG4.B	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT245
CY74FCT245TSOC	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245
CY74FCT245TSOC.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245
CY74FCT245TSOCG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245
CY74FCT245TSOCG4.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245
CY74FCT245TSOCT	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245
CY74FCT245TSOCT.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT245

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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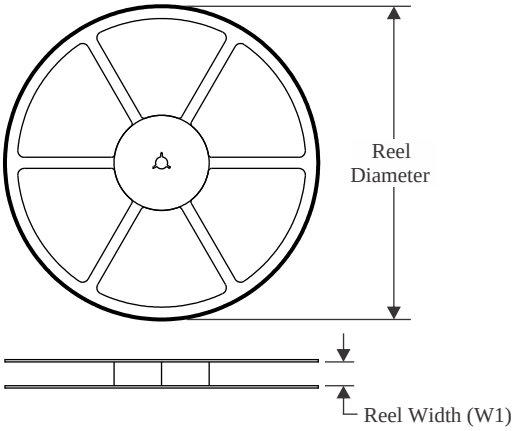
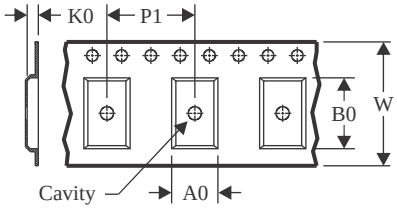
TAPE AND REEL INFORMATION

REEL DIMENSIONS

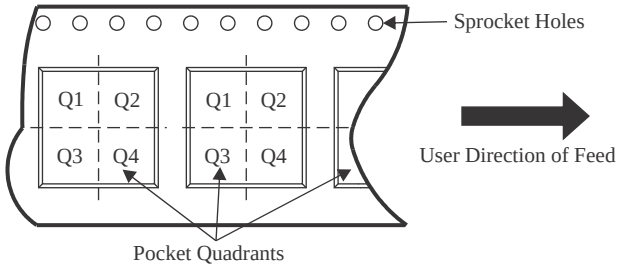


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

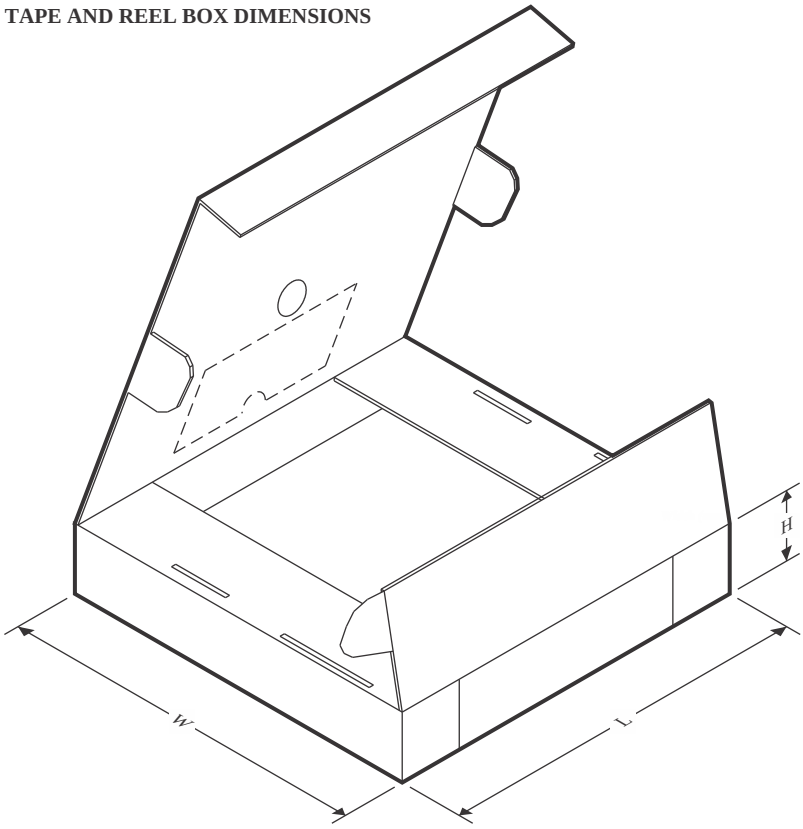
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT245ATQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245ATQCTG4	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245ATSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CY74FCT245CTQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245TQCT	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245TQCTG4	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT245TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

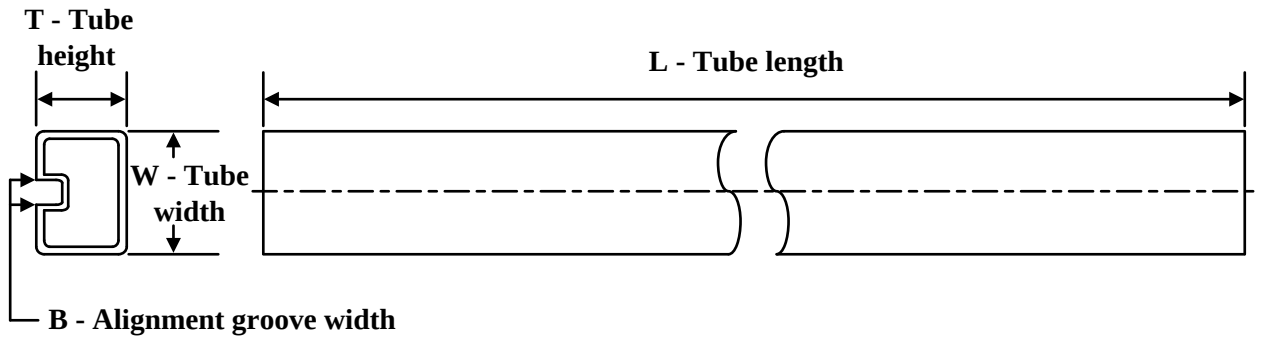
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT245ATQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT245ATQCTG4	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT245ATSOCT	SOIC	DW	20	2000	367.0	367.0	45.0
CY74FCT245CTQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT245TQCT	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT245TQCTG4	SSOP	DBQ	20	2500	356.0	356.0	35.0
CY74FCT245TSOCT	SOIC	DW	20	2000	367.0	367.0	45.0

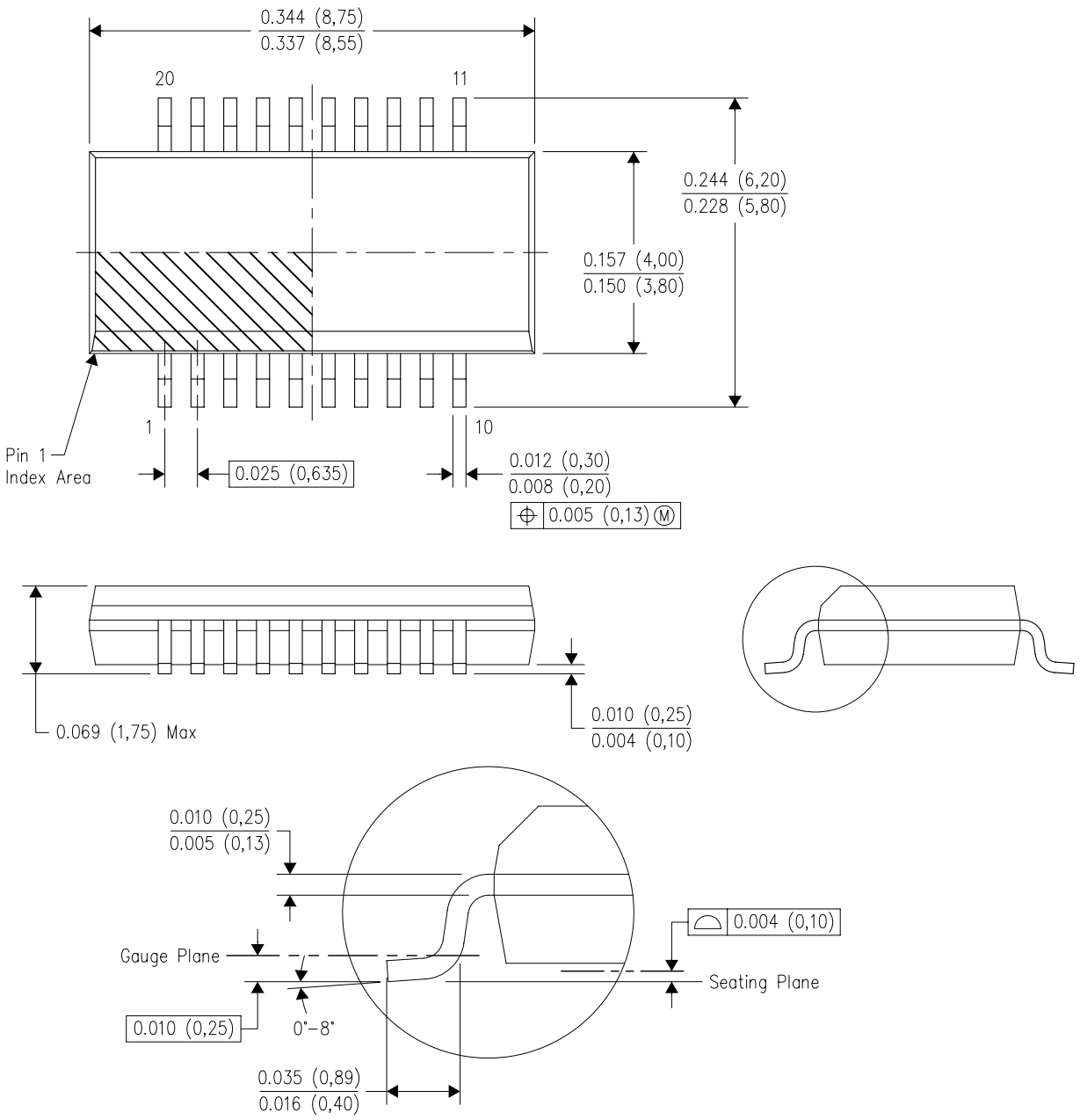
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9221401M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9221403M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9221405M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT245CTLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY54FCT245TLMB	FK	LCCC	20	55	506.98	12.06	2030	NA
CY74FCT245ATPC	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT245ATPC.B	N	PDIP	20	20	506	13.97	11230	4.32
CY74FCT245ATSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT245ATSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT245CTSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT245CTSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT245TSOC	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT245TSOC.B	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT245TSOCG4	DW	SOIC	20	25	507	12.83	5080	6.6
CY74FCT245TSOCG4.B	DW	SOIC	20	25	507	12.83	5080	6.6

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE

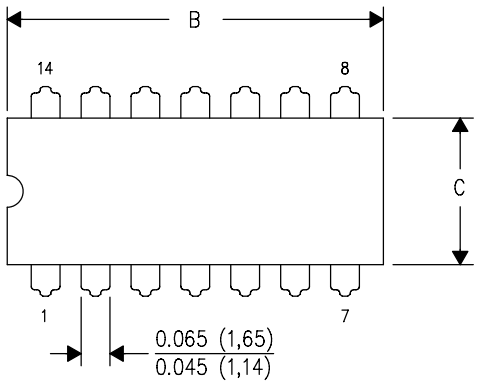


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

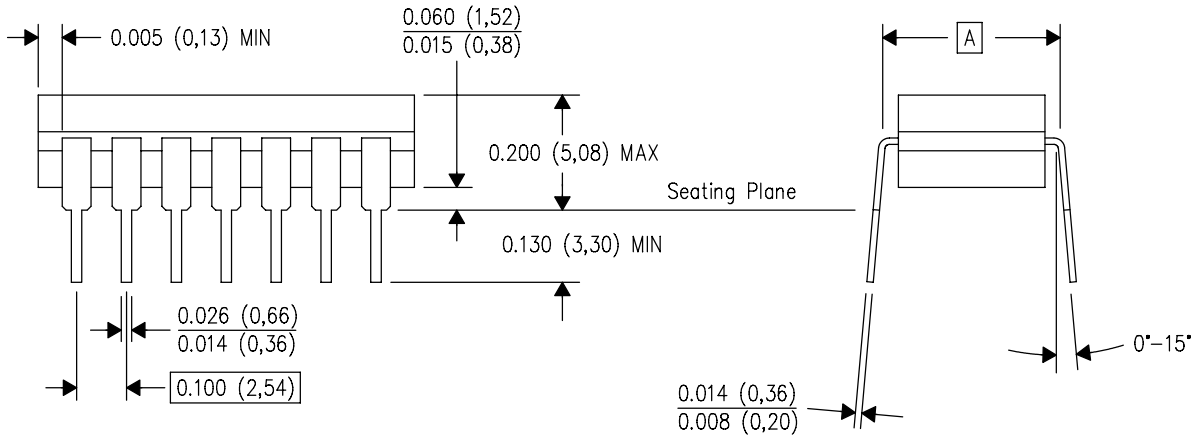
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

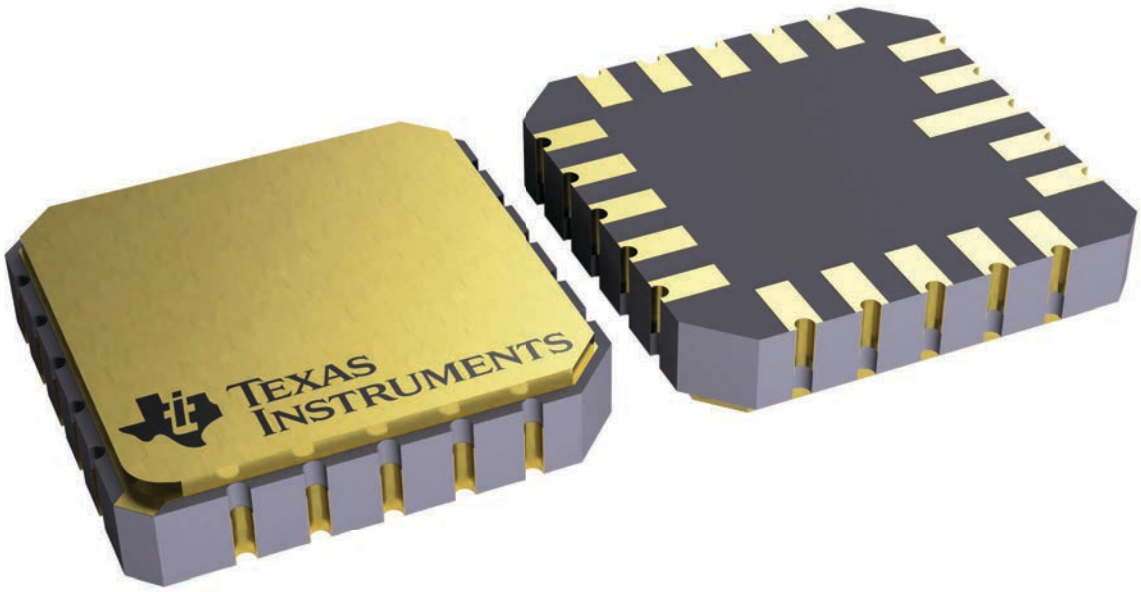
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

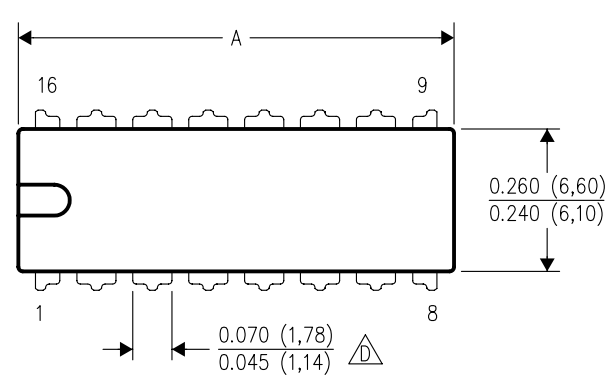


4229370VA\

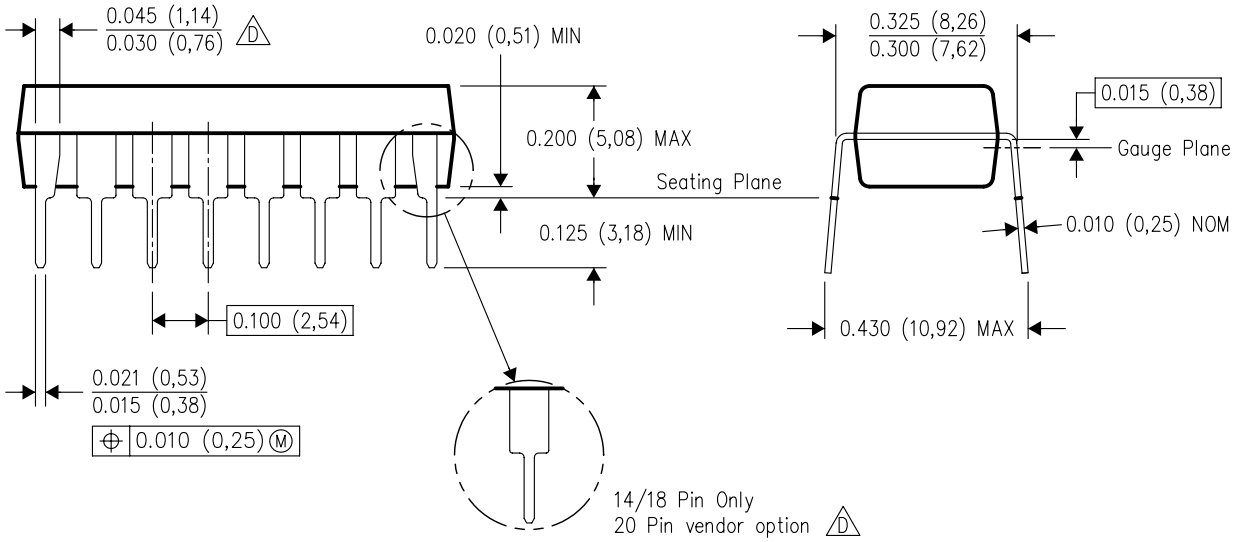
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

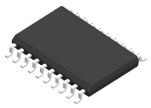


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

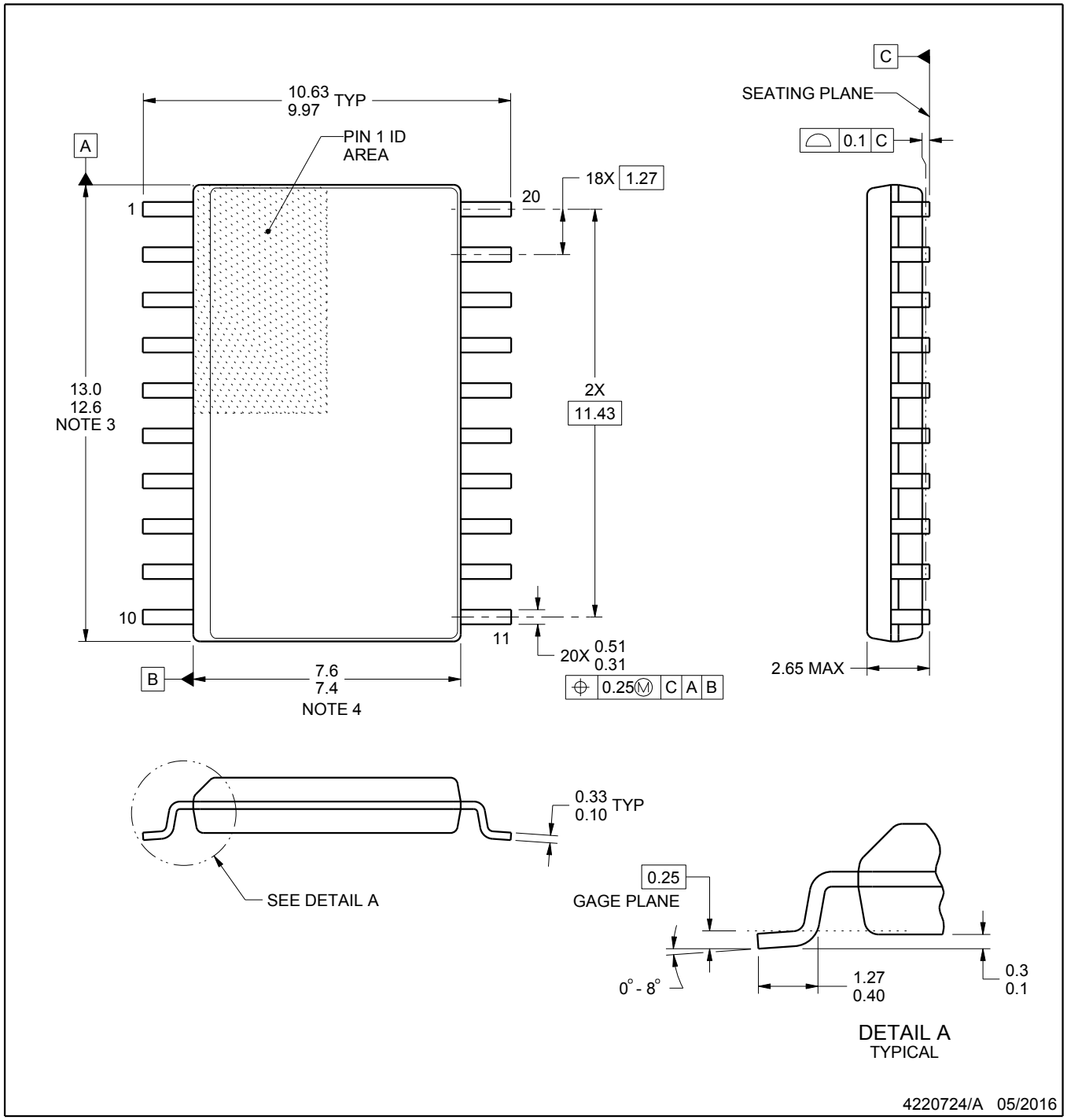


PACKAGE OUTLINE

DW0020A

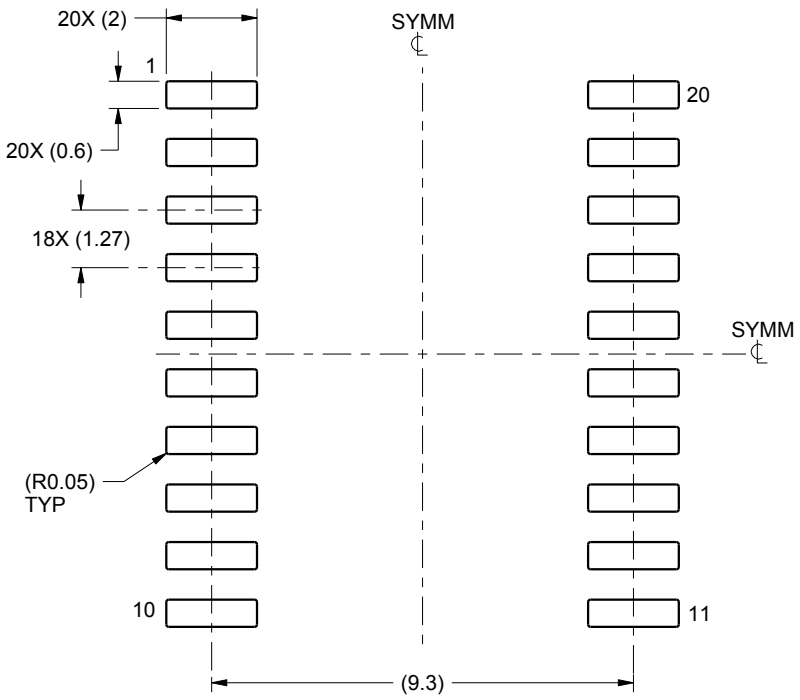
SOIC - 2.65 mm max height

SOIC

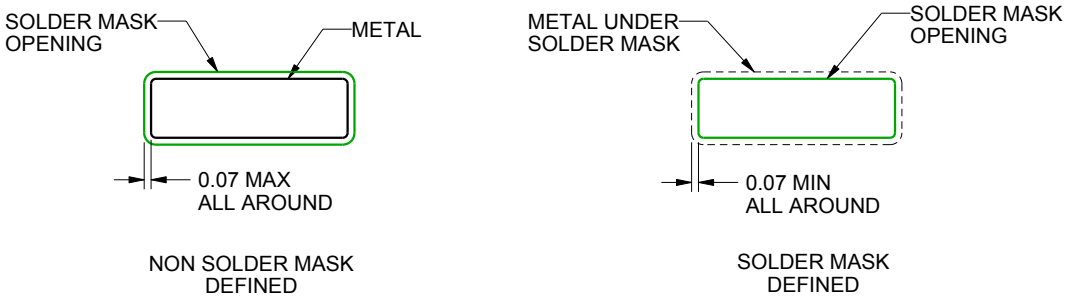


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

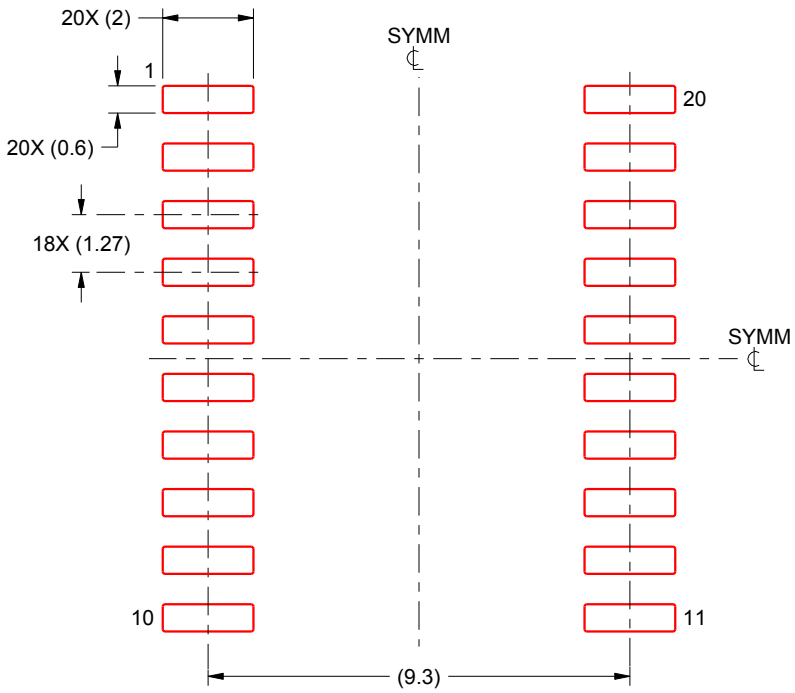


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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