

TLC69629-Q1 Automotive 60mA, 48-Channel LED Driver with Integrated Oscillator , Advance Diagnostics and Cascaded Serial Interface

1 Features

- AEC-Q100 qualified for automotive applications
 - Grade 1: -40°C to 125°C ambient operating temperature
 - Device HBM classification level H1C
 - Device CDM classification level C4B
- Targeted **Functional Safety-Compliant**
 - Developed for functional safety applications
 - Documentation available to aid ISO 26262 system design up to ASIL B
- 48 integrated current sinks
 - Programmable 16-bit PWM / Hybrid dimming
 - Programmable 7-bit analog dot correction (DC)
 - Maximum output current / voltage: 60mA / 16V
- Integrated 33MHz oscillator
 - 16-bit PWM output in 500Hz
 - $>20\text{KHz}$ refresh rate with enhanced spectrum (ES) PWM
- High speed communication
 - Cascaded serial interface (CSI)
 - Data rates up to 17Mbps
- Power efficiency optimization
 - Adaptive headroom voltage control (AHVC)
 - Device power save mode (PSM)
- EMI mitigation
 - Interface: programmable buffer driving capability
 - Current sinks: phase shifting / spread spectrum
- Protection and Diagnostic
 - LED: open / short detection / health check
 - Current sink: adjacent-pin short / health check
 - Interface: CRC / command error / time-out error / communication watchdog
 - Device: under voltage / ISET out of range / thermal shutdown / memory CRC / OTP CRC / OSC watchdog

2 Applications

- Automotive Central Information Display
- Automotive Cluster Display
- Automotive Head-up Display

3 Description

The TLC69629-Q1 is a LED driver with 48 constant current sink channels which could provide up to 16-bit individual pixel-level LED PWM control. The additional 7-bit dot correction (DC) is also implemented to each channel to control peak current. Each device shares data stream by cascaded serial interface (CSI) which supports up to 511 devices connection. The interface is **software compatible with LED drivers in the same group** which can be applied to different application scenarios based on LED current and total LED number.

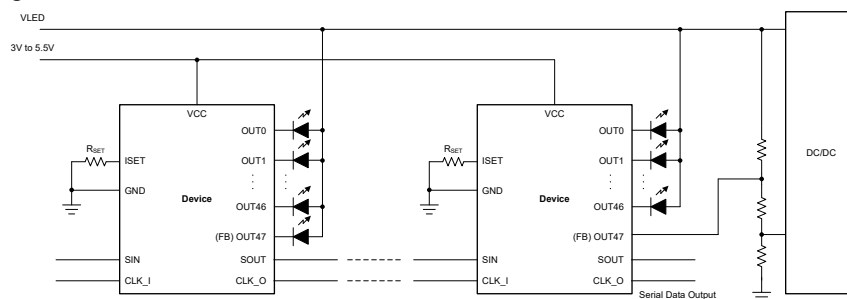
To optimize overall systematic power efficiency, the device is equipped with adaptive headroom voltage control (AHVC) scheme to optimize headroom voltage across each channel and device. Only the OUT47 pin from the last device of daisy chain is required to be programmed as FB pin to optimize LED supply voltage from DC/DC.

The TLC69629-Q1 is equipped diagnostics for LED, current sink, communication and device.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TLC69629-Q1	VQFN (56) Wettable flank	8mm × 8mm
	HTSSOP (56)	14mm × 6.1mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

Table of Contents

1 Features	1	5.3 Trademarks.....	4
2 Applications	1	5.4 Electrostatic Discharge Caution.....	4
3 Description	1	5.5 Glossary.....	4
4 Device Comparison	3	6 Revision History	4
5 Device and Documentation Support	4	7 Mechanical, Packaging, and Orderable Information	5
5.1 Receiving Notification of Documentation Updates.....	4	7.1 Tape and Reel Information.....	15
5.2 Support Resources.....	4		

ADVANCE INFORMATION

4 Device Comparison

PART NUMBER	CHANNEL NUMBER	MAX. CHANNEL CURRENT	FUNCTIONAL SAFETY CLASSIFICATION	INTERFACE	SOFTWARE COMPATIBLE
TLC69621-Q1 ⁽¹⁾	8	60mA	Functional Safety-Capable	SPI	Group 1
TLC69624-Q1 ⁽¹⁾	24				
TLC69627-Q1	48				
TLC69631-Q1 ⁽¹⁾	8	100mA			
TLC69634-Q1 ⁽¹⁾	24				
TLC69637-Q1	48				
TLC69622-Q1 ⁽¹⁾	8	60mA	Functional Safety-Compliant	SPI	Group 2
TLC69625-Q1 ⁽¹⁾	24				
TLC69628-Q1	48				
TLC69632-Q1 ⁽¹⁾	8	100mA			
TLC69635-Q1 ⁽¹⁾	24				
TLC69638-Q1	48				
TLC69623-Q1 ⁽¹⁾	8	60mA	Functional Safety-Compliant	CSI	Group 3
TLC69626-Q1 ⁽¹⁾	24				
TLC69629-Q1	48				
TLC69633-Q1 ⁽¹⁾	8	100mA			
TLC69636-Q1 ⁽¹⁾	24				
TLC69639-Q1	48				

(1) Product preview

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

5.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

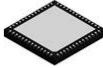
6 Revision History

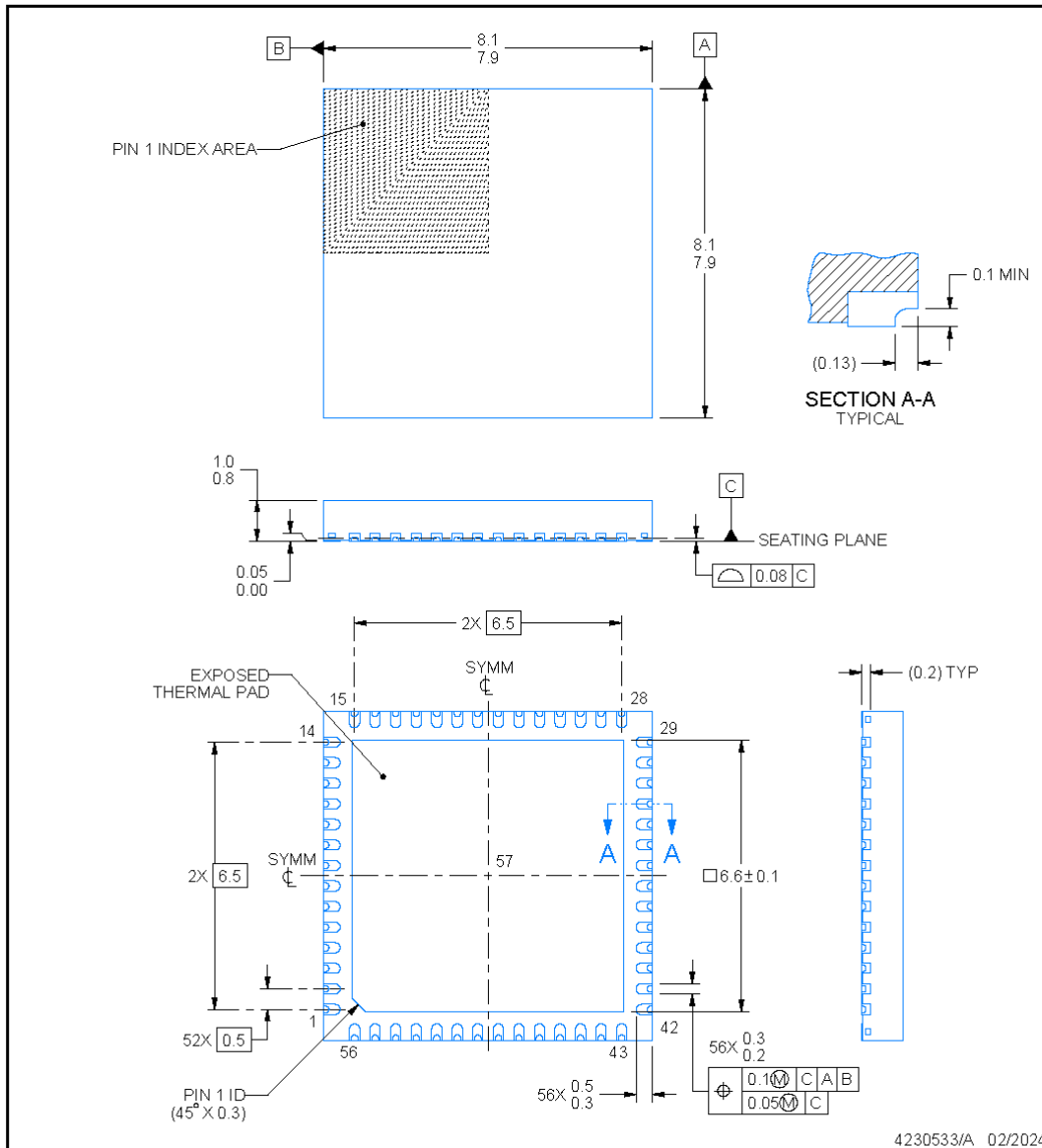
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2025	*	Advance Information Release

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

RTQ0056K  **PACKAGE OUTLINE**
VQFN - 1 mm max height
PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

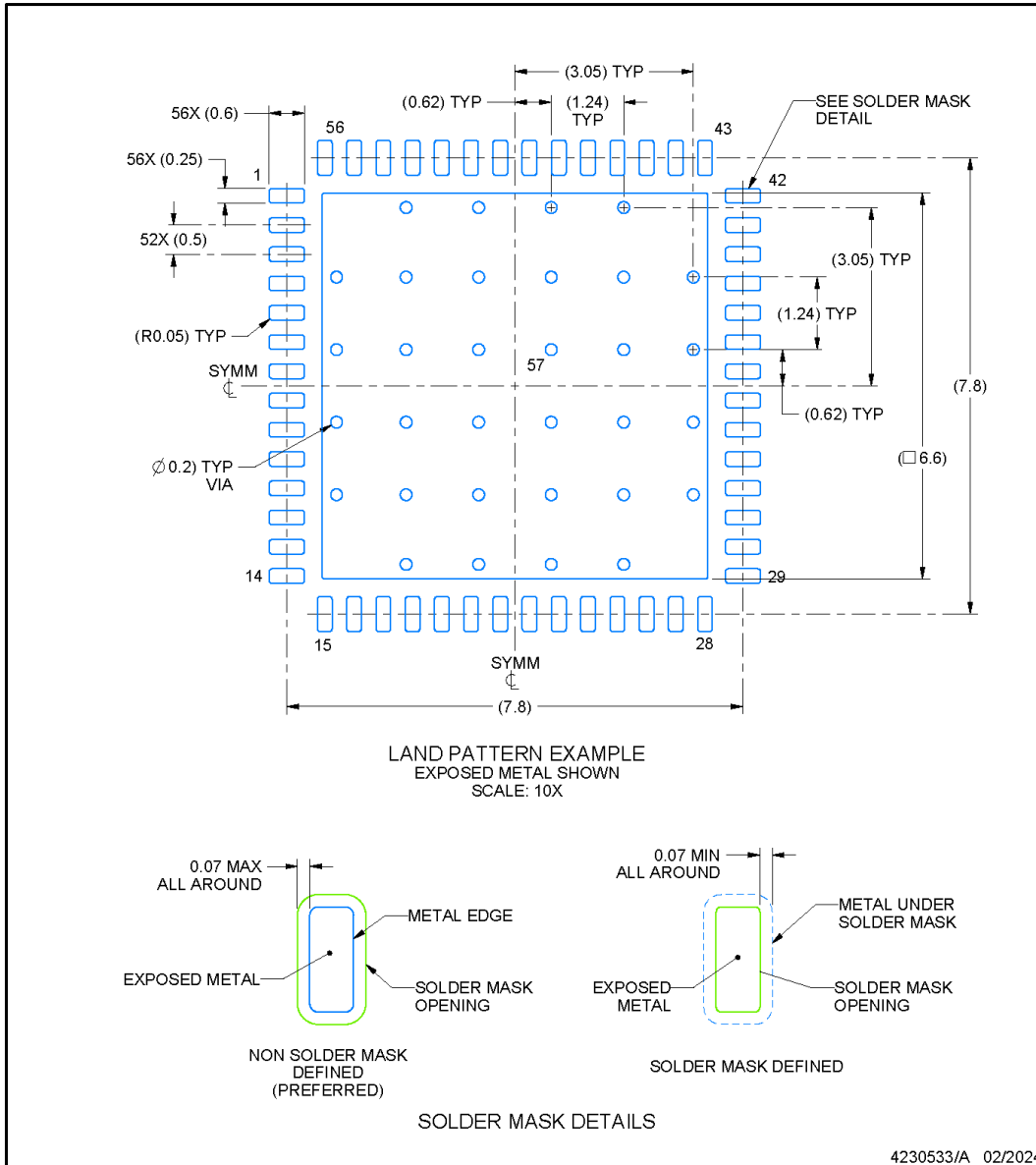
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

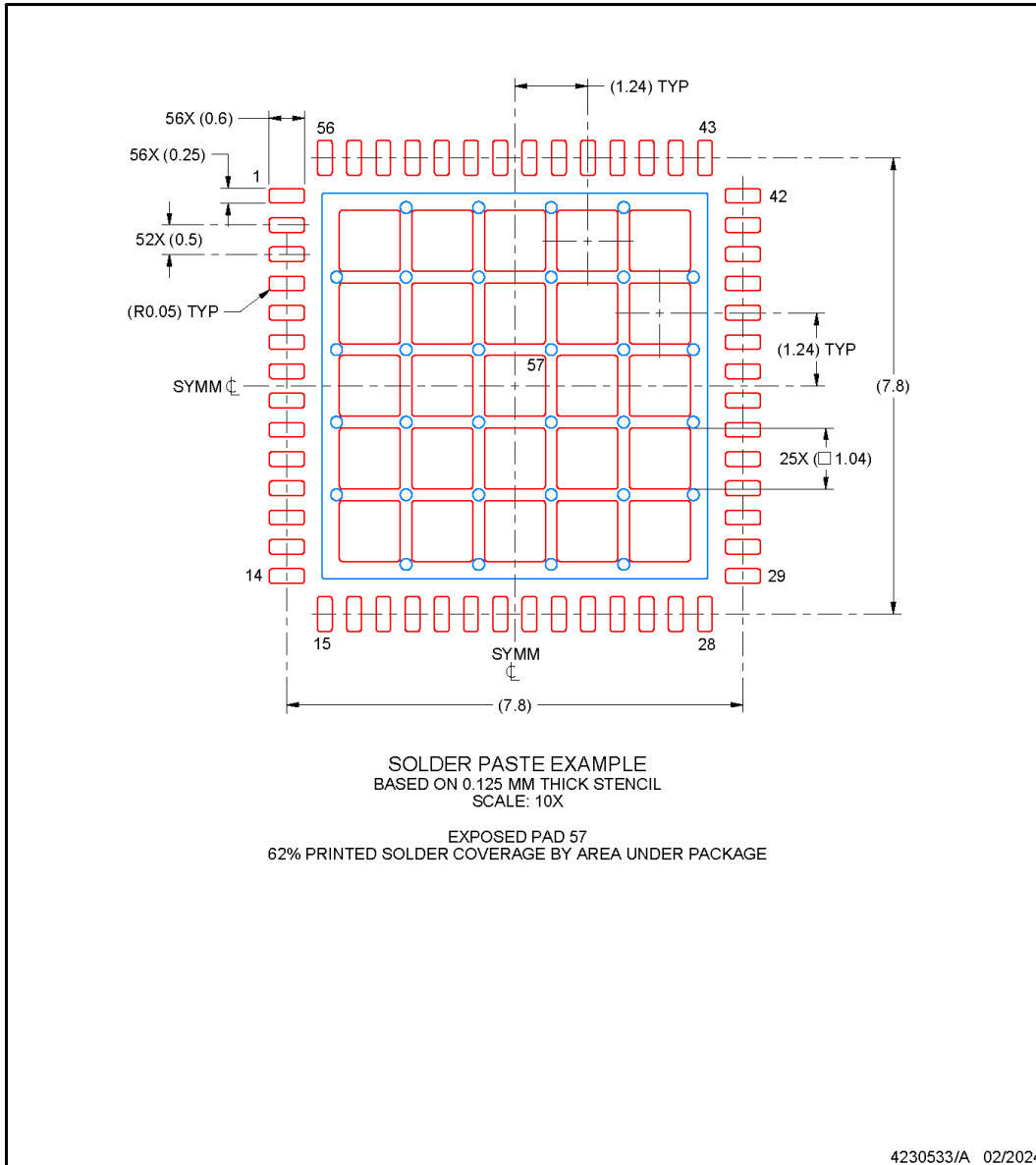
EXAMPLE STENCIL DESIGN

RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

ADVANCE INFORMATION



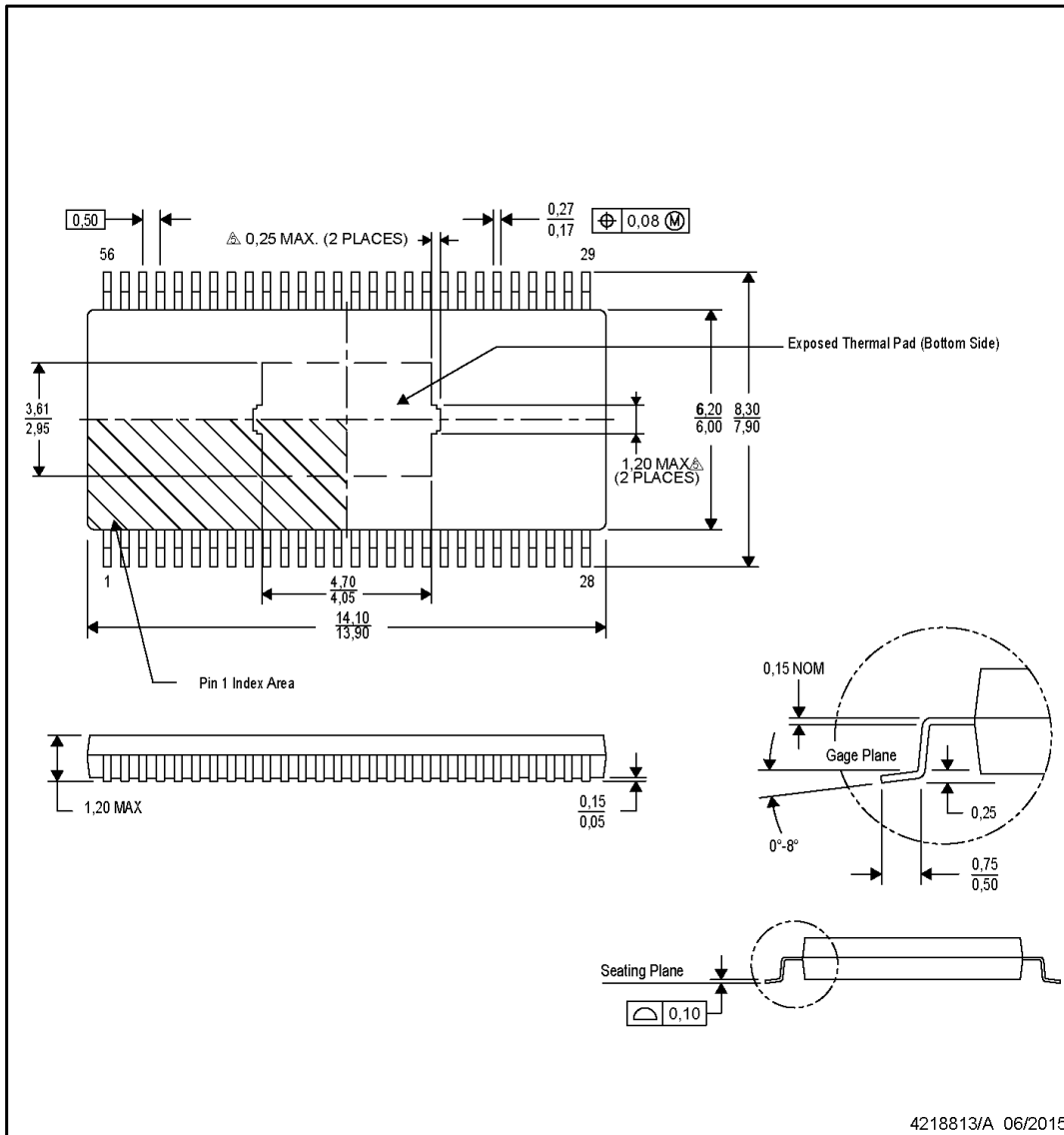
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE
HTSSOP - 1.2 mm max height

PowerPAD™ HTSSOP

DCA0056F



NOTES:

PowerPAD is a trademark of Texas Instruments

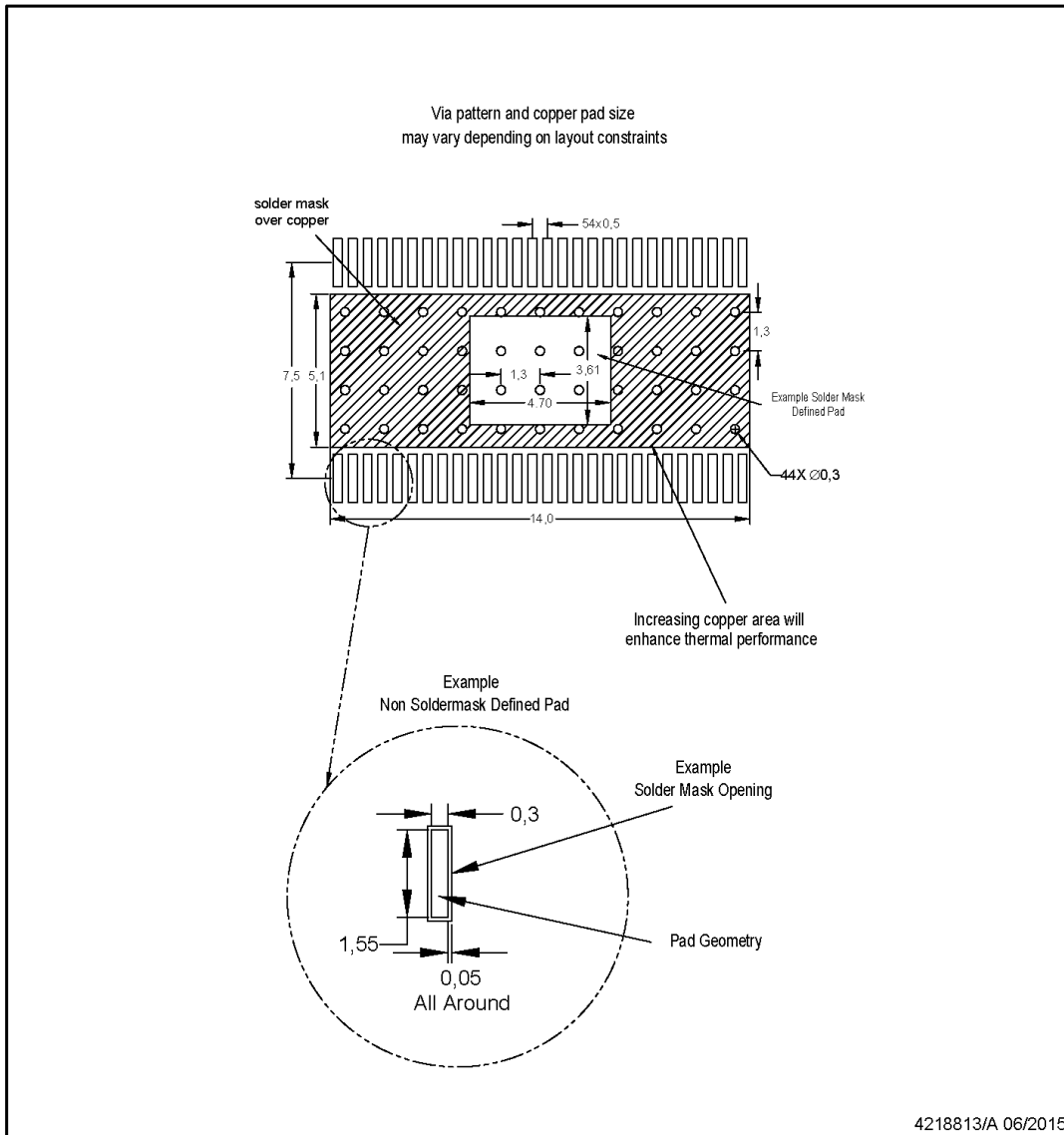
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This package falls within JEDEC MO-153.
5. Keep-out features are identified to prevent board routing interference. These exposed metal features may vary within the identified area or completely absent on some devices.

EXAMPLE BOARD LAYOUT
HTSSOP - 1.2 mm max height

DCA0056F

PowerPAD™ HTSSOP

ADVANCE INFORMATION



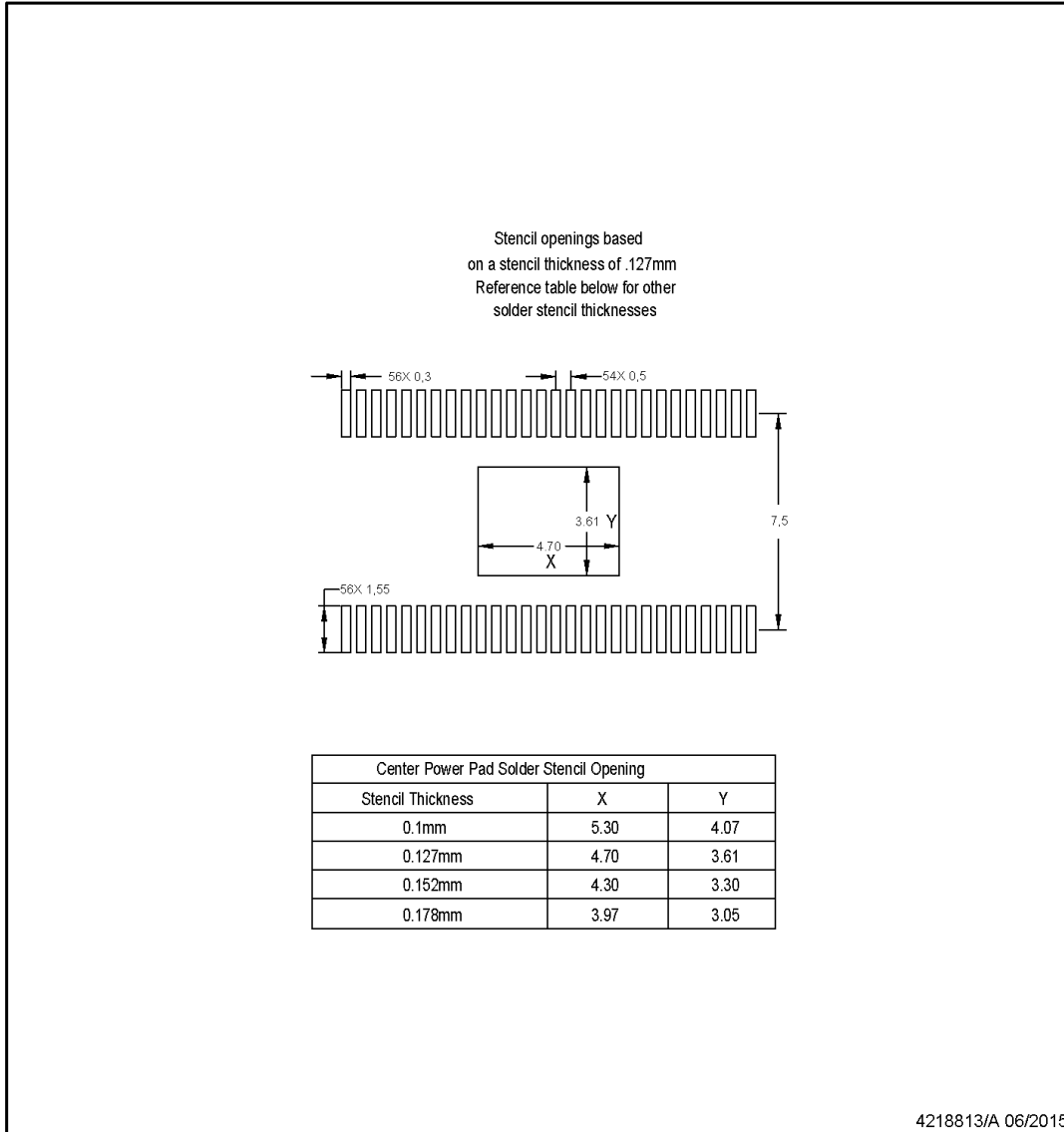
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. Refer to technical brief, Powerpad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN
HTSSOP - 1.2 mm max height

DCA0056F

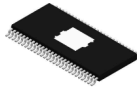
PowerPAD™ HTSSOP



NOTES: (continued)

- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

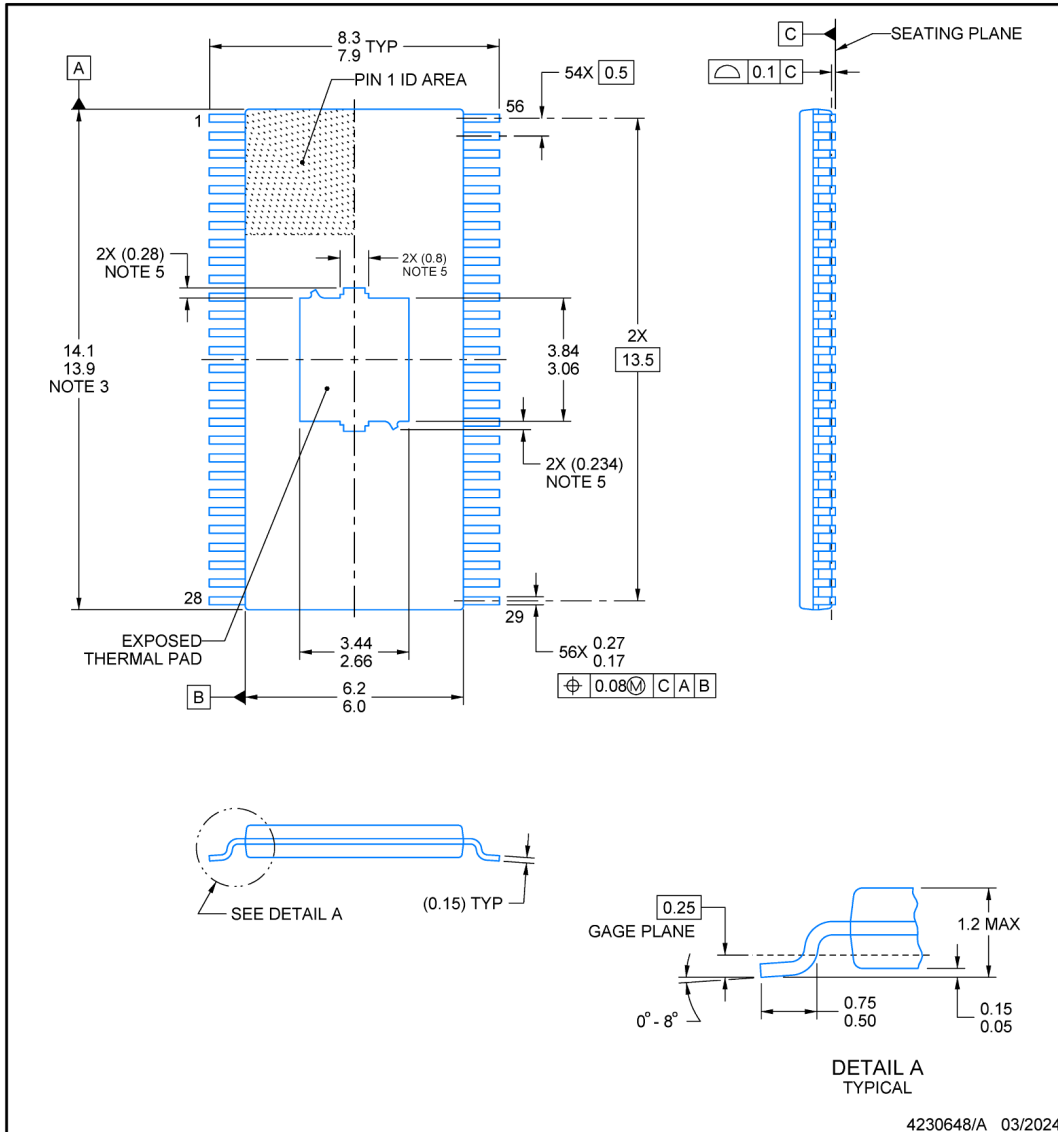


PACKAGE OUTLINE

DFD0056D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



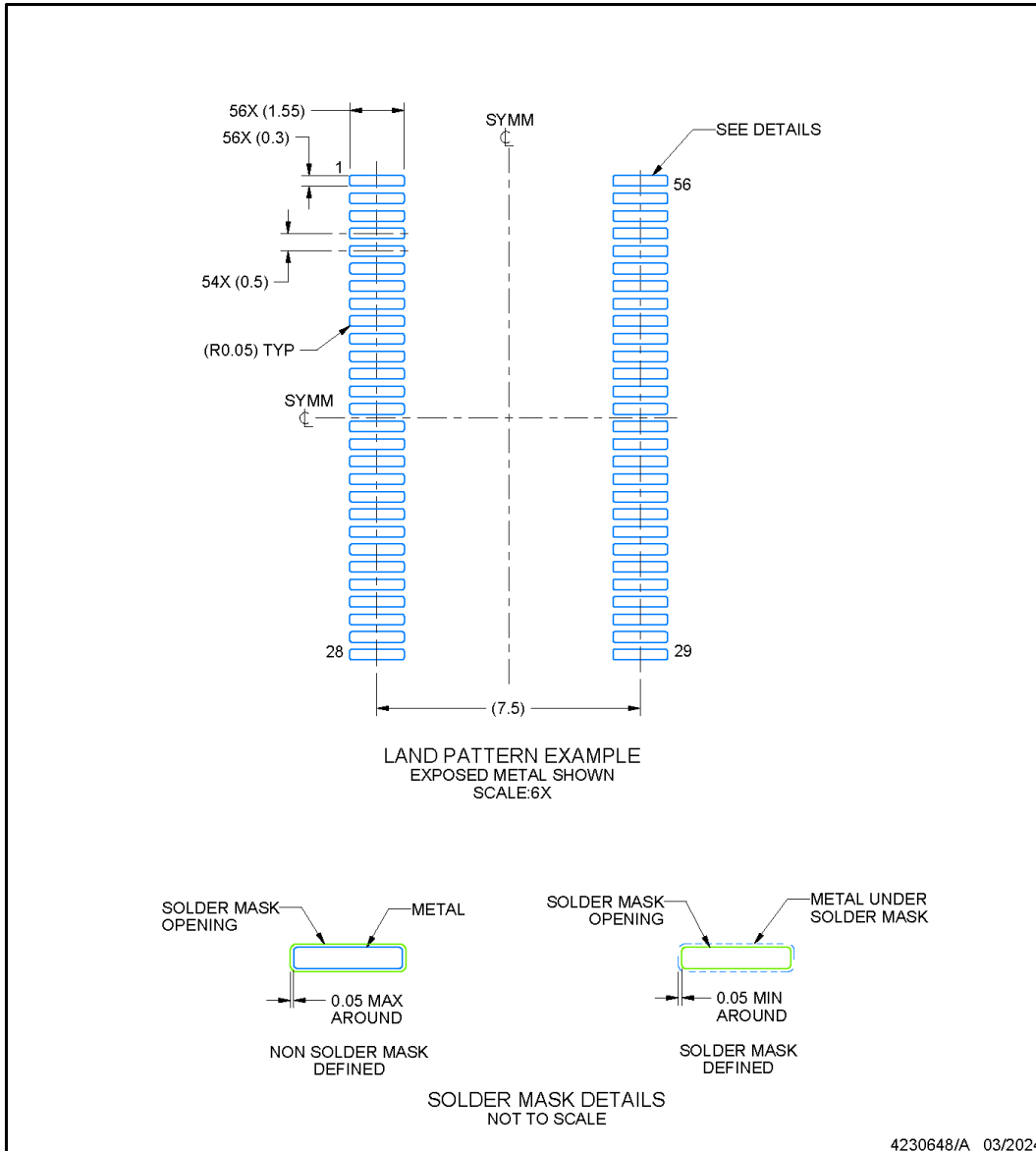
- NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.
 5. Features may not present.
 6. This package incorporates an exposed thermal pad that is designed to be attached directly to an external heat sink. This optimizes the heat transfer from the integrated circuit (IC).
- PowerPAD is a trademark of Texas Instruments.

EXAMPLE BOARD LAYOUT

DFD0056D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

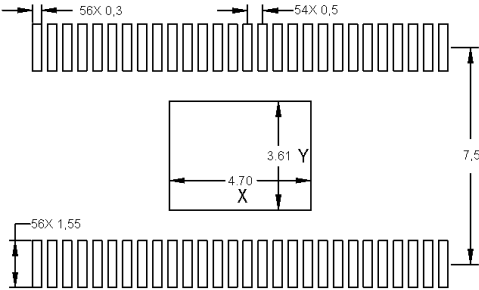
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN
HTSSOP - 1.2 mm max height

DCA0056F

PowerPAD™ HTSSOP

Stencil openings based
on a stencil thickness of .127mm
Reference table below for other
solder stencil thicknesses



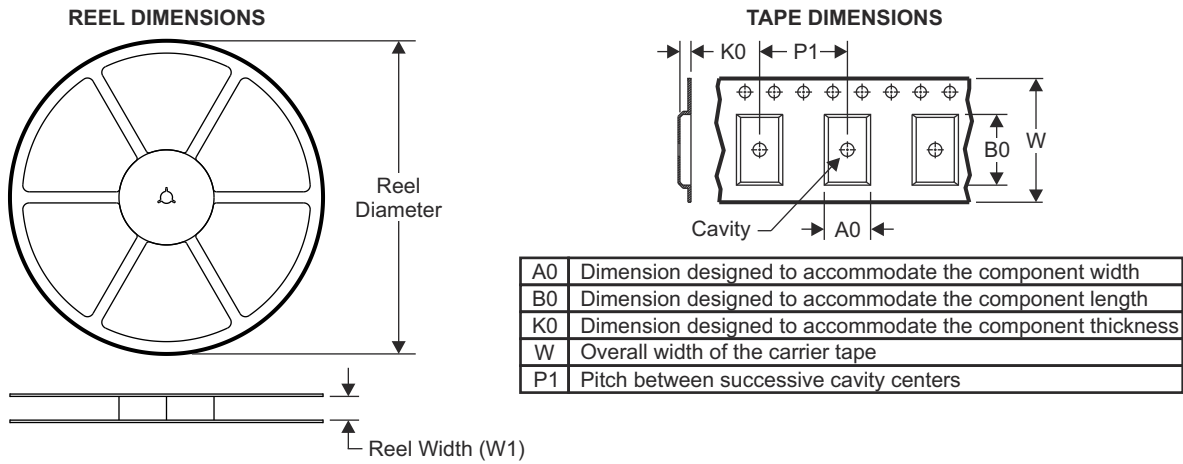
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.30	4.07
0.127mm	4.70	3.61
0.152mm	4.30	3.30
0.178mm	3.97	3.05

4218813/A 06/2015

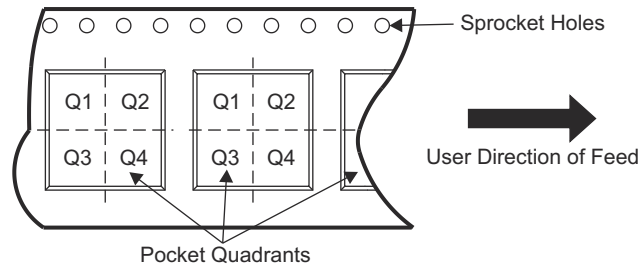
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

7.1 Tape and Reel Information



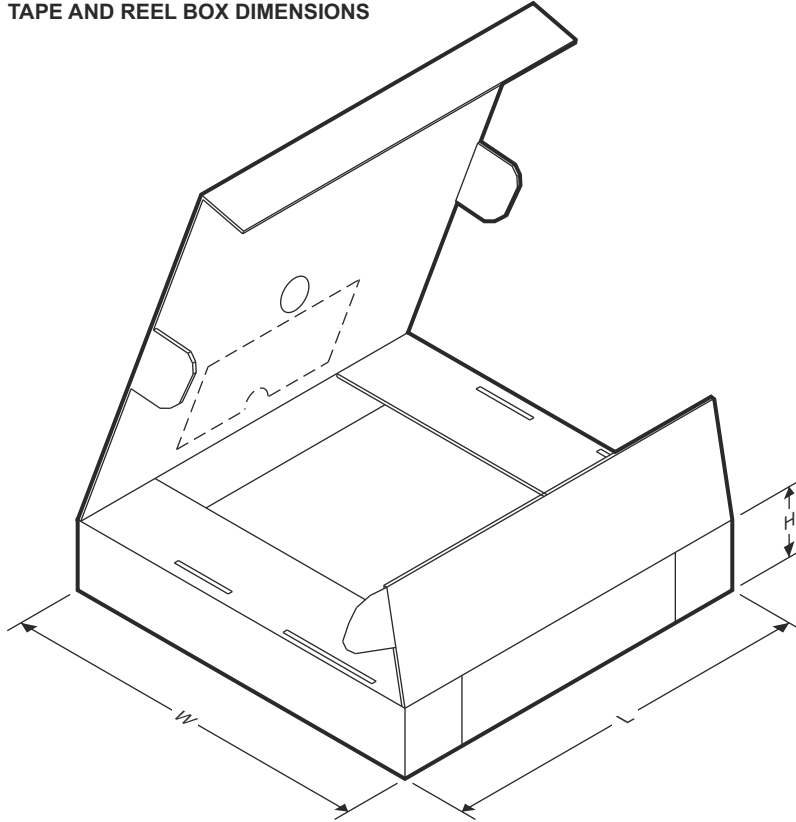
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC69629QDCARQ1	HTSSOP	DCA	56	2500	330	24.4	8.6	15.6	1.8	12	24	Q1
TLC69629QRTQRQ1	VQFN	RTQ	56	3500	330	16.4	8.3	8.3	1.1	12	16	Q2
TLC69629QDFDRQ1	HTSSOP	DFD	56	2500	330	24.4	8.9	14.7	1.4	12	24	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC69629QDCARQ1	HTSSOP	DCA	56	2500	367	367	45
TLC69629QRTQRQ1	VQFN	RTQ	56	3500	367	367	35
TLC69629QDFDRQ1	HTSSOP	DFD	56	2500	350	350	43

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTLC69629QRTQRQ1	Active	Preproduction	QFN (RTQ) 56	3500 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTLC69629QRTQRQ1.A	Active	Preproduction	QFN (RTQ) 56	3500 LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

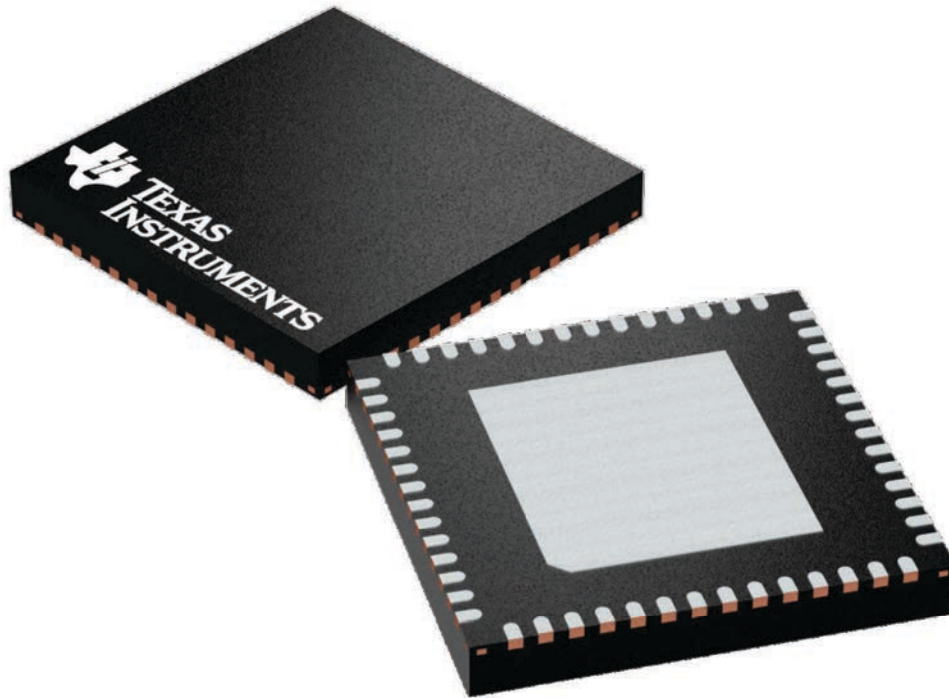
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

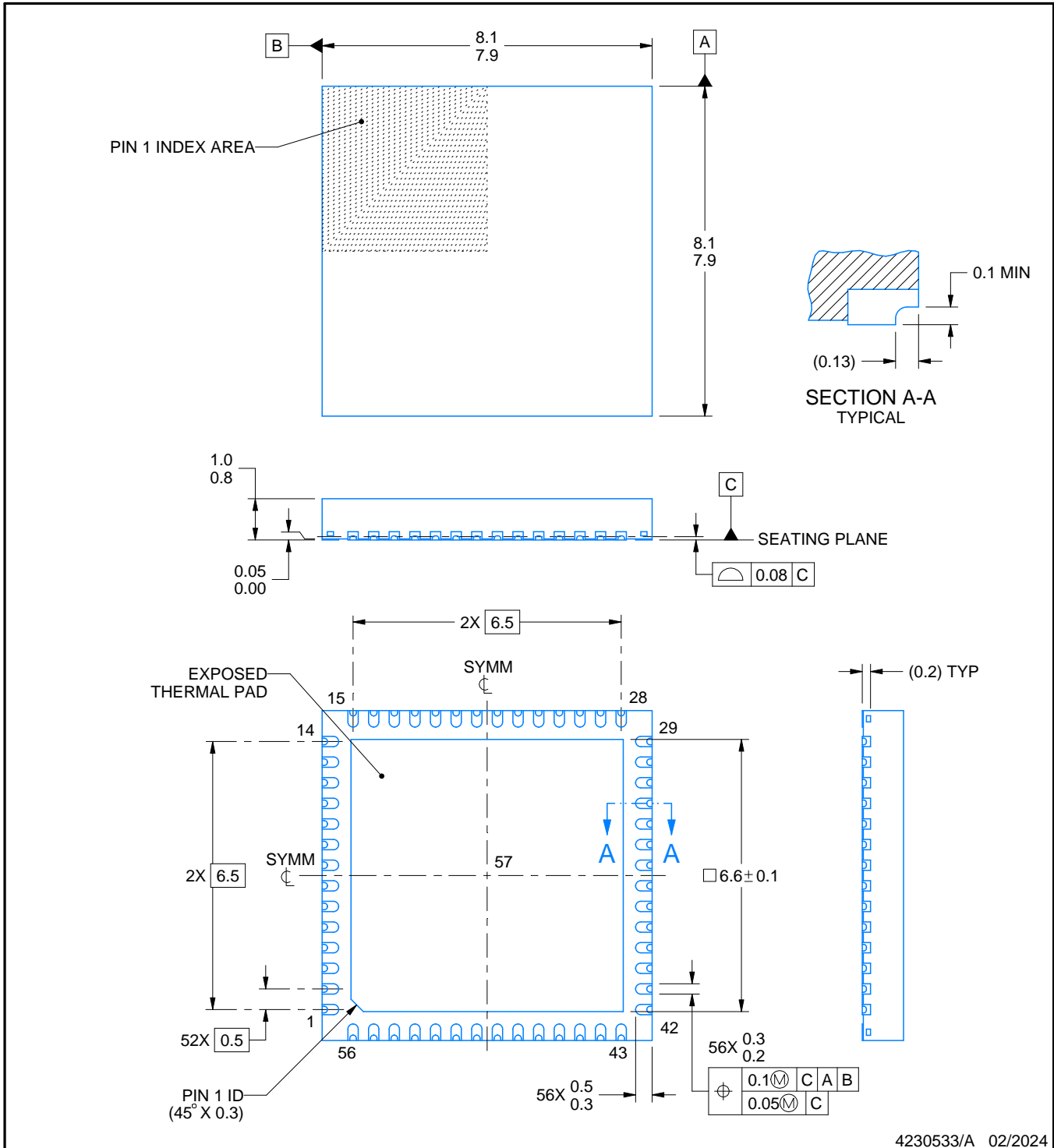
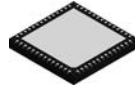
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224653/A



4230533/A 02/2024

NOTES:

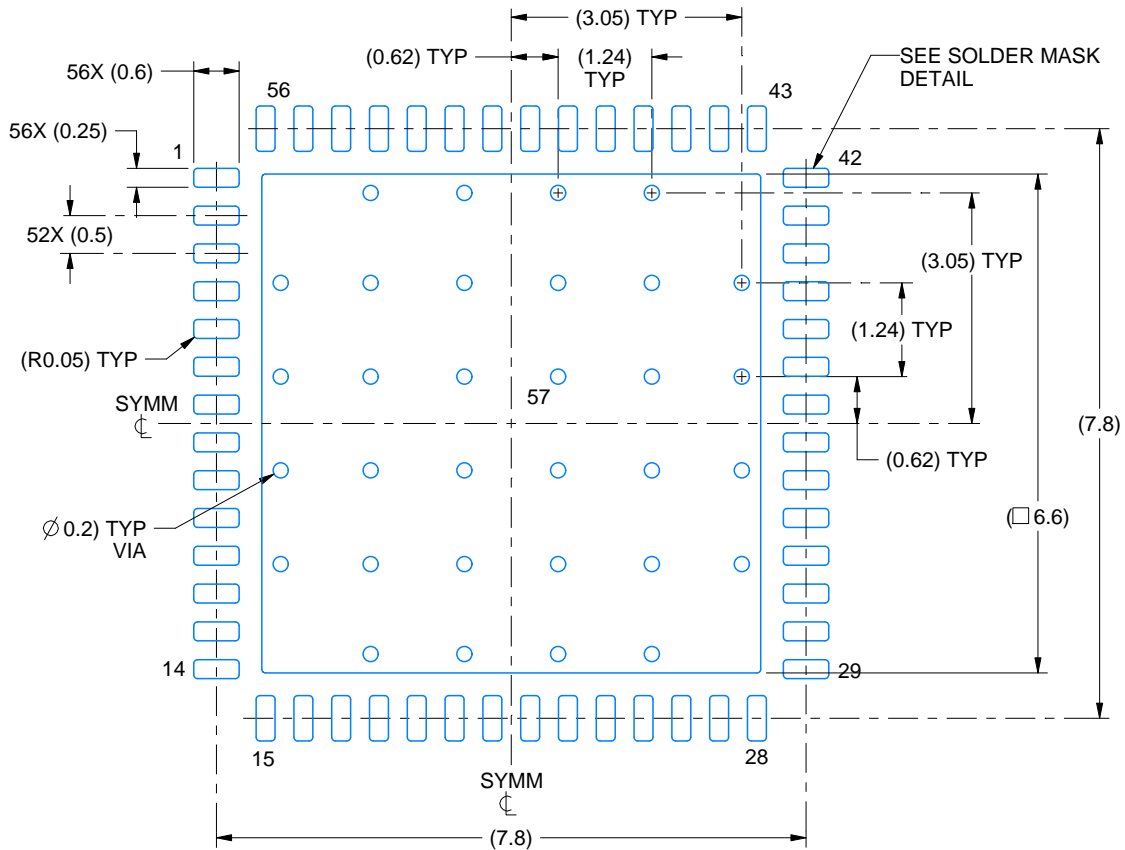
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

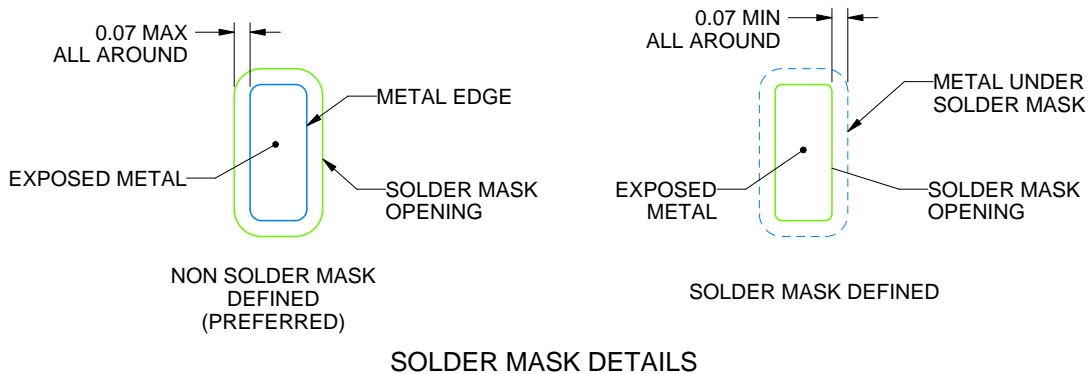
RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4230533/A 02/2024

NOTES: (continued)

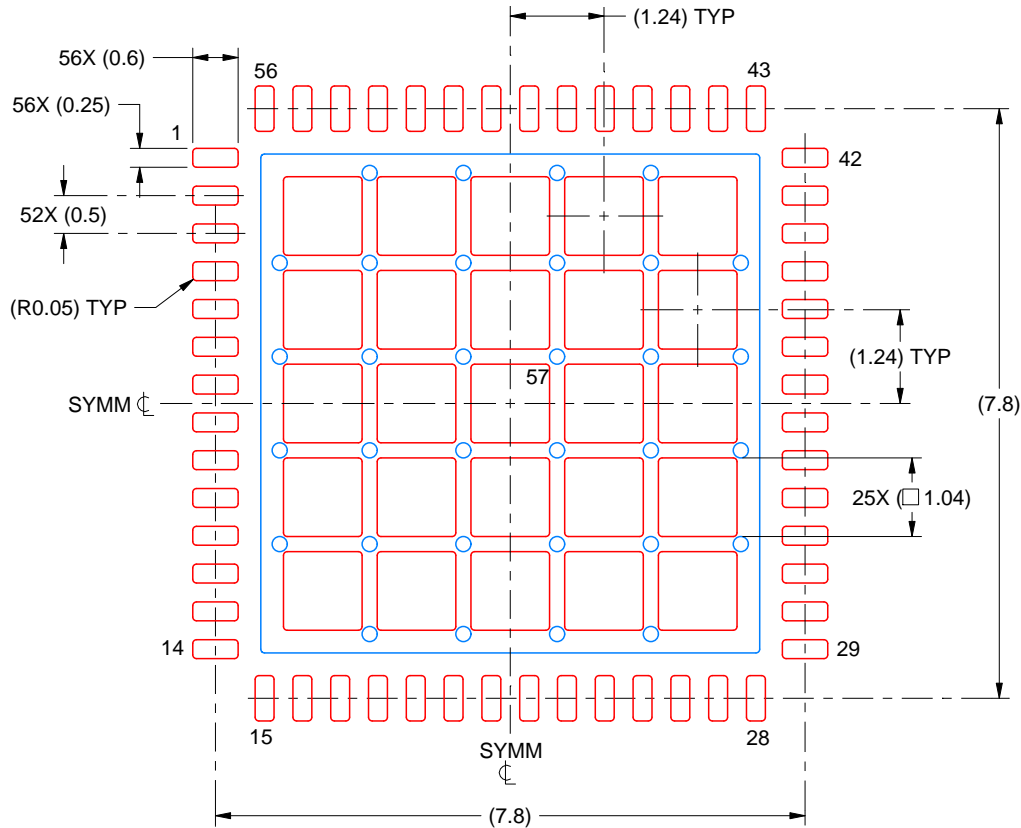
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTQ0056K

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
62% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4230533/A 02/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated