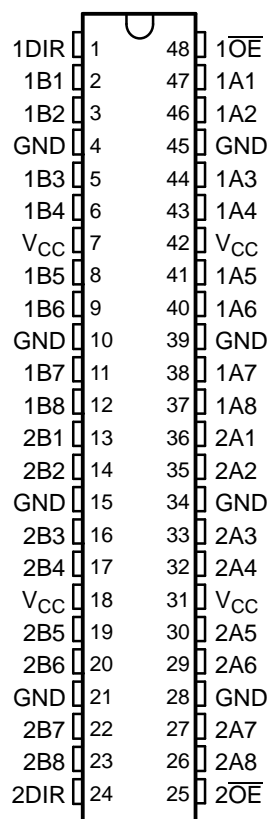


FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Latch-Up Performance Exceeds 500 mA Per JESD 70
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Includes Plastic Thin Very Small-Outline (DGV), Shrink Small-Outline (DL), and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic (WD) Flat Package Using 25-mil Center-to-Center Spacings

SN54ABT16245A . . . WD PACKAGE
SN74ABT16245A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



DESCRIPTION

The 'ABT16245A devices are 16-bit noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16245A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16245A is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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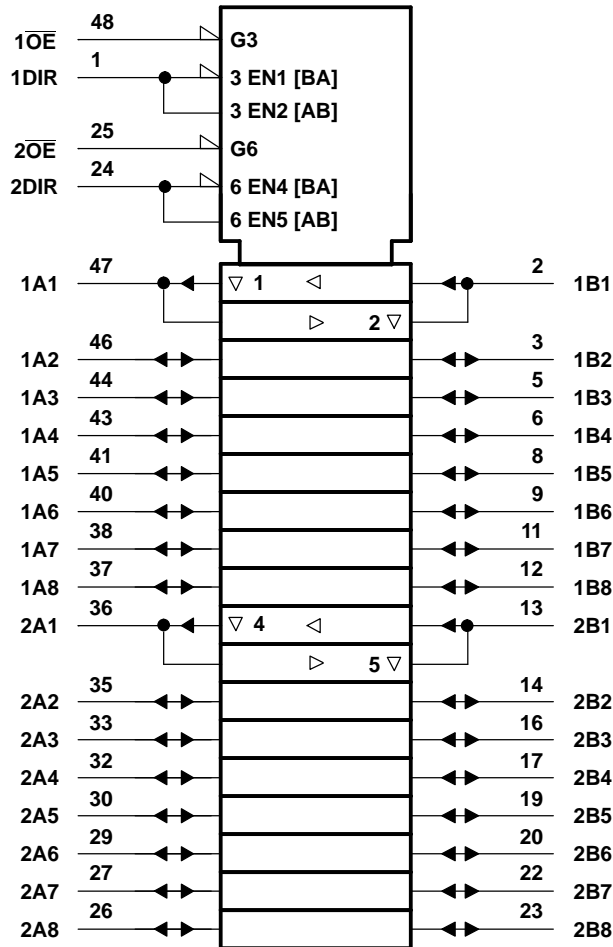
SN54ABT16245A, SN74ABT16245A
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS300G—MARCH 1994—REVISED JANUARY 2006

FUNCTION TABLE
(EACH 8-BIT SECTION)

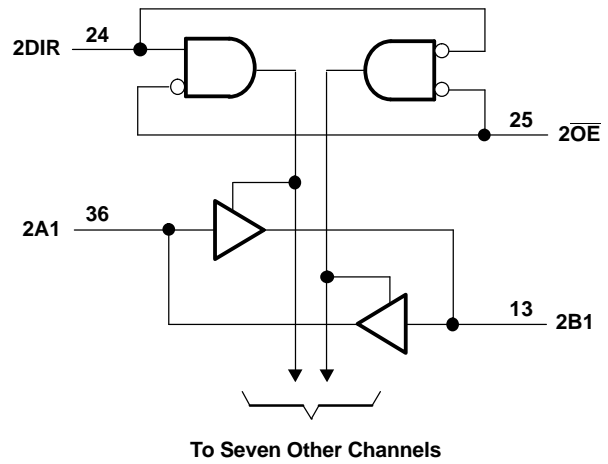
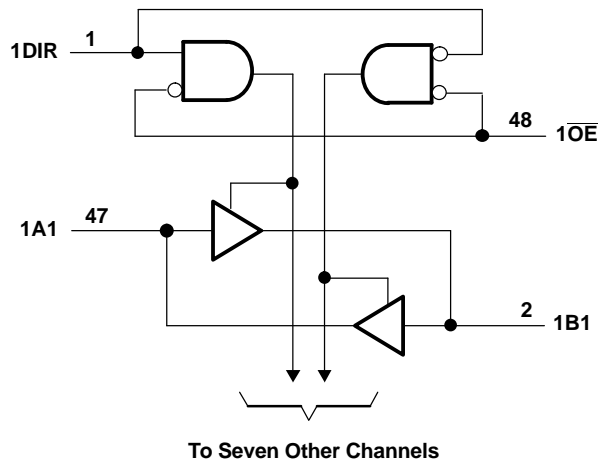
INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC SYMBOL ⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I	Input voltage range (except I/O ports) ⁽²⁾	-0.5	7	V
V_O	Voltage range applied to any output in the high or power-off state	-0.5	5.5	V
I_O	Current into any output in the low state	SN54ABT16245A		mA
		SN74ABT16245A		
I_{IK}	Input clamp current	$V_I < 0$		-18
I_{OK}	Output clamp current	$V_O < 0$		-50
θ_{JA}	Package thermal impedance ⁽³⁾	DGG package		89
		DGV package		93
		DL package		94
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51.

SN54ABT16245A, SN74ABT16245A 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS300G—MARCH 1994—REVISED JANUARY 2006

Recommended Operating Conditions⁽¹⁾

		SN54ABT16245A		SN74ABT16245A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		-24		-32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μ s/V
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}$ C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT16245A		SN74ABT16245A		UNIT		
			MIN	TYP ⁽¹⁾	MAX	MIN	MAX	MIN	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		-1.2		V		
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA		2.5			2.5		2.5		V		
	V _{CC} = 5 V, I _{OH} = -3 mA		3			3		3				
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2						
I _{OH} = -32 mA		2 ⁽²⁾					2					
V _{OL}	V _{CC} = 4.5 V		I _{OL} = 48 mA			0.55				V		
			I _{OL} = 64 mA			0.55 ⁽²⁾		0.55				
V _{hys}			100							mV		
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA	
	A or B port	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND		±20 ⁽²⁾			±100		±20			
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$		±50 ⁽³⁾			±50 ⁽³⁾		±50		μA		
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$		±50 ⁽³⁾			±50 ⁽³⁾		±50		μA		
I _{OZH} ⁽⁴⁾	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V		10 ⁽⁵⁾			10		10 ⁽⁵⁾		μA		
I _{OZL} ⁽⁴⁾	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≥ 2 V		-10 ⁽⁵⁾			-10		-10 ⁽⁵⁾		μA		
I _{off}	V _{CC} = 0, V _I or V _O ≤ 5.5 V		±100					±100		μA		
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V		Outputs high		50			50		50	μA	
I _O ⁽⁶⁾	V _{CC} = 5.5 V, V _O = 2.5 V		-50	-100	-180	-50	-180	-50	-180	mA		
I _{CC}	A or B port	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		Outputs high		2		2		2		mA
				Outputs low		32		32		32		
				Outputs disabled		2		2		2		
ΔI _{CC} ⁽⁷⁾	Data inputs	V _{CC} = 5.5 V, One inputs at 3.4 V, Other inputs at V _{CC} or GND		Outputs enabled		2		1.5		2		mA
				Outputs disabled		0.05		1		0.05		
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5		1.5		1.5				
C _i	Control inputs	V _I = 2.5 V or 0.5 V		3							pF	
C _o	A or B port	V _O = 2.5 V or 0.5 V		6							pF	

 (1) All typical values are at V_{CC} = 5 V.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

 (4) The parameters I_{OZH} and I_{OZL} include the input leakage current.

(5) This limit may vary among suppliers.

(6) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

 (7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN54ABT16245A, SN74ABT16245A 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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Switching Characteristics

over recommended operating ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF
(unless otherwise noted) (see [Figure 1](#))

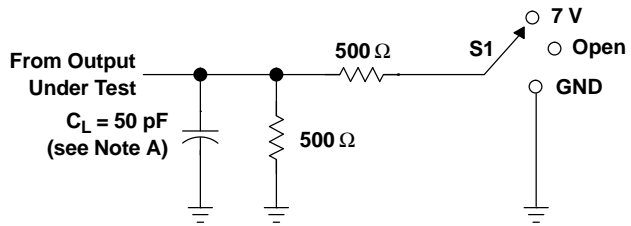
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT16245A					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	0.5	2.2	3.4	0.5	4	ns
t_{PHL}			0.5	2.3	3.8	0.5	4.6	
t_{PZH}	\overline{OE}	B or A	0.8	3.6	5.2	0.8	5.5	ns
t_{PZL}			0.9	3.7	6.1	0.1	7.3	
t_{PHZ}	\overline{OE}	B or A	1.3	4.4	5.8	1.3	6.3	ns
t_{PLZ}			1.4	3.3	4.7	1.4	5.5	

Switching Characteristics

over recommended operating ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF
(unless otherwise noted) (see [Figure 1](#))

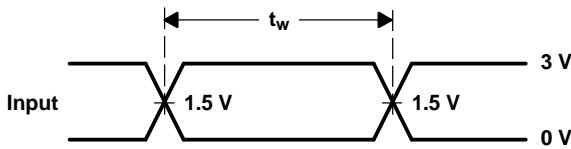
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT16245A					UNIT
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN	MAX	
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1	2.2	3.4	1	3.9	ns
t_{PHL}			1	2.3	3.7	1	4.2	
t_{PZH}	\overline{OE}	B or A	1	3.6	5.2	1	6.3	ns
t_{PZL}			1	3.7	5.4	1	6.4	
t_{PHZ}	\overline{OE}	B or A	2	4.4	5.8	2	6.3	ns
t_{PLZ}			1.5	3.3	4.7	1.5	5.2	

PARAMETER MEASUREMENT INFORMATION

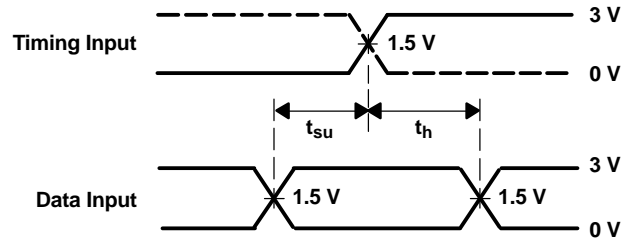


LOAD CIRCUIT

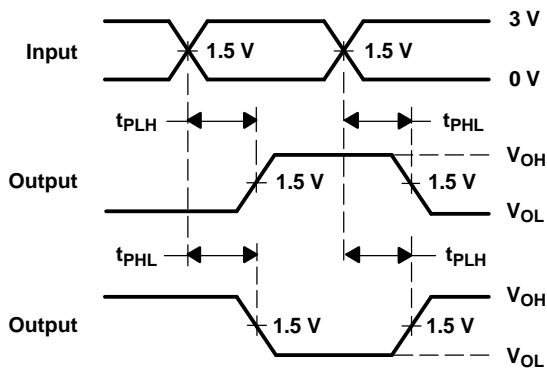
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



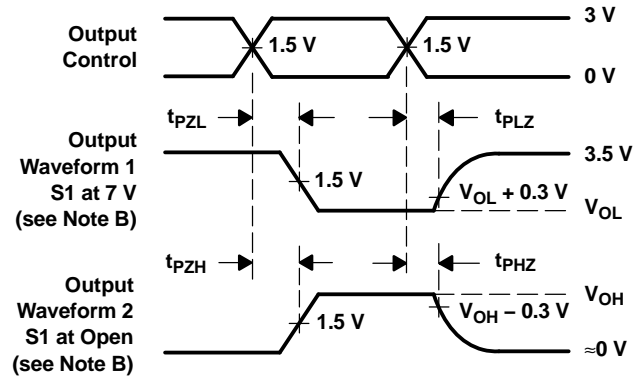
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
1O16245ADLRG4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
1O16245ADLRG4.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
5962-9317501MXA	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9317501MX A SNJ54ABT16245A WD
74ABT16245ADGGRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
74ABT16245ADGVRG4	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH245A
74ABT16245ADGVRG4.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH245A
SN74ABT16245ADGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
SN74ABT16245ADGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
SN74ABT16245ADGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH245A
SN74ABT16245ADGVR.B	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH245A
SN74ABT16245ADL	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
SN74ABT16245ADL.B	Active	Production	SSOP (DL) 48	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
SN74ABT16245ADLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
SN74ABT16245ADLR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT16245A
SNJ54ABT16245AWD	Active	Production	CFP (WD) 48	15 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9317501MX A SNJ54ABT16245A WD

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ABT16245A, SN74ABT16245A :

- Catalog : [SN74ABT16245A](#)
- Enhanced Product : [SN74ABT16245A-EP](#), [SN74ABT16245A-EP](#)
- Military : [SN54ABT16245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

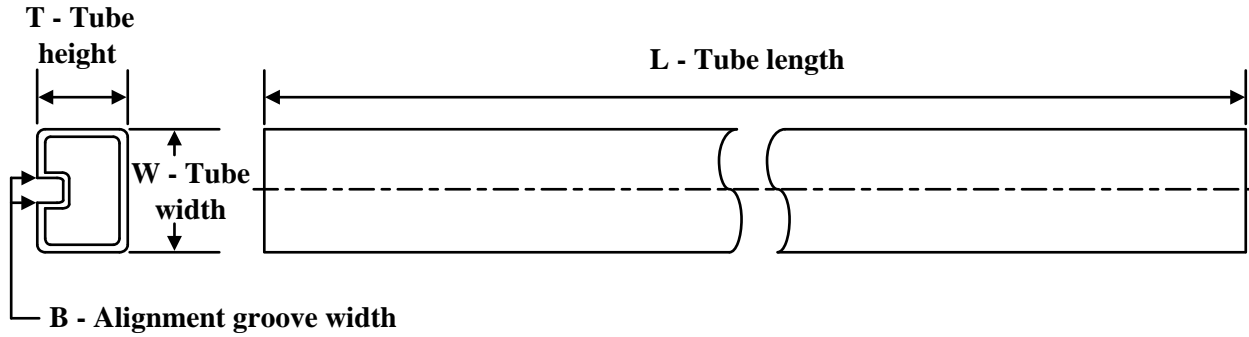

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1O16245ADLRG4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
74ABT16245ADGV RG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ABT16245ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ABT16245ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74ABT16245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1O16245ADLRG4	SSOP	DL	48	1000	367.0	367.0	55.0
74ABT16245ADGVRG4	TVSOP	DGV	48	2000	356.0	356.0	35.0
SN74ABT16245ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ABT16245ADGVR	TVSOP	DGV	48	2000	356.0	356.0	35.0
SN74ABT16245ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT16245ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74ABT16245ADL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

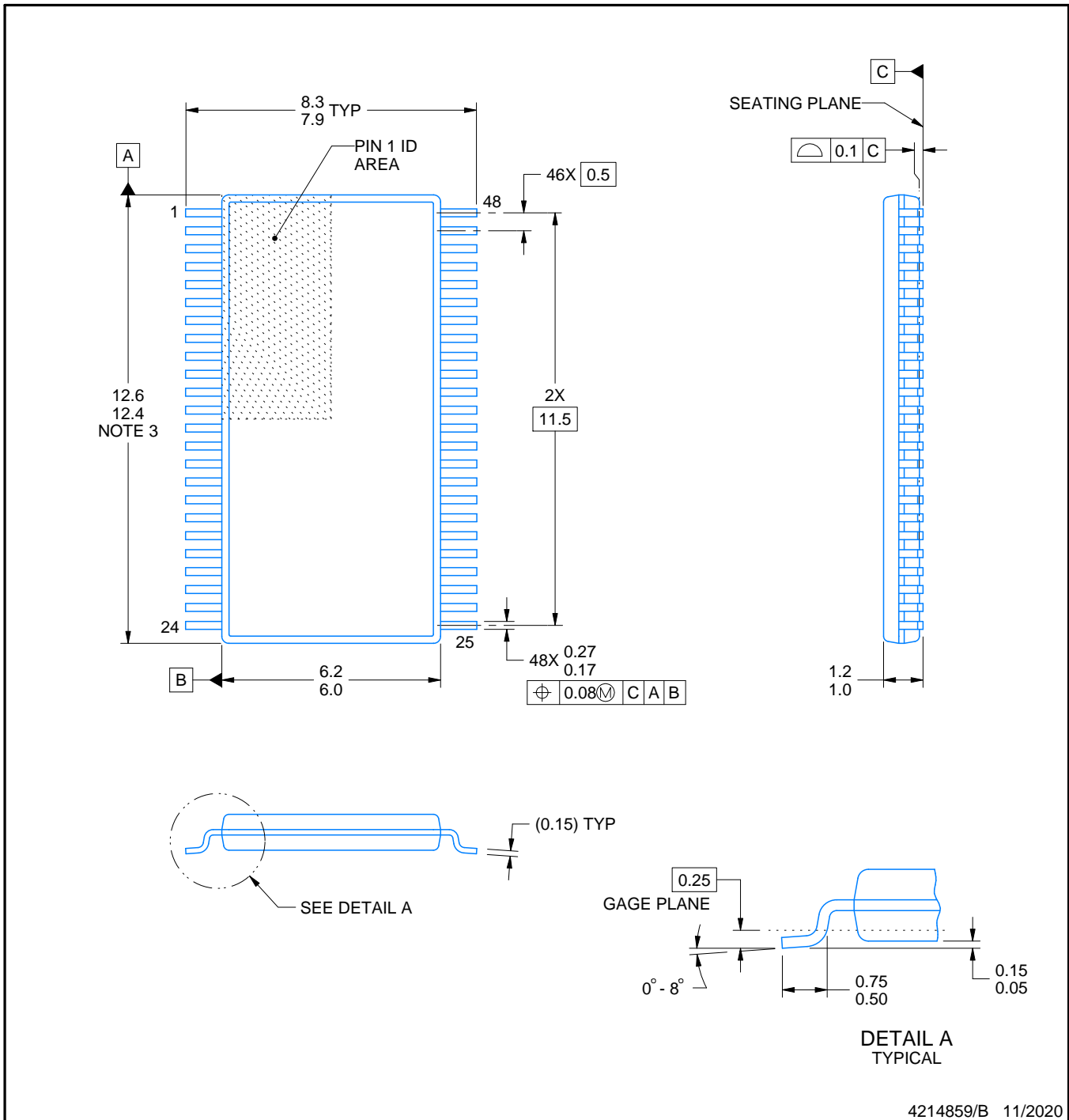
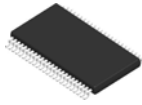
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

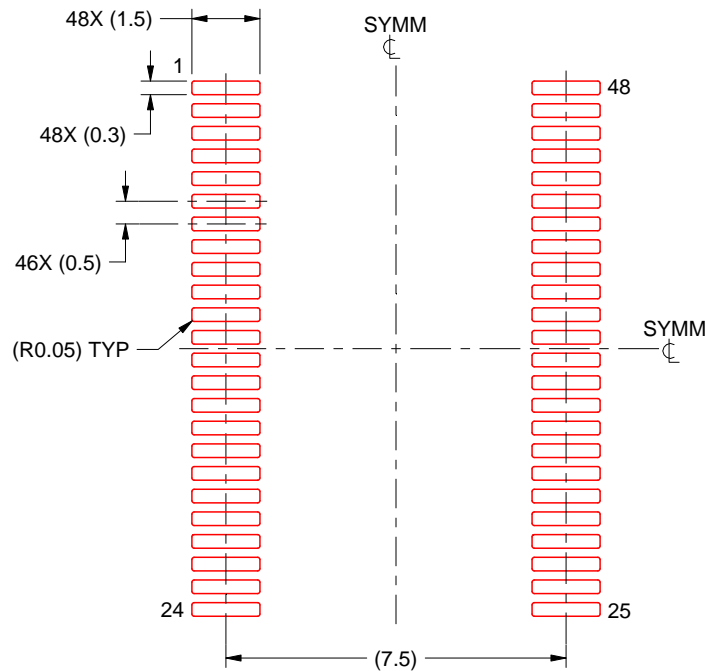
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

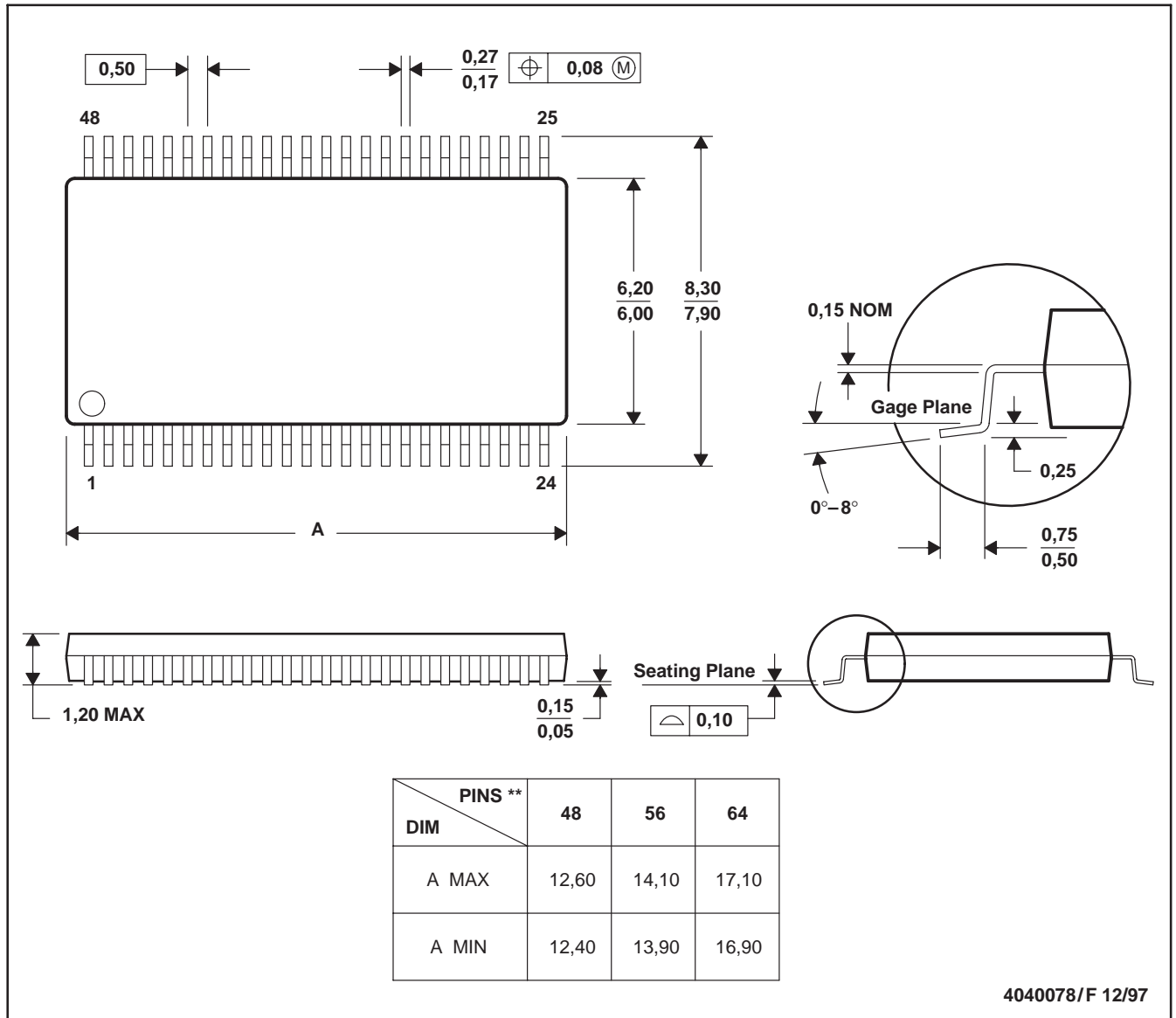
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

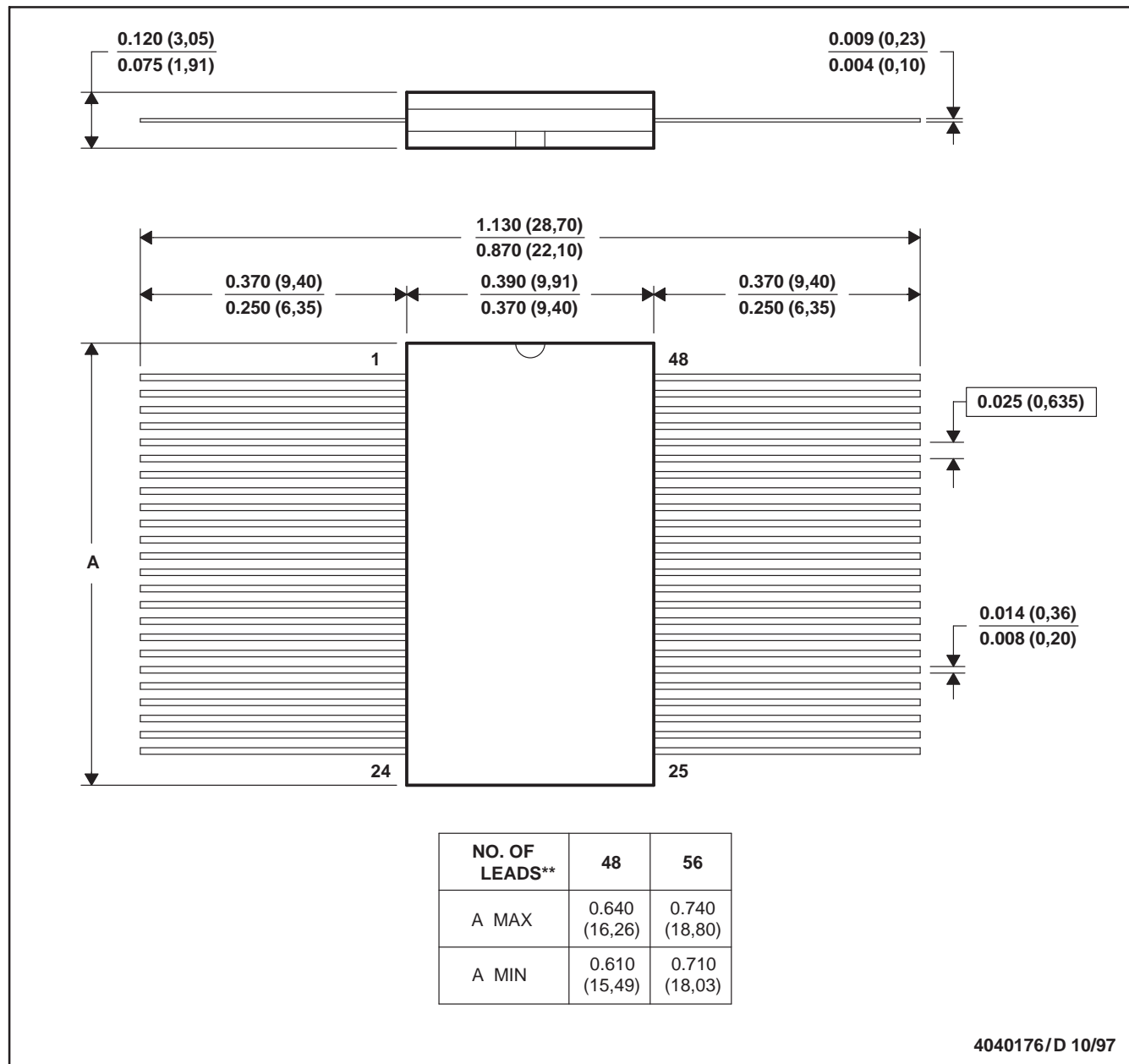


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN

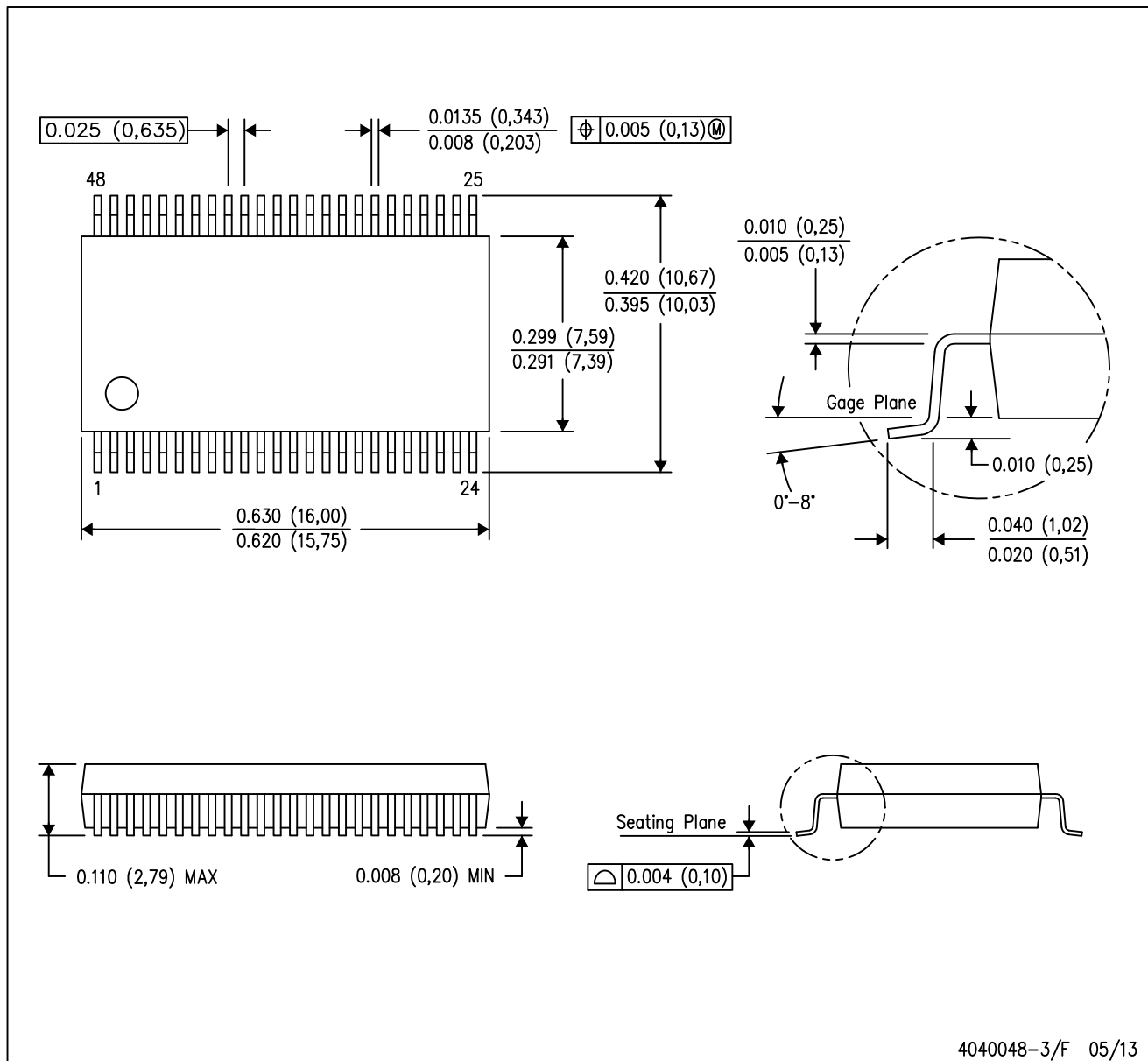


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



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- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

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