

SN74AC2G101 Dual Configurable Clock Flip-Flops With Clear

1 Features

- Wide operating range of 1.5V to 6V
- Inputs accept voltages up to 6V
- Continuous $\pm 24\text{mA}$ output drive at 5V
- Supports up to $\pm 75\text{mA}$ output drive at 5V in short bursts
- Drives 50Ω transmission lines
- Maximum t_{pd} of 11.3ns at 5V, 50pF load

2 Applications

- [Hold a signal during controller reset](#)
- [Input slow edge-rate signals](#)
- [Operate in noisy environments](#)

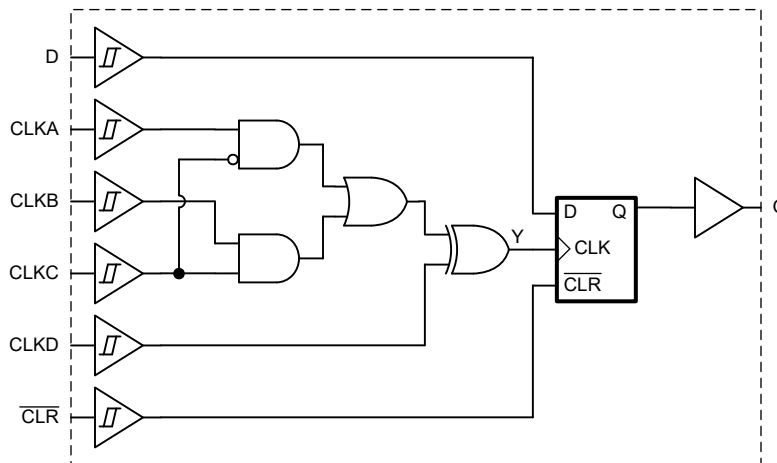
3 Description

The SN74AC2G101 contains two independent D-type flip-flops with rising edge triggered configurable logic clock, active low clear, and data inputs. The clock inputs can be configured for many 1- and 2-input logic functions, including buffer, inverter, AND, OR, NAND, NOR, XOR, XNOR. All inputs have Schmitt-trigger architecture to support slow or noisy input signals..

Package Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE ⁽³⁾ |
|-------------|------------------------|-----------------------------|--------------------------|
| SN74AC2G101 | BQB (WQFN, 16) | 3.6mm × 2.6mm | 3.6mm × 2.6mm |
| | PW (TSSOP, 16) | 6.4mm × 5mm | 5mm × 4.4mm |

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

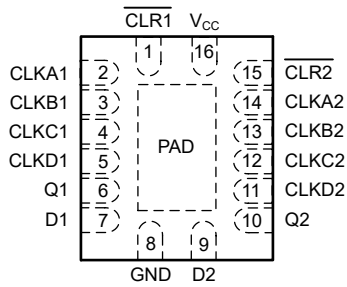


Figure 4-1. BQB Package, 16-Pin WQFN (Top View)

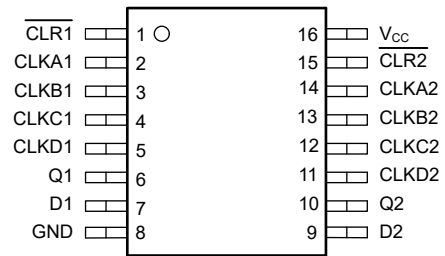


Figure 4-2. PW Package, 16-Pin TSSOP (Top View)

Table 4-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|----------------------------|-----|---------------------|---|
| NAME | NO. | | |
| CLR1 | 1 | I | Channel 1, clear, active low |
| CLKA1 | 2 | I | Channel 1, clock input A |
| CLKB1 | 3 | I | Channel 1, clock input B |
| CLKC1 | 4 | I | Channel 1, clock input C |
| CLKD1 | 5 | I | Channel 1, clock input D |
| Q1 | 6 | O | Channel 1, non-inverted output |
| D1 | 7 | I | Channel 1, data input |
| GND | 8 | G | Ground |
| D2 | 9 | I | Channel 2, data input |
| Q2 | 10 | O | Channel 2, non-inverted output |
| CLKD2 | 11 | I | Channel 2, clock input D |
| CLKC2 | 12 | I | Channel 2, clock input C |
| CLKB2 | 13 | I | Channel 2, clock input B |
| CLKA2 | 14 | I | Channel 2, clock input A |
| CLR2 | 15 | I | Channel 2, clear, active low |
| V _{CC} | 16 | P | Positive supply |
| Thermal Pad ⁽²⁾ | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) BQB package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|--|---|------|-----------------------|------|
| V _{CC} | Supply voltage range | | -0.5 | 7 | V |
| V _I | Input voltage range ⁽²⁾ | | -0.5 | V _{CC} + 0.5 | V |
| V _O | Output voltage range ⁽²⁾ | | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < -0.5V or V _I > V _{CC} + 0.5V | | ±20 | mA |
| I _{OK} | Output clamp current | V _O < -0.5V or V _O > V _{CC} + 0.5V | | ±50 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±50 | mA |
| | Continuous output current through V _{CC} or GND | | | ±200 | mA |
| T _J | Junction temperature | | | 150 | °C |
| T _{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±1000 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------------|------------------------------|-----|-----------------|------|
| V _{CC} | Supply voltage | | 1.5 | 6 | V |
| V _I | Input Voltage | | 0 | V _{CC} | V |
| V _O | Output Voltage | | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.8V | | -1 | mA |
| | | V _{CC} = 2.5V | | -2 | |
| | | V _{CC} = 3V | | -12 | |
| | | V _{CC} = 4.5V to 6V | | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.8V | | 1 | mA |
| | | V _{CC} = 2.5V | | 2 | |
| | | V _{CC} = 3V | | 12 | |
| | | V _{CC} = 4.5V to 6V | | 24 | |
| T _A | Operating free-air temperature | | -40 | 125 | °C |

5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC ⁽¹⁾ | | | | | | UNIT |
|------------|------|-------------------------------|-----------------------|------------------|-----------------|-----------------|-----------------------|------|
| | | R _{θJA} | R _{θJC(top)} | R _{θJB} | Ψ _{JT} | Ψ _{JB} | R _{θJC(bot)} | |
| PW (TSSOP) | 16 | 140 | 80 | 90 | 30 | 90 | N/A | °C/W |

| PACKAGE | PINS | THERMAL METRIC ⁽¹⁾ | | | | | | UNIT |
|------------|------|-------------------------------|-----------------------|------------------|-----------------|-----------------|-----------------------|------|
| | | R _{θJA} | R _{θJC(top)} | R _{θJB} | Ψ _{JT} | Ψ _{JB} | R _{θJC(bot)} | |
| BQB (WQFN) | 16 | 91.2 | 95.1 | 61.4 | 18.0 | 61.2 | 38.0 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------|---|-----------------|------|------|------|------|
| V _{T+} | Positive-going input threshold voltage | 1.5V | 0.71 | | 1.06 | V |
| | | 1.8V | 0.82 | | 1.22 | |
| | | 2.5V | 1.08 | | 1.51 | |
| | | 3V | 1.19 | | 1.72 | V |
| | | 4.5V | 1.61 | | 2.37 | |
| | | 6V | 1.87 | | 2.82 | V |
| V _{T-} | Negative-going input threshold voltage | 1.5V | 0.33 | | 0.68 | V |
| | | 1.8V | 0.42 | | 0.68 | |
| | | 2.5V | 0.59 | | 0.8 | |
| | | 3V | 0.68 | | 0.95 | V |
| | | 4.5V | 0.98 | | 1.36 | |
| | | 6V | 1.14 | | 1.63 | V |
| ΔV _T | Hysteresis (V _{T+} - V _{T-}) | 1.5V | 0.31 | | 0.66 | V |
| | | 1.8V | 0.37 | | 0.66 | |
| | | 2.5V | 0.45 | | 0.74 | |
| | | 3V | 0.47 | | 0.84 | V |
| | | 4.5V | 0.62 | | 1.06 | |
| | | 6V | 0.71 | | 1.23 | V |
| V _{OH} | I _{OH} = -50μA | 1.5V | 1.4 | 1.49 | | V |
| | | 1.8V | 1.7 | 1.79 | | |
| | | 2.5V | 2.4 | 2.49 | | |
| | | 3V | 2.9 | 2.99 | | |
| | | 4.5V | 4.4 | 4.49 | | |
| | | 6V | 5.4 | 5.99 | | |
| | I _{OH} = -1mA | 1.8V | 1.44 | | | |
| | I _{OH} = -2mA | 2.5V | 2 | | | |
| | I _{OH} = -12mA | 3V | 2.4 | | | |
| | I _{OH} = -24mA | 4.5V | 3.7 | | | |
| | I _{OH} = -24mA | 6V | 4.7 | | | |
| | I _{OH} = -75mA | 6V | 3.85 | | | |

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|-----------------|-----|------|------|------|
| V _{OL} | I _{OL} = 50μA | 1.5V | | 0.01 | 0.1 | V |
| | | 1.8V | | 0.01 | 0.1 | |
| | | 2.5V | | 0.01 | 0.1 | |
| | | 3V | | 0.01 | 0.1 | |
| | | 4.5V | | 0.01 | 0.1 | |
| | | 6V | | 0.01 | 0.1 | |
| | I _{OL} = 1mA | 1.8V | | | 0.36 | |
| | I _{OL} = 2mA | 2.5V | | | 0.5 | |
| | I _{OL} = 12mA | 3V | | | 0.5 | |
| | I _{OL} = 24mA | 4.5V | | | 0.5 | |
| | I _{OL} = 24mA | 6V | | | 0.5 | |
| I _{OL} = 75mA | 6V | | | 1.65 | | |
| I _I | V _I = 6V or GND | 0V to 6V | | | ±1 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 6V | | | 20 | μA |
| C _I | V _I = V _{CC} or GND | 5V | | 2 | | pF |

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | V _{CC} | -40°C to 125°C | | UNIT |
|--------------------|-----------------|--------------------------|-----------------|----------------|------|------|
| | | | | MIN | MAX | |
| f _{clock} | Clock frequency | | 1.5V | | 22 | MHz |
| | | | 3.3V ± 0.3V | | 80 | |
| | | | 5V ± 0.5V | | 140 | |
| | | | 6V | | 175 | |
| t _w | Pulse duration | CLR low | 1.5V | | 4.1 | ns |
| | | | 3.3V ± 0.3V | | 3.3 | |
| | | | 5V ± 0.5V | | | |
| | | | 6V | | 3.3 | |
| | | CLKx | 1.5V | | 4.1 | |
| | | | 3.3V ± 0.3V | | 3.3 | |
| | | | 5V ± 0.5V | | | |
| | | | 6V | | 3.3 | |
| t _{su} | Set up time | D before any CLKx | 1.5V | | 8.3 | ns |
| | | | 3.3V ± 0.3V | | 6.02 | ns |
| | | | 5V ± 0.5V | | | |
| | | | 6V | | 6.02 | ns |
| | | CLR high before any CLKx | 1.5V | | 8.3 | ns |
| | | | 3.3V ± 0.3V | | 6.02 | ns |
| | | | 5V ± 0.5V | | | |
| | | | 6V | | 6.02 | ns |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | DESCRIPTION | CONDITION | V _{CC} | -40°C to 125°C | | UNIT |
|----------------------|---------------------------------|---|-----------------|----------------|-----|------|
| | | | | MIN | MAX | |
| t _{CLKX_SU} | Set up time between CLKx inputs | CLKA input pin relative to CLKB, CLKC and CLKD pins | 1.5V | 8.3 | ns | |
| | | | 3.3V ± 0.3V | 6.02 | ns | |
| | | | 5V ± 0.5V | | | |
| | | | 6V | 6.02 | ns | |
| | | CLKB input pin relative to CLKA, CLKC and CLKD pins | 1.5V | 1 | ns | |
| | | | 3.3V ± 0.3V | 1 | ns | |
| | | | 5V ± 0.5V | | | |
| | | | 6V | 1 | ns | |
| | | CLKC input pin relative to CLKA, CLKB and CLKD pins | 1.5V | 1 | ns | |
| | | | 3.3V ± 0.3V | 1 | ns | |
| | | | 5V ± 0.5V | | | |
| | | | 6V | 1 | ns | |
| | | CLKD input pin relative to CLKA, CLKB and CLKC pins | 1.5V | 1 | ns | |
| | | | 3.3V ± 0.3V | 1 | ns | |
| | | | 5V ± 0.5V | | | |
| | | | 6V | 1 | ns | |
| t _H | Hold time | D after any CLKx | 1.5V | 8.3 | ns | |
| | | | 3.3V ± 0.3V | 6.02 | ns | |
| | | | 5V ± 0.5V | | | |
| | | | 6V | 6.02 | ns | |

5.7 Switching Characteristics

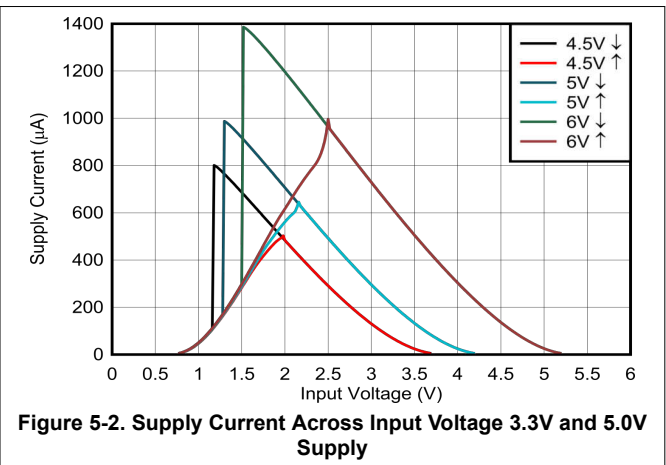
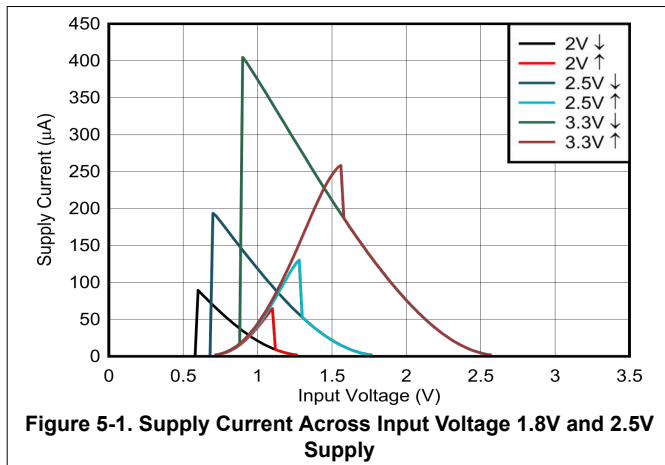
over operating free-air temperature range; $C_L = 50\text{pF}$ typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See *Parameter Measurement Information*

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | -40°C to 125°C | | | UNIT |
|-------------------------|----------------|-----------------|-----------------|----------------|------|------|------|
| | | | | MIN | TYP | MAX | |
| t_{pd} | CLKA | Q | 1.5V | | | 50.2 | ns |
| | | | $3.3V \pm 0.3V$ | | | 16.4 | ns |
| | | | $5V \pm 0.5V$ | | | 11.3 | ns |
| | | | 6V | | | 9.1 | ns |
| | CLKB | Q | 1.5V | | | 50.1 | ns |
| | | | $3.3V \pm 0.3V$ | | | 16.4 | ns |
| | | | $5V \pm 0.5V$ | | | 11.2 | ns |
| | | | 6V | | | 9.2 | ns |
| | CLKC | Q | 1.5V | | | 50.3 | ns |
| | | | $3.3V \pm 0.3V$ | | | 15 | ns |
| | | | $5V \pm 0.5V$ | | | 10.4 | ns |
| | | | 6V | | | 8.7 | ns |
| | CLKD | Q | 1.5V | | | 45.9 | ns |
| | | | $3.3V \pm 0.3V$ | | | 15.3 | ns |
| | | | $5V \pm 0.5V$ | | | 10.5 | ns |
| | | | 6V | | | 8.5 | ns |
| $\overline{\text{CLR}}$ | Q | 1.5V | | | 36.1 | ns | |
| | | $3.3V \pm 0.3V$ | | | 13.1 | ns | |
| | | $5V \pm 0.5V$ | | | 9.7 | ns | |
| | | 6V | | | 8.2 | ns | |
| $t_{sk(o)}$ | | Q | 1.5V | | | 4 | ns |
| | | | 6V | | | 1 | ns |
| $C_{PD}^{(1)}$ | CLK or CLK INH | Q_H | 5V | | | 50 | pF |

(1) Power dissipation capacitance measured with $C_L = 50\text{pF}$, $F = 1\text{MHz}$

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)



5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

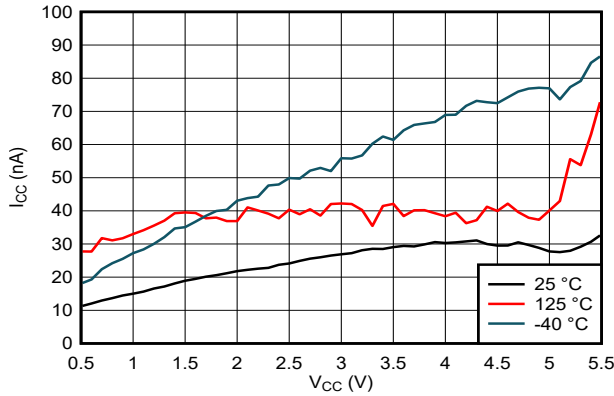


Figure 5-3. Supply Current Across Supply Voltage

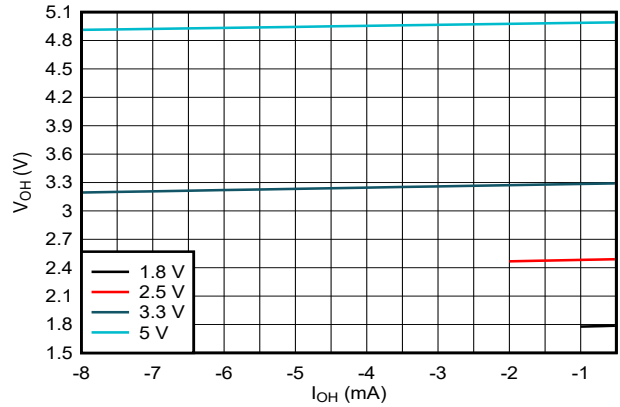


Figure 5-4. Output Voltage vs Current in HIGH State

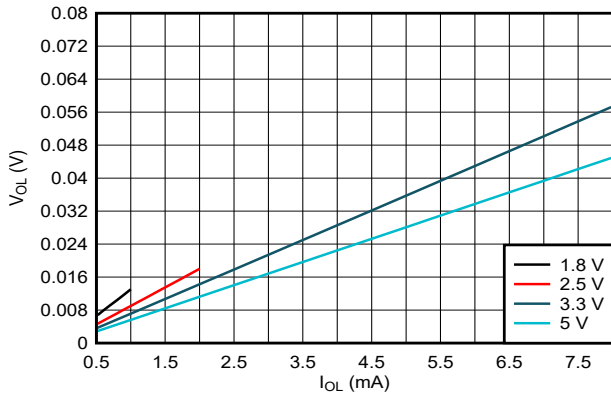


Figure 5-5. Output Voltage vs Current in LOW State

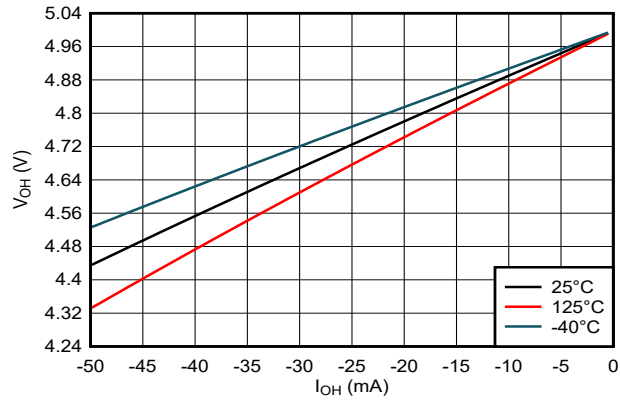


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

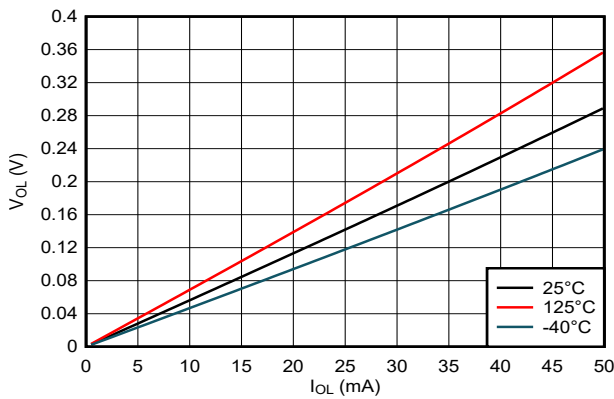


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

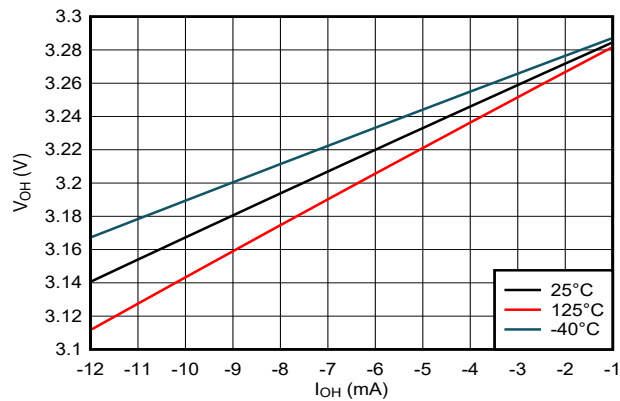


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

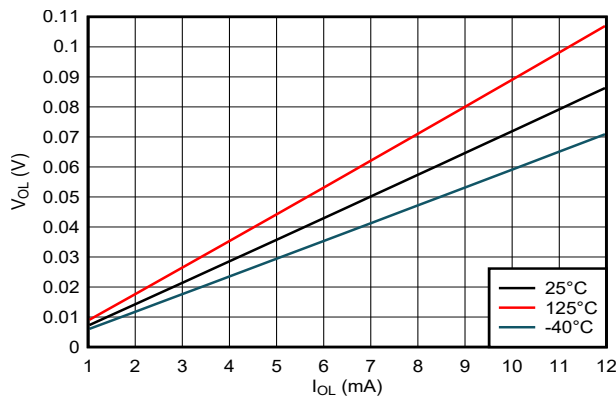


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

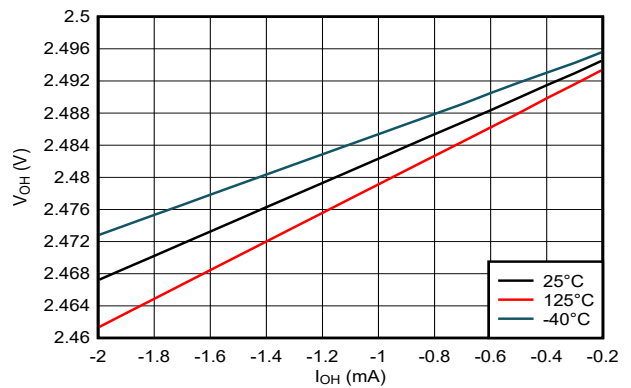


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

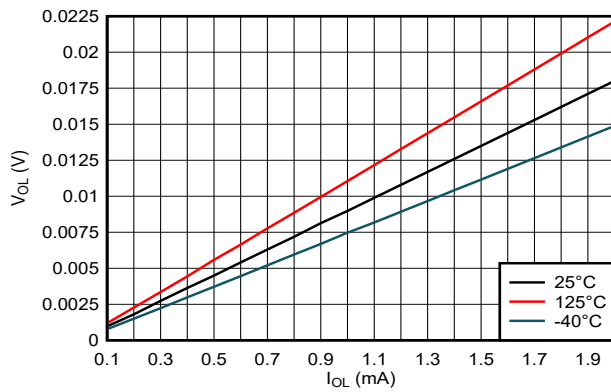


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

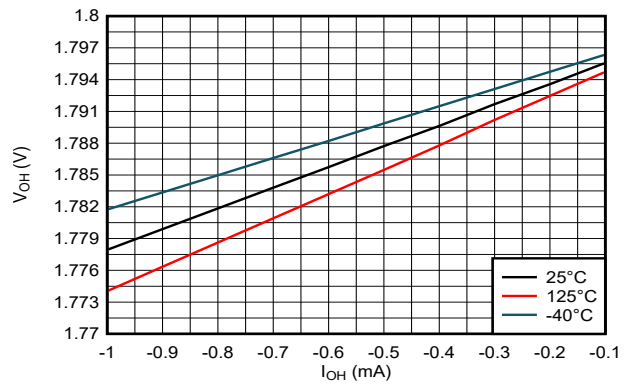


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

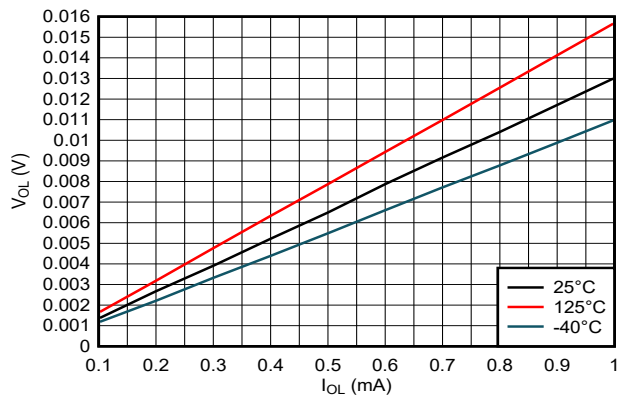
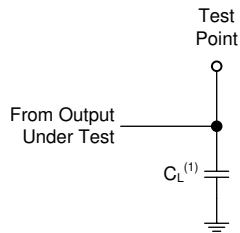


Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

6 Parameter Measurement Information

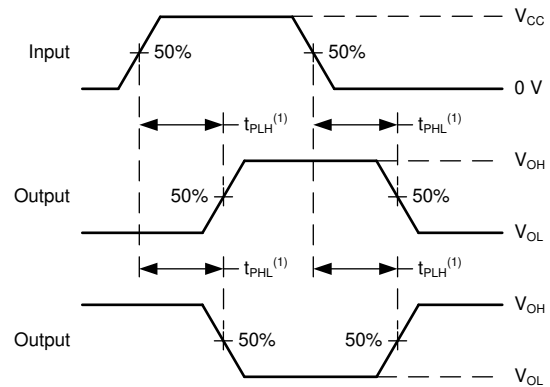
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O = 50\Omega$, $t_f < 2.5\text{ns}$.

The outputs are measured individually with one input transition per measurement.



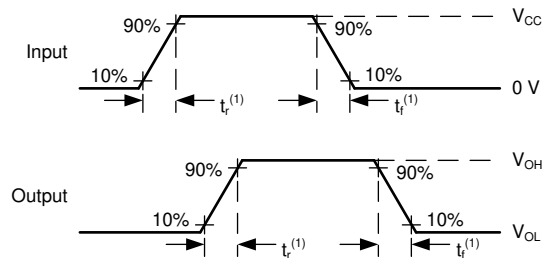
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74AC2G101 contains two independent D-type flip-flops. Each channel has separate data (D) and asynchronous active-low clear ($\overline{\text{CLR}}$) inputs, output (Q), as well as configurable clock inputs (CLKA, CLKB, CLKC, CLKD). The clock inputs utilize combinational logic to provide a variety of possible logic combinations, including common 2-input gates as well as inverted and non-inverted configurations.

7.2 Functional Block Diagram

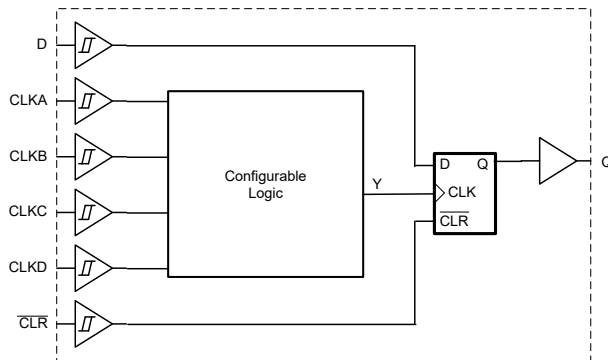


Figure 7-1. Each channel

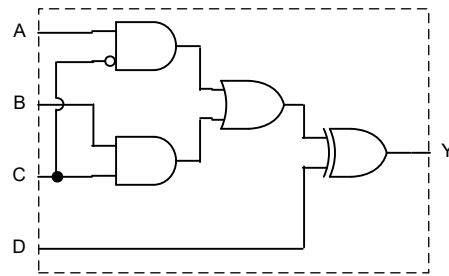


Figure 7-2. Configurable logic

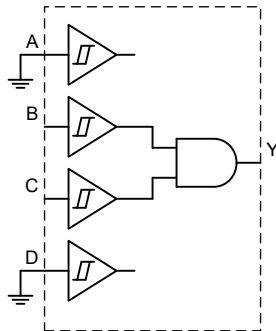


Figure 7-3. 2-input AND configuration

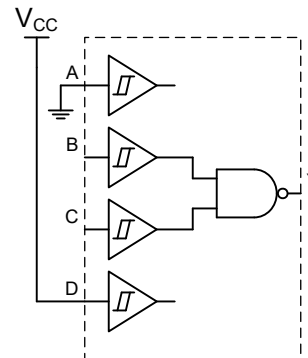


Figure 7-4. 2-input NAND configuration

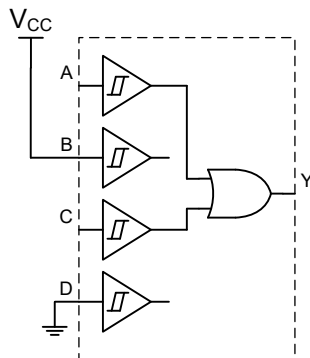


Figure 7-5. 2-input OR configuration

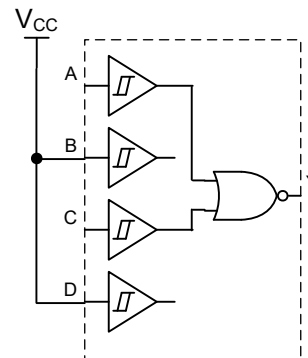


Figure 7-6. 2-input NOR configuration

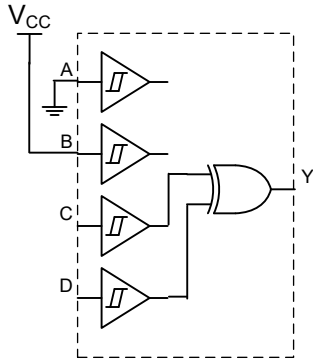


Figure 7-7. 2-input XOR configuration

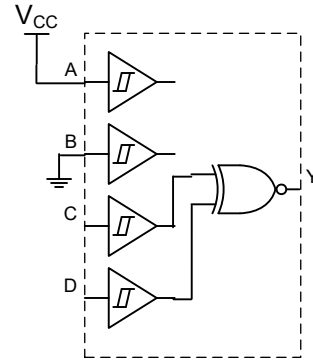


Figure 7-8. 2-input XNOR configuration

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

7.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

7.3.3 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.4 Clamp Diode Structure

As shown in [Figure 7-9](#), the inputs and outputs to this device have both positive and negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

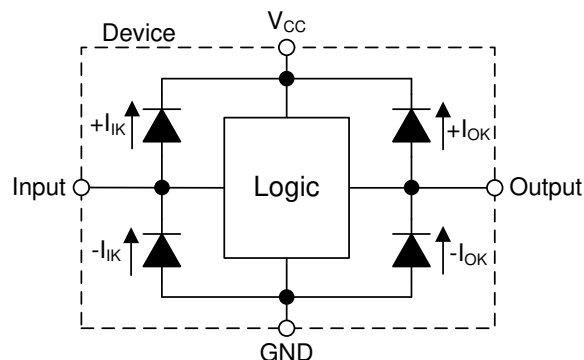


Figure 7-9. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Flip-Flop Function Table

| INPUTS ⁽¹⁾ | | | OUTPUT ⁽²⁾ |
|-------------------------|--------------------|---|-----------------------|
| $\overline{\text{CLR}}$ | CLK ⁽³⁾ | D | Q |
| L | X | X | L |
| H | L, H, ↓ | X | Q ₀ |
| H | ↑ | L | L |
| H | ↑ | H | H |

- (1) L = Input low, H = Input high, ↑ = Input transitioning from low to high, ↓ = Input transitioning from high to low, X = Don't care
 (2) L = Output low, H = Output high, Q₀ = Previous state
 (3) Internal flip-flop input, denoted as Y on functional block diagram

Table 7-2. Combinational Logic Function Table

| INPUTS | | | | OUTPUT |
|--------|---|---|---|--------|
| A | B | C | D | Y |
| L | L | L | L | L |
| L | L | L | H | H |
| L | L | H | L | L |
| L | L | H | H | H |
| L | H | L | L | L |
| L | H | L | H | H |
| L | H | H | L | H |
| L | H | H | H | L |
| H | L | L | L | H |
| H | L | L | H | L |
| H | L | H | L | L |
| H | L | H | H | H |
| H | H | L | L | H |
| H | H | L | H | L |
| H | H | H | L | H |
| H | H | H | H | L |

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74AC2G101 is used to read in two different active-high fault signals (FAULT1, FAULT2) and latch an output signal (LATCHED FAULT) high when the boolean logic FAULT1 OR FAULT2 has a rising edge.

At power-up, the initial state of the flip-flop is unknown. To give it a defined state of zero, the device can be cleared by applying a low signal to the clear (CLR) input.

8.2 Typical Application

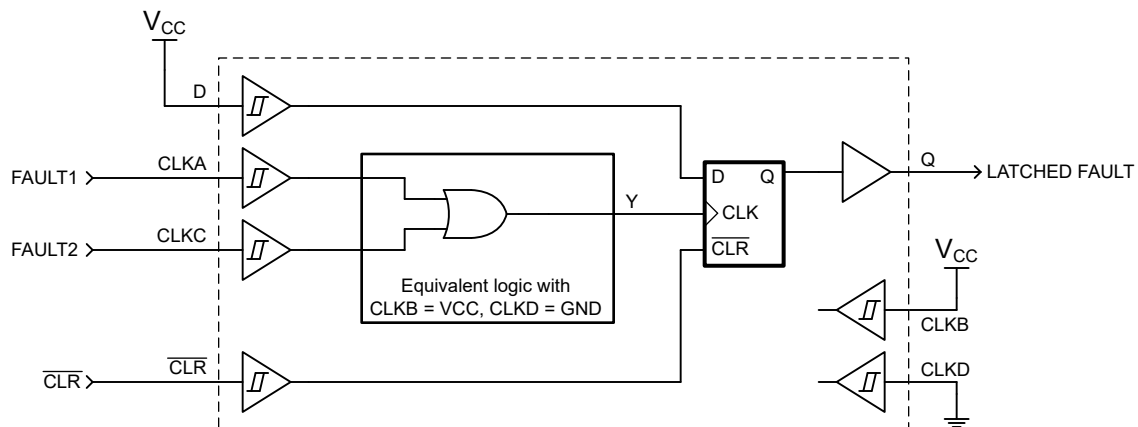


Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AC2G101 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AC2G101 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AC2G101 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AC2G101 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{t-(\min)}$ to be considered a logic LOW, and $V_{t+(\max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AC2G101 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74AC2G101 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(\min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq 50\text{pF}$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AC2G101 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in $M\Omega$; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

8.2.3 Reference

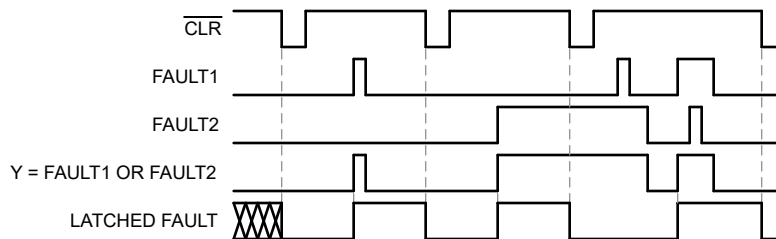


Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

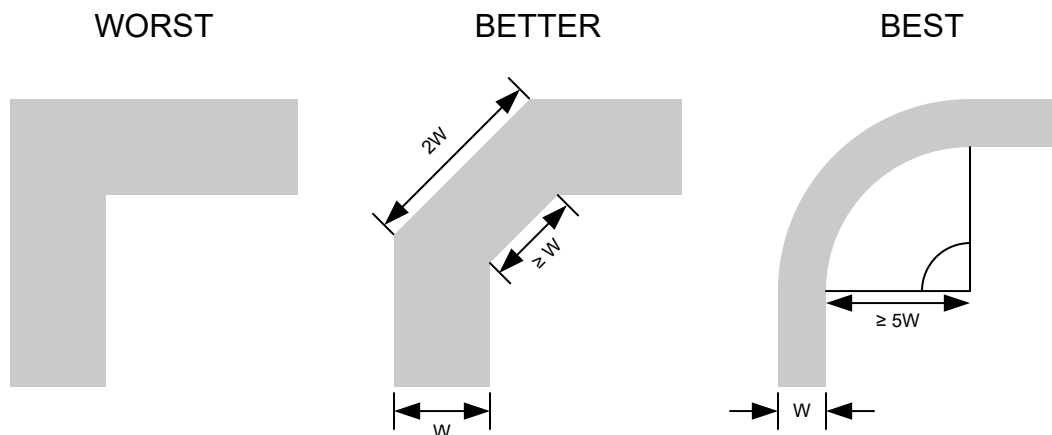


Figure 8-3. Example Trace Corners for Improved Signal Integrity

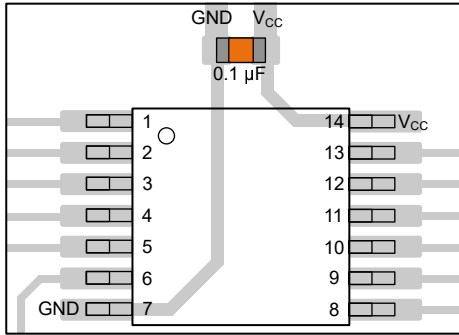


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

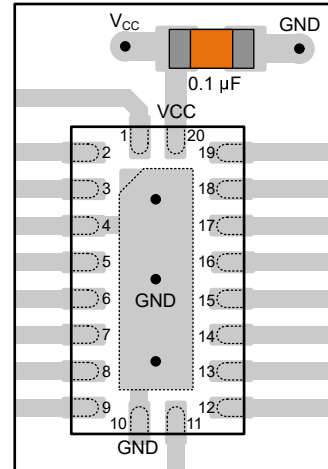


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

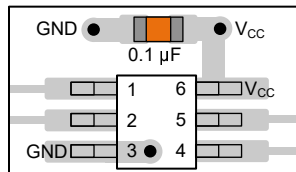


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

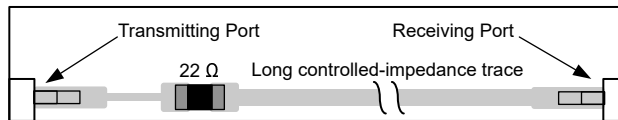


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (September 2024) to Revision A (June 2025) | Page |
|---|------|
| • Updated part number typo throughout. | 1 |
| • Changed data sheet status from Advanced Information to Production Data..... | 1 |
| • Added PW package..... | 1 |
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| PSN74AC2G101BQBR | Active | Preproduction | WQFN (BQB) 16 | 3000 LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| PSN74AC2G101BQBR.A | Active | Preproduction | WQFN (BQB) 16 | 3000 LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| SN74AC2G101BQBR | Active | Production | WQFN (BQB) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC101 |
| SN74AC2G101PWR | Active | Production | TSSOP (PW) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AC101 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74AC2G101 :

- Automotive : [SN74AC2G101-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AC2G101BQBR | WQFN | BQB | 16 | 3000 | 180.0 | 12.4 | 2.8 | 3.8 | 1.2 | 4.0 | 12.0 | Q1 |
| SN74AC2G101PWR | TSSOP | PW | 16 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AC2G101BQBR | WQFN | BQB | 16 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AC2G101PWR | TSSOP | PW | 16 | 3000 | 353.0 | 353.0 | 32.0 |



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

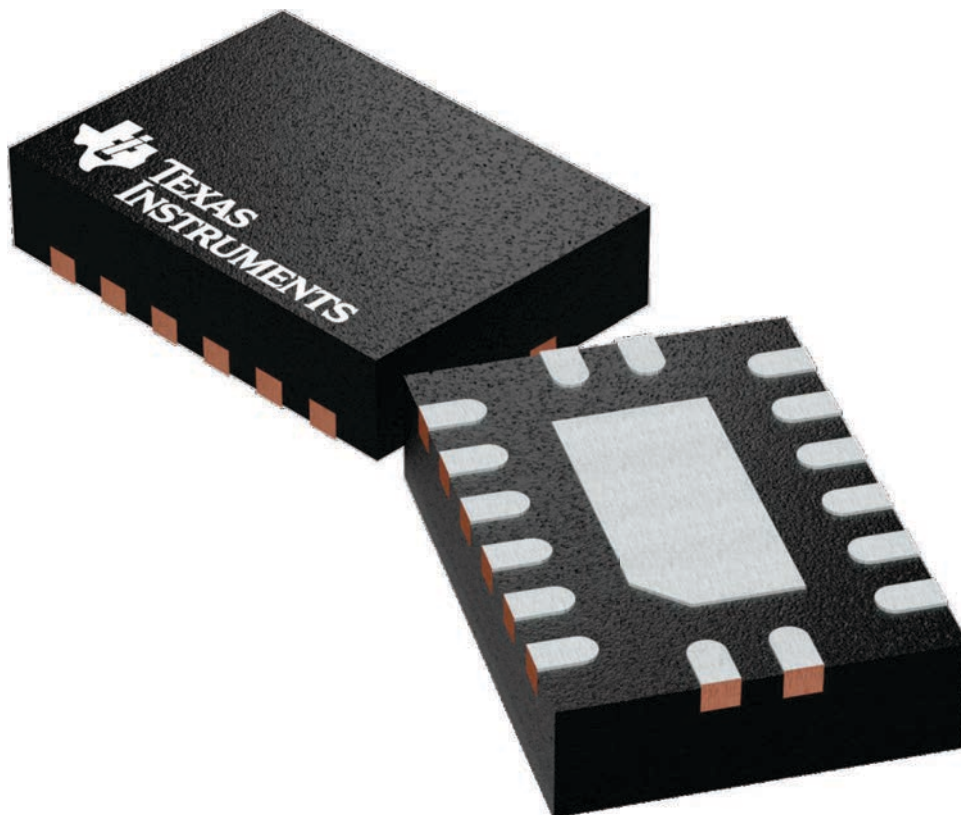
BQB 16

WQFN - 0.8 mm max height

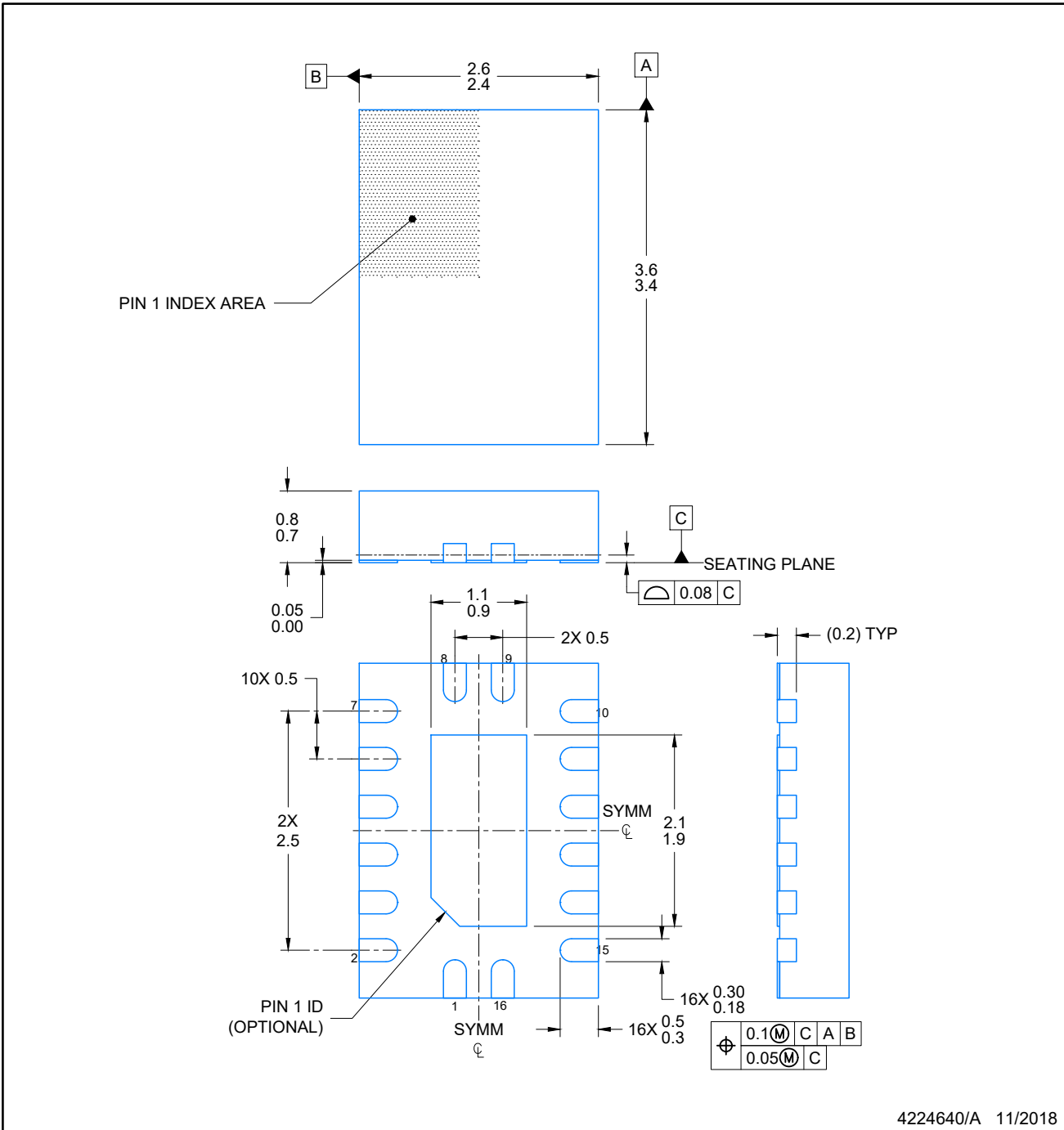
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226161/A



4224640/A 11/2018

NOTES:

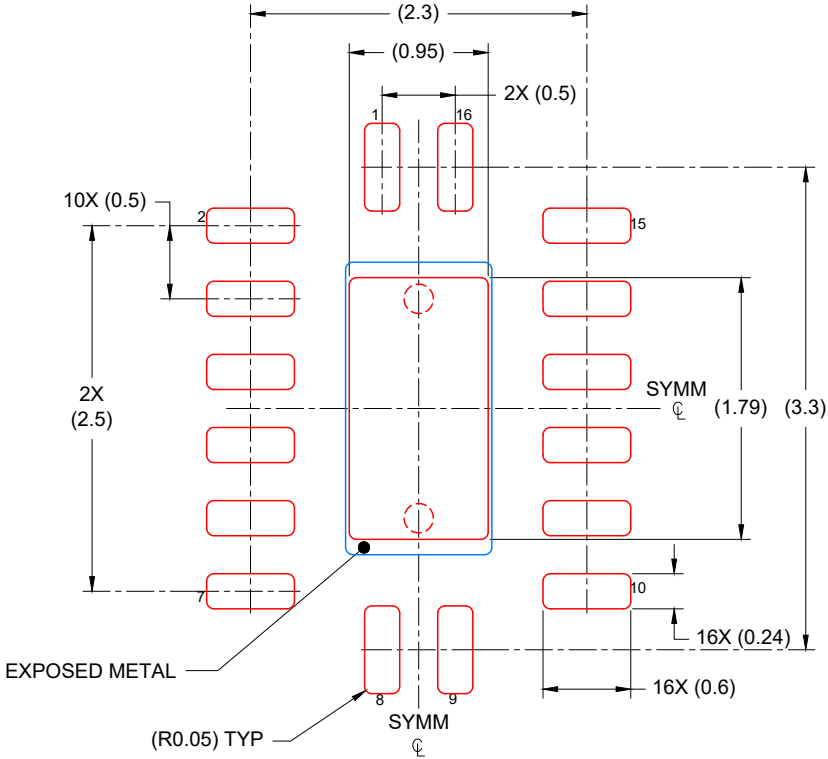
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

BQB0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 85% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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