F28E12x Real-Time Microcontrollers

1 Features

- Real-time processing
  - 160MHz C28x 32-bit DSP CPU
  - Equivalent to 320MHz Arm® Cortex®-M7 based device on real-time signal chain performance (see the *Real-time Benchmarks Showcasing C2000™ Control MCU's Optimized Signal Chain* Application Note)
  - Floating Point Unit (FPU) for more precise mathematical calculations
- On-chip memory
  - Up to 128KB (64KW) of single bank flash (ECC-protected)
  - 16KB (8KW) of RAM (Parity-protected)
  - Security
    - JTAGLOCK
    - Zero-pin boot
    - Dual-zone security
- Clock and system control
  - Internal 32MHz oscillator with up to ±1.2% accuracy (SYSOSC)
  - Crystal oscillator or external clock input
  - Windowed watchdog timer module
  - Missing clock detection circuitry
  - Dual-clock Comparator (DCC)
- 3.3V I/O design
  - Internal VREG generation allows for single-supply design
  - Brownout reset (BOR) circuit
- System peripherals
  - 27 individually programmable multiplexed General-Purpose Input/Output (GPIO) pins (8 shared with Analog)
  - 9 digital inputs on analog pins
  - One 2-channel Direct Memory Access (DMA) controller
  - Enhanced Peripheral Interrupt Expansion (ePIE)
  - Multiple low-power mode (LPM) support
  - Unique Identification (UID) number
- Communications peripherals
  - One Inter-integrated Circuit (I2C) interface
  - One high-speed (20Mbps) Universal Asynchronous Receiver/Transmitter (UART)
  - One Serial Peripheral Interface (SPI) port
  - Two UART-compatible Serial Communication Interfaces (SCIs)
- Analog system
  - One 9.4MSPS, 12-bit Analog-to-Digital Converter (ADC)
    - Up to 17 external channels (8 shared with GPIO)
    - Three integrated Post-Processing Blocks (PPB) per ADC
  - Three windowed comparators (CMPSS_LITE) with 10-bit effective reference DACs
    - Digital glitch filters
    - One DAC output (CMP3_LITE_DACL) available on the pin
  - One Programmable Gain Amplifier (PGA)
    - Unity gain support
    - Inverting and non-inverting gain mode support
    - Inputs with 3-to-1 multiplexer
    - Programmable output filtering
- Enhanced control peripherals
  - 2 MCPWM modules, 8 total PWM channels (one 6-channel MCPWM module and one 2-channel module)
  - One Enhanced Capture (eCAP) module
  - One Enhanced Quadrature Encoder Pulse (eQEP) module with support for CW/CCW operation modes
- CMAC Keys (128-bit) for SW AES
- Package options:
  - 48-pin Low-Profile Quad Flat Pack (LQFP) [PT suffix]
  - 32-pin Low-Profile Quad Flat Pack (LQFP) [VFC suffix]
  - 32-pin Very Thin Quad Flatpack No-Lead (VQFN) [RHB suffix]
- Temperature options:
  - Junction (T_J): –40°C to 125°C

2 Applications

- Appliances
  - Air conditioner outdoor unit
  - Washer & dryer
  - Robotic lawn mower
  - Merchant telecom rectifiers
  - Appliances pumps & fans
  - Appliances: compressor
  - Cordless handheld garden tool
  - Cordless power tool
  - Lawn mower
  - Mains powered tools
  - Cooker hood
  - Dishwasher

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  - Refrigerator & freezer
  - Air conditioner indoor unit
  - Vacuum robot
  - Air purifier & humidifier
  - Cordless vacuum cleaner
  - Mixer, blender & food processor
  - Residential & living fan
- Building automation
  - Automated door & gate
  - HVAC motor control
- Factory automation & control
  - Actuator
  - Automated sorting equipment
- Mobile robot motor controller
  - Textile machine
- Motor drives
  - AC drive control module
  - AC drive power stage module
  - Linear motor power stage
  - Drone propeller ESC
  - Servo drive control module
  - Servo drive power stage module
  - AC-input BLDC motor drive
  - DC-input BLDC motor drive
  - Closed loop stepper
  - Open loop stepper
- Industrial power
  - Industrial AC-DC
- Portable power station
  - UPS
- Single-phase line interactive UPS
  - Single-phase online UPS
- Grid infrastructure
  - Micro inverter
  - Rapid shutdown
  - Solar charge controller
  - Solar power optimizer

3 Description

The F28E12x is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in motor drive applications.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 160MHz of signal-processing performance for fixed-point code running from either on-chip flash or SRAM.

The F28E12x supports up to 128KB (64KW) of flash memory. Up to 16KB (8KW) of on-chip SRAM is also available to supplement the flash memory.

High-performance analog blocks are integrated into the F28E12x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Eight PWM channels enable control of various power stages from a 3-phase inverter to power-factor correction and other advanced multilevel power topologies.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, and UART) and offers multiple pin-muxing options for optimal signal placement.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out *The Essential Guide for Developing With C2000™ Real-Time Microcontrollers* and visit the C2000 real-time microcontrollers page.

The *Getting Started With C2000™ Real-Time Control Microcontrollers (MCUs) Getting Started Guide* covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the LAUNCHXL-F28E12X development kit and download C2000Ware.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
F28E120SC	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
	VFC (LQFP, 32)	9mm × 9mm	7mm × 7mm
	RHB (VQFN, 32)	5mm × 5mm	5mm × 5mm
F28E120SB	PT (LQFP, 48)	9mm × 9mm	7mm × 7mm
	VFC (LQFP, 32)	9mm × 9mm	7mm × 7mm
	RHB (VQFN, 32)	5mm × 5mm	5mm × 5mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* section.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER(1)	PACKAGE OPTIONS	FLASH SIZE	INTERNAL VOLTAGE REGULATOR	EXTERNAL VOLTAGE REGULATOR
F28E120SC	48 PT 32 VFC 32 RHB	128KB	Yes	No
F28E120SB	48 PT 32 VFC 32 RHB	64KB	Yes	No

(1) For more information on these devices, see the *Device Comparison* table.

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3.1 Functional Block Diagram

The Functional Block Diagram shows the CPU system and associated peripherals.

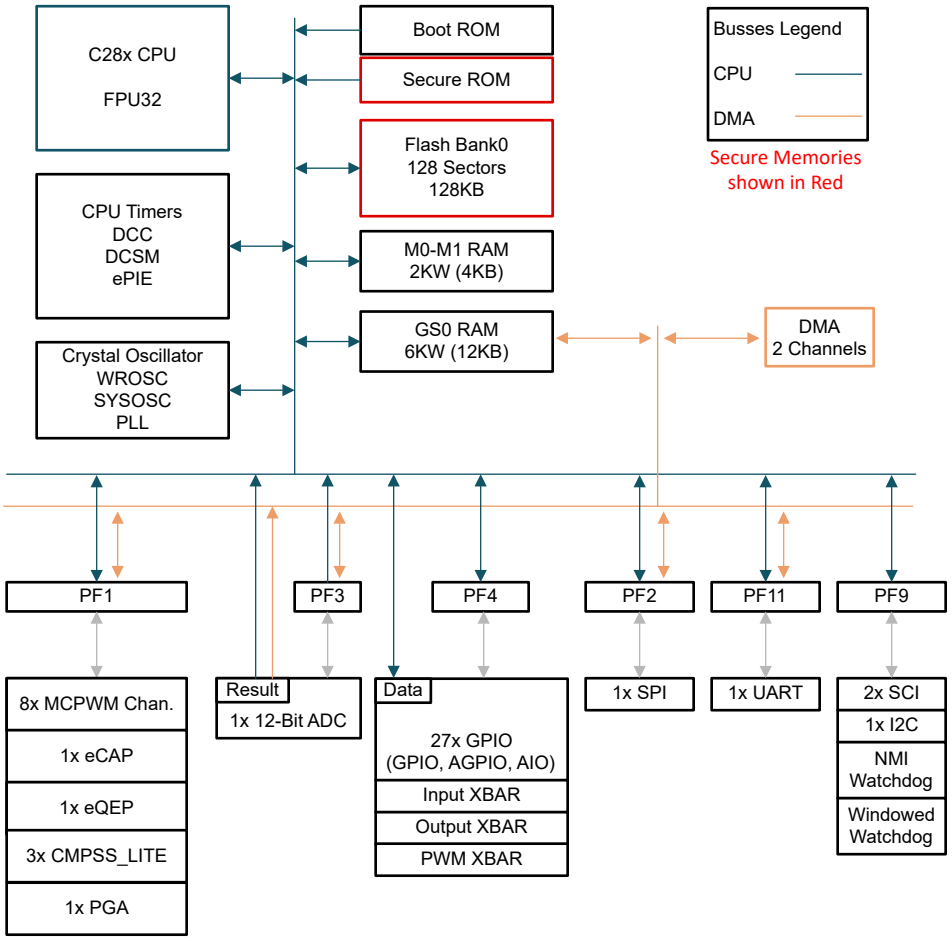

Figure 3-1. Functional Block Diagram

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4 Device Comparison

Table 4-1 lists the features of the F28E12x devices.

Table 4-1. Device Comparison

FEATURE[1]		F28E120SC	F28E120SB
PROCESSOR AND ACCELERATORS			
C28x	Frequency (MHz)	160	
	FPU32 - Type 0	Yes	
2-Channel DMA - Type 0		**1**	
MEMORY			
Flash		128KB (64KW)	64KB (32KW)
RAM		16KB (8KW)	
Security: JTAGLOCK, Zero-pin boot, Dual-zone security		Yes	
SYSTEM			
32-bit CPU timers		3	
Watchdog-timer		1	
Dual Clock Compare (DCC)		1	
External Interrupts		5	
Nonmaskable Interrupt Watchdog (NMIWD) timers		1	
Crystal oscillator/External clock input		1	
Internal oscillator accuracy (WROSC and SYSOSC)		See the *Internal Oscillators* section.	
Internal 3.3-V to 1.2-V Voltage Regulator (VREG)		Yes	
GPIO		See the *GPIO and ADC Allocation* section.	
ANALOG PERIPHERALS			
ADC 12-bit	Number of ADCs	1	
	Conversion-time (ns)[2]	68.75 ns / 9.4 MSPS	
	ADC channels	See the *GPIO and ADC Allocation* section.	
Temperature sensor		1	
Comparator Subsystem	CMPSS_LITE (each includes two comparators and two static 10-bit effective DACs)	3	
PGA		1	
CONTROL PERIPHERALS[3]			
eCAP modules – Type 2		1	
MCPWM – Type 0	Total Channels	8	
eQEP modules – Type 2		1	
COMMUNICATION PERIPHERALS[3]			
I2C – Type 2		1	
SCI – Type 0 (UART-Compatible)		2	
SPI – Type 2		1	
UART – Type 0		1	

Table 4-1. Device Comparison (continued)

FEATURE(1)	F28E120SC	F28E120SB
PACKAGE, TEMPERATURE, AND QUALIFICATION OPTIONS		
Junction temperature (T_J)	–40°C to 125°C	
Free-Air temperature (T_A)	–40°C to 105°C	

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module.
(2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
(3) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has fewer device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number. See the *Pin Configuration and Functions* section to identify which peripheral instances are accessible on pins in the smaller package.

4.1 Related Products

TMS320F2802x Real-Time Microcontrollers
The F2802x series increases the pin count and memory size options.

TMS320F2803x Real-Time Microcontrollers
The F2803x series increases the pin count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

TMS320F280013x Real-Time Microcontrollers
The F280013x series is a reduced version of the F28003x series with the latest generational enhancements.

TMS320F280015x Real-Time Microcontrollers
The F280015x series builds upon the F28002x series offering higher frequency, more memory, and more peripheral options. CAN-FD and security features are introduced from the F2838x series.

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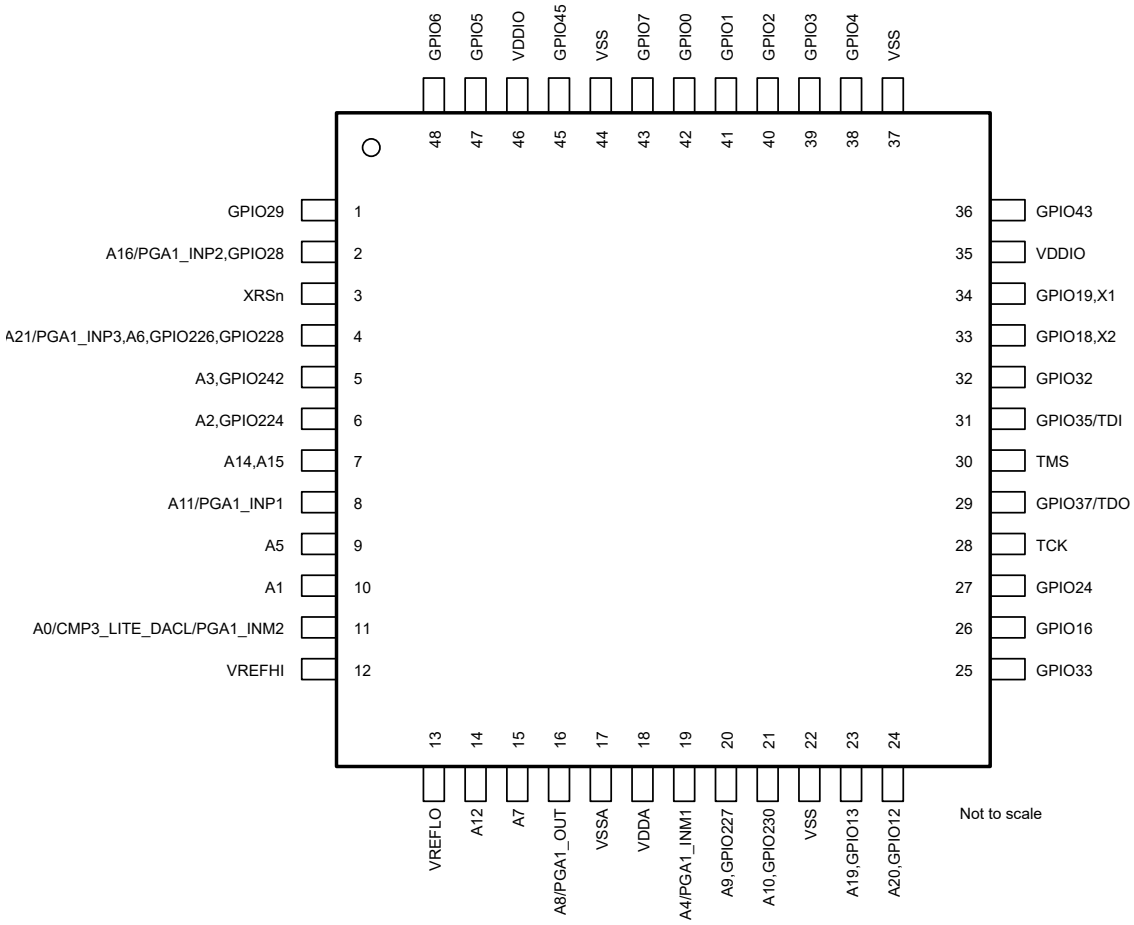
5 Pin Configuration and Functions

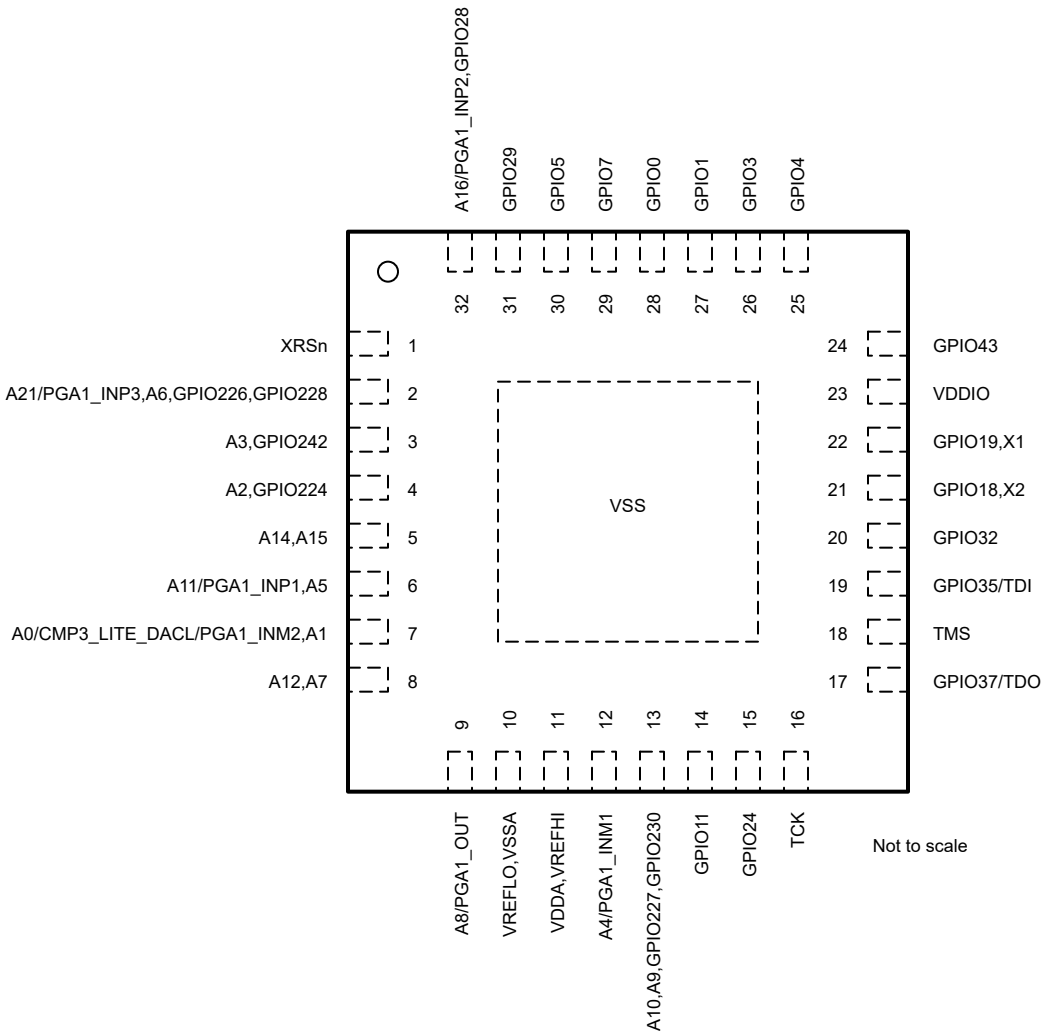
5.1 Pin Diagrams

Figure 5-1 shows the pin assignments on the 48-pin PT LQFP. Figure 5-2 shows the pin assignments on the 32-pin RHB VQFN. Figure 5-3 shows the pin assignments on the 32-pin VFC LQFP.



A. Only the GPIO function is shown on GPIO terminals. See the *Pin Attributes* section for the complete, muxed signal name.

Figure 5-1. 48-Pin PT Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO terminals. See the *Pin Attributes* section for the complete, muxed signal name.

Figure 5-2. 32-Pin RHB Very Thin Quad Flatpack No-Lead (Top View)

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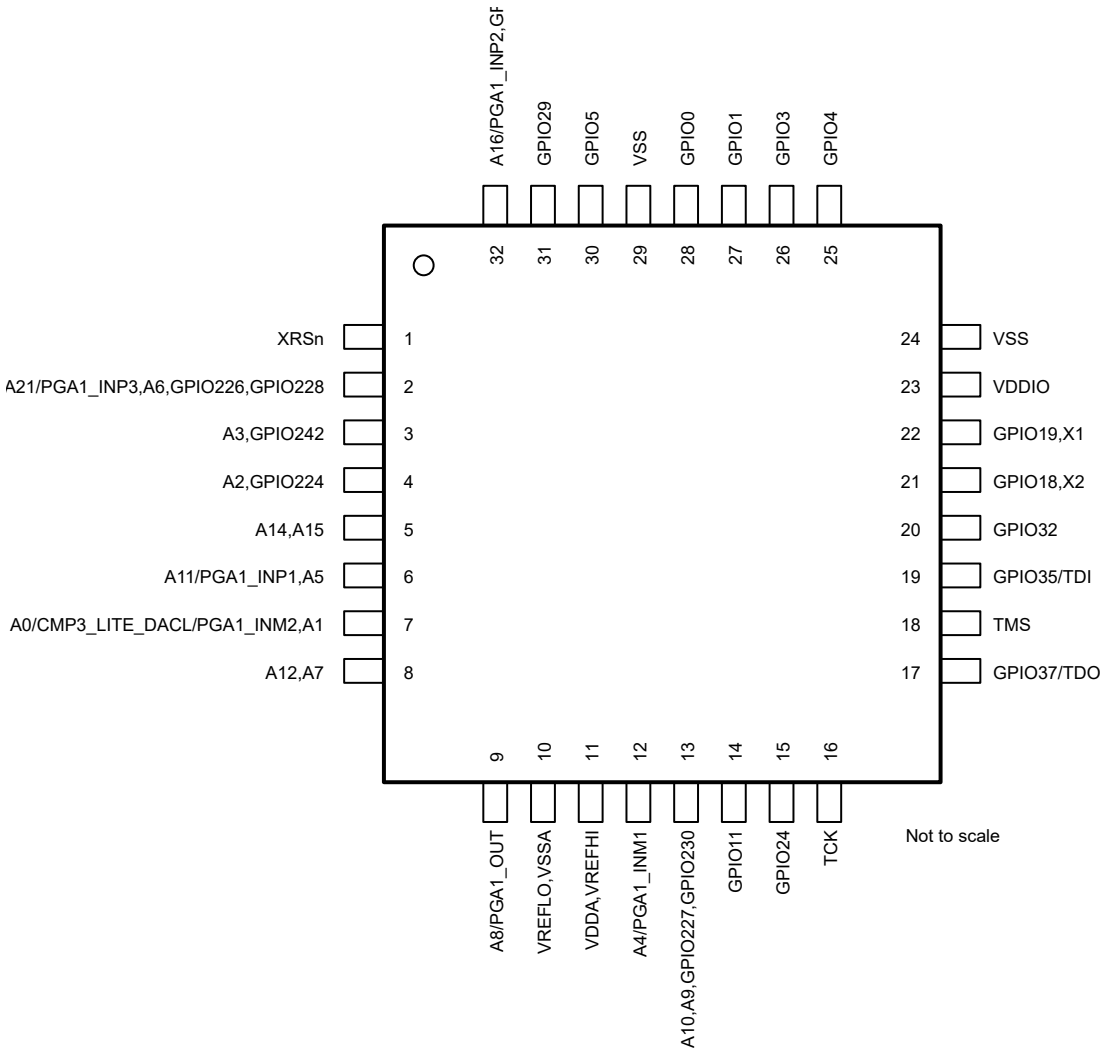

A. Only the GPIO function is shown on GPIO terminals. See the *Pin Attributes* section for the complete, muxed signal name.

Figure 5-3. 32-Pin VFC Low-Profile Quad Flatpack (Top View)

5.2 Pin Attributes

Table 5-1. Pin Attributes

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
ANALOG						
A0					I	ADC-A Input 0
CMP3_HP2					I	CMPSS-3 High Comparator Positive Input 2
CMP3_LP2		11	7	7	I	CMPSS-3 Low Comparator Positive Input 2
PGA1_INM2					I	PGA-1 Minus 2
AIO231	0, 4, 8, 12				I	Analog Pin Used For Digital Input 231
A1					I	ADC-A Input 1
CMP1_HP4		10	7	7	I	CMPSS-1 High Comparator Positive Input 4
CMP1_LP4					I	CMPSS-1 Low Comparator Positive Input 4
AIO232	0, 4, 8, 12				I	Analog Pin Used For Digital Input 232
A2					I	ADC-A Input 2
CMP1_HP0					I	CMPSS-1 High Comparator Positive Input 0
CMP1_LP0		6	4	4	I	CMPSS-1 Low Comparator Positive Input 0
GPIO224					I/O	General-Purpose Input Output 224 This pin also has digital mux functions which are described in the GPIO section of this table.
A3					I	ADC-A Input 3
CMP3_HN0					I	CMPSS-3 High Comparator Negative Input 0
CMP3_HP3					I	CMPSS-3 High Comparator Positive Input 3
CMP3_LN0		5	3	3	I	CMPSS-3 Low Comparator Negative Input 0
CMP3_LP3					I	CMPSS-3 Low Comparator Positive Input 3
GPIO242					I/O	General-Purpose Input Output 242 This pin also has digital mux functions which are described in the GPIO section of this table.
A4					I	ADC-A Input 4
CMP2_HP0					I	CMPSS-2 High Comparator Positive Input 0
CMP2_LP0					I	CMPSS-2 Low Comparator Positive Input 0
CMP4_HN0					I	CMPSS-4 High Comparator Negative Input 0
CMP4_HP3		19	12	12	I	CMPSS-4 High Comparator Positive Input 3
CMP4_LN0					I	CMPSS-4 Low Comparator Negative Input 0
CMP4_LP3					I	CMPSS-4 Low Comparator Positive Input 3
PGA1_INM1					I	PGA-1 Minus 1
AIO225	0, 4, 8, 12				I	Analog Pin Used For Digital Input 225
A5					I	ADC-A Input 5
CMP3_HN1					I	CMPSS-3 High Comparator Negative Input 1
CMP3_HP1		9	6	6	I	CMPSS-3 High Comparator Positive Input 1
CMP3_LN1					I	CMPSS-3 Low Comparator Negative Input 1
CMP3_LP1					I	CMPSS-3 Low Comparator Positive Input 1
AIO244	0, 4, 8, 12				I	Analog Pin Used For Digital Input 244
A6					I	ADC-A Input 6
CMP1_HP2					I	CMPSS-1 High Comparator Positive Input 2
CMP1_LP2		4	2	2	I	CMPSS-1 Low Comparator Positive Input 2
GPIO228					I/O	General-Purpose Input Output 228 This pin also has digital mux functions which are described in the GPIO section of this table.

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
A7					I	ADC-A Input 7
CMP4_HN1					I	CMPSS-4 High Comparator Negative Input 1
CMP4_HP1		15	8	8	I	CMPSS-4 High Comparator Positive Input 1
CMP4_LN1					I	CMPSS-4 Low Comparator Negative Input 1
CMP4_LP1					I	CMPSS-4 Low Comparator Positive Input 1
AIO245	0, 4, 8, 12				I	Analog Pin Used For Digital Input 245
A8					I	ADC-A Input 8
CMP2_HP4					I	CMPSS-2 High Comparator Positive Input 4
CMP2_LP4					I	CMPSS-2 Low Comparator Positive Input 4
CMP4_HP4		16	9	9	I	CMPSS-4 High Comparator Positive Input 4
CMP4_LP4					I	CMPSS-4 Low Comparator Positive Input 4
PGA1_OUT					O	PGA-1 Output
AIO241	0, 4, 8, 12				I	Analog Pin Used For Digital Input 241
A9					I	ADC-A Input 9
CMP2_HP2					I	CMPSS-2 High Comparator Positive Input 2
CMP2_LP2					I	CMPSS-2 Low Comparator Positive Input 2
CMP4_HP0		20	13	13	I	CMPSS-4 High Comparator Positive Input 0
CMP4_LP0					I	CMPSS-4 Low Comparator Positive Input 0
GPIO227					I/O	General-Purpose Input Output 227 This pin also has digital mux functions which are described in the GPIO section of this table.
A10					I	ADC-A Input 10
CMP2_HN0					I	CMPSS-2 High Comparator Negative Input 0
CMP2_HP3					I	CMPSS-2 High Comparator Positive Input 3
CMP2_LN0		21	13	13	I	CMPSS-2 Low Comparator Negative Input 0
CMP2_LP3					I	CMPSS-2 Low Comparator Positive Input 3
GPIO230					I/O	General-Purpose Input Output 230 This pin also has digital mux functions which are described in the GPIO section of this table.
A11					I	ADC-A Input 11
CMP1_HN1					I	CMPSS-1 High Comparator Negative Input 1
CMP1_HP1					I	CMPSS-1 High Comparator Positive Input 1
CMP1_LN1		8	6	6	I	CMPSS-1 Low Comparator Negative Input 1
CMP1_LP1					I	CMPSS-1 Low Comparator Positive Input 1
PGA1_INP1					I	PGA-1 Plus 1
AIO237	0, 4, 8, 12				I	Analog Pin Used For Digital Input 237
A12					I	ADC-A Input 12
CMP2_HN1					I	CMPSS-2 High Comparator Negative Input 1
CMP2_HP1					I	CMPSS-2 High Comparator Positive Input 1
CMP2_LN1		14	8	8	I	CMPSS-2 Low Comparator Negative Input 1
CMP2_LP1					I	CMPSS-2 Low Comparator Positive Input 1
CMP4_HP2					I	CMPSS-4 High Comparator Positive Input 2
CMP4_LP2					I	CMPSS-4 Low Comparator Positive Input 2
AIO238	0, 4, 8, 12				I	Analog Pin Used For Digital Input 238

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
A14		7	5	5	I	ADC-A Input 14
CMP3_HP4					I	CMPSS-3 High Comparator Positive Input 4
CMP3_LP4					I	CMPSS-3 Low Comparator Positive Input 4
AIO239	0, 4, 8, 12				I	Analog Pin Used For Digital Input 239
A15		7	5	5	I	ADC-A Input 15
CMP1_HN0					I	CMPSS-1 High Comparator Negative Input 0
CMP1_HP3					I	CMPSS-1 High Comparator Positive Input 3
CMP1_LN0					I	CMPSS-1 Low Comparator Negative Input 0
CMP1_LP3					I	CMPSS-1 Low Comparator Positive Input 3
AIO233	0, 4, 8, 12				I	Analog Pin Used For Digital Input 233
A16		2	32	32	I	ADC-A Input 16
GPIO28					I/O	General-Purpose Input Output 28 This pin also has digital mux functions which are described in the GPIO section of this table.
PGA1_INP2					I	PGA-1 Plus 2
A19		23			I	ADC-A Input 19
GPIO13					I/O	General-Purpose Input Output 13 This pin also has digital mux functions which are described in the GPIO section of this table.
A20		24			I	ADC-A Input 20
GPIO12					I/O	General-Purpose Input Output 12 This pin also has digital mux functions which are described in the GPIO section of this table.
CMP3_HP0		4	2	2	I	CMPSS-3 High Comparator Positive Input 0
CMP3_LP0					I	CMPSS-3 Low Comparator Positive Input 0
GPIO226					I/O	General-Purpose Input Output 226 This pin also has digital mux functions which are described in the GPIO section of this table.
PGA1_INP3					I	PGA-1 Plus 3
VREFHI		12	11	11	I	ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor and a 10Ohm resistor in series on this pin. This capacitor and resistor should be placed as close to the device as possible between the VREFHI and VREFLO pins. On the 32 QFN package, VREFHI is internally tied to VDDA.
VREFLO		13	10	10	I	ADC Low Reference, should be tied to VSSA
GPIO						
GPIO0	0, 4, 8, 12	42	28	28	I/O	General-Purpose Input Output 0
MCPWM1_1A	1				O	MCPWM-1 Output 1A
OUTPUTXBAR7	3				O	Output X-BAR Output 7
SCIA_RX	5				I	SCI-A Receive Data
I2CA_SDA	6				I/OD	I2C-A Open-Drain Bidirectional Data
SPIA_PTE	7				I/O	SPI-A Peripheral Transmit Enable (PTE)
EQEP1_INDEX	13				I/O	eQEP-1 Index
MCPWM1_3A	15				O	MCPWM-1 Output 3A

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
GPIO1	0, 4, 8, 12	41	27	27	I/O	General-Purpose Input Output 1
MCPWM1_1B	1				O	MCPWM-1 Output 1B
OUTPUTXBAR4	3				O	Output X-BAR Output 4
SCIA_TX	5				O	SCI-A Transmit Data
I2CA_SCL	6				I/OD	I2C-A Open-Drain Bidirectional Clock
SPIA_POCI	7				I/O	SPI-A Peripheral Out, Controller In (POCI)
EQEP1_STROBE	9				I/O	eQEP-1 Strobe
MCPWM1_3B	15				O	MCPWM-1 Output 3B
GPIO2	0, 4, 8, 12	40			I/O	General-Purpose Input Output 2
MCPWM1_2A	1				O	MCPWM-1 Output 2A
OUTPUTXBAR1	5				O	Output X-BAR Output 1
SPIA_PICO	7				I/O	SPI-A Peripheral In, Controller Out (PICO)
SCIA_TX	9				O	SCI-A Transmit Data
I2CA_SDA	11				I/OD	I2C-A Open-Drain Bidirectional Data
GPIO3	0, 4, 8, 12	39	26	26	I/O	General-Purpose Input Output 3
MCPWM1_2B	1				O	MCPWM-1 Output 2B
OUTPUTXBAR2	2, 5				O	Output X-BAR Output 2
SPIA_CLK	7				I/O	SPI-A Clock
SCIA_RX	9				I	SCI-A Receive Data
I2CA_SCL	11				I/OD	I2C-A Open-Drain Bidirectional Clock
GPIO4	0, 4, 8, 12	38	25	25	I/O	General-Purpose Input Output 4
MCPWM1_3A	1				O	MCPWM-1 Output 3A
I2CA_SCL	2				I/OD	I2C-A Open-Drain Bidirectional Clock
OUTPUTXBAR3	5				O	Output X-BAR Output 3
EQEP1_STROBE	9				I/O	eQEP-1 Strobe
SPIA_POCI	14				I/O	SPI-A Peripheral Out, Controller In (POCI)
MCPWM1_1A	15				O	MCPWM-1 Output 1A
GPIO5	0, 4, 8, 12	47	30	30	I/O	General-Purpose Input Output 5
MCPWM1_3B	1				O	MCPWM-1 Output 3B
I2CA_SDA	2				I/OD	I2C-A Open-Drain Bidirectional Data
OUTPUTXBAR3	3				O	Output X-BAR Output 3
SPIA_PTE	7				I/O	SPI-A Peripheral Transmit Enable (PTE)
SPIA_POCI	9				I/O	SPI-A Peripheral Out, Controller In (POCI)
SCIA_RX	11				I	SCI-A Receive Data
MCPWM1_1B	15				O	MCPWM-1 Output 1B
GPIO6	0, 4, 8, 12	48			I/O	General-Purpose Input Output 6
OUTPUTXBAR4	2				O	Output X-BAR Output 4
SYNCOUT	3				O	External MCPWM Synchronization Pulse
EQEP1_A	5				I	eQEP-1 Input A
MCPWM1_3A	10				O	MCPWM-1 Output 3A
MCPWM1_2A	15				O	MCPWM-1 Output 2A

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
GPIO7	0, 4, 8, 12	43		29	I/O	General-Purpose Input Output 7
MCPWM1_2A	2				O	MCPWM-1 Output 2A
OUTPUTXBAR5	3				O	Output X-BAR Output 5
EQEP1_B	5				I	eQEP-1 Input B
SPIA_PICO	7				I/O	SPI-A Peripheral In, Controller Out (PICO)
MCPWM3_1A	9				O	MCPWM-3 Output 1A
SCIA_TX	11				O	SCI-A Transmit Data
MCPWM1_2B	15				O	MCPWM-1 Output 2B
GPIO8	0, 4, 8, 12				I/O	General-Purpose Input Output 8
ADCSOCAO	3				O	ADC Start of Conversion A for External ADC
EQEP1_STROBE	5				I/O	eQEP-1 Strobe
SCIA_TX	6				O	SCI-A Transmit Data
SPIA_PICO	7				I/O	SPI-A Peripheral In, Controller Out (PICO)
I2CA_SCL	9				I/OD	I2C-A Open-Drain Bidirectional Clock
GPIO9	0, 4, 8, 12				I/O	General-Purpose Input Output 9
SCIB_TX	2				O	SCI-B Transmit Data
OUTPUTXBAR6	3				O	Output X-BAR Output 6
EQEP1_INDEX	5				I/O	eQEP-1 Index
SCIA_RX	6				I	SCI-A Receive Data
SPIA_CLK	7				I/O	SPI-A Clock
MCPWM1_1B	9				O	MCPWM-1 Output 1B
I2CA_SCL	14				I/OD	I2C-A Open-Drain Bidirectional Clock
GPIO10	0, 4, 8, 12				I/O	General-Purpose Input Output 10
MCPWM1_2B	2				O	MCPWM-1 Output 2B
ADCSOCBO	3				O	ADC Start of Conversion B for External ADC
EQEP1_A	5				I	eQEP-1 Input A
SCIB_TX	6				O	SCI-B Transmit Data
SPIA_POCI	7				I/O	SPI-A Peripheral Out, Controller In (POCI)
I2CA_SDA	9				I/OD	I2C-A Open-Drain Bidirectional Data
GPIO11	0, 4, 8, 12		14	14	I/O	General-Purpose Input Output 11
OUTPUTXBAR7	3				O	Output X-BAR Output 7
EQEP1_B	5				I	eQEP-1 Input B
SCIB_RX	6				I	SCI-B Receive Data
SPIA_PTE	7				I/O	SPI-A Peripheral Transmit Enable (PTE)
MCPWM3_1B	9				O	MCPWM-3 Output 1B
EQEP1_A	11				I	eQEP-1 Input A
SPIA_PICO	13				I/O	SPI-A Peripheral In, Controller Out (PICO)
GPIO12	0, 4, 8, 12	24			I/O	General-Purpose Input Output 12 This pin also has analog functions which are described in the ANALOG section of this table.
MCPWM3_1A	1				O	MCPWM-3 Output 1A
EQEP1_STROBE	5				I/O	eQEP-1 Strobe
SCIB_TX	6				O	SCI-B Transmit Data
SPIA_CLK	11				I/O	SPI-A Clock

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
GPIO13	0, 4, 8, 12	23			I/O	General-Purpose Input Output 13 This pin also has analog functions which are described in the ANALOG section of this table.
MCPWM3_1B	1				O	MCPWM-3 Output 1B
EQEP1_INDEX	5				I/O	eQEP-1 Index
SCIB_RX	6				I	SCI-B Receive Data
SPIA_POCI	11				I/O	SPI-A Peripheral Out, Controller In (POCI)
GPIO16	0, 4, 8, 12	26			I/O	General-Purpose Input Output 16
SPIA_PICO	1				I/O	SPI-A Peripheral In, Controller Out (PICO)
OUTPUTXBAR7	3				O	Output X-BAR Output 7
SCIA_TX	6				O	SCI-A Transmit Data
EQEP1_STROBE	9				I/O	eQEP-1 Strobe
XCLKOUT	11				O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
EQEP1_B	13				I	eQEP-1 Input B
GPIO17	0, 4, 8, 12				I/O	General-Purpose Input Output 17
SPIA_POCI	1				I/O	SPI-A Peripheral Out, Controller In (POCI)
OUTPUTXBAR8	3				O	Output X-BAR Output 8
EQEP1_INDEX	9				I/O	eQEP-1 Index
GPIO18	0, 4, 8, 12	33	21	21	I/O	General-Purpose Input Output 18
SPIA_CLK	1				I/O	SPI-A Clock
SCIB_TX	2				O	SCI-B Transmit Data
I2CA_SCL	6				I/OD	I2C-A Open-Drain Bidirectional Clock
EQEP1_A	9				I	eQEP-1 Input A
XCLKOUT	11				O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
X2	ALT				I/O	Crystal oscillator output.
GPIO19	0, 4, 8, 12	34	22	22	I/O	General-Purpose Input Output 19
SPIA_PTE	1				I/O	SPI-A Peripheral Transmit Enable (PTE)
SCIB_RX	2				I	SCI-B Receive Data
I2CA_SDA	6				I/OD	I2C-A Open-Drain Bidirectional Data
EQEP1_B	9				I	eQEP-1 Input B
X1	ALT				I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.
GPIO20	0, 4, 8, 12				I/O	General-Purpose Input Output 20
EQEP1_A	1				I	eQEP-1 Input A
SPIA_PICO	6				I/O	SPI-A Peripheral In, Controller Out (PICO)
I2CA_SCL	11				I/OD	I2C-A Open-Drain Bidirectional Clock
UARTA_TX	15				O	UART-A Transmit Data

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
GPIO21	0, 4, 8, 12				I/O	General-Purpose Input Output 21
EQEP1_B	1				I	eQEP-1 Input B
SPIA_POCI	6				I/O	SPI-A Peripheral Out, Controller In (POCI)
I2CA_SDA	11				I/OD	I2C-A Open-Drain Bidirectional Data
UARTA_RX	15				I	UART-A Receive Data
GPIO22	0, 4, 8, 12				I/O	General-Purpose Input Output 22
EQEP1_STROBE	1				I/O	eQEP-1 Strobe
SCIB_TX	3				O	SCI-B Transmit Data
GPIO23	0, 4, 8, 12				I/O	General-Purpose Input Output 23
EQEP1_INDEX	1				I/O	eQEP-1 Index
SPIA_PTE	2				I/O	SPI-A Peripheral Transmit Enable (PTE)
SCIB_RX	3				I	SCI-B Receive Data
GPIO24	0, 4, 8, 12				I/O	General-Purpose Input Output 24
OUTPUTXBAR1	1				O	Output X-BAR Output 1
EQEP1_A	2				I	eQEP-1 Input A
SPIA_PTE	3	27	15	15	I/O	SPI-A Peripheral Transmit Enable (PTE)
SPIA_PICO	6				I/O	SPI-A Peripheral In, Controller Out (PICO)
SCIA_TX	11				O	SCI-A Transmit Data
ERRORSTS	13				O	Error Status Output. This signal requires an external pulldown.
GPIO28	0, 4, 8, 12				I/O	General-Purpose Input Output 28 This pin also has analog functions which are described in the ANALOG section of this table.
SCIA_RX	1				I	SCI-A Receive Data
OUTPUTXBAR8	2				O	Output X-BAR Output 8
MCPWM3_1A	3				O	MCPWM-3 Output 1A
OUTPUTXBAR5	5				O	Output X-BAR Output 5
EQEP1_A	6	2	32	32	I	eQEP-1 Input A
EQEP1_STROBE	9				I/O	eQEP-1 Strobe
UARTA_TX	10				O	UART-A Transmit Data
SPIA_CLK	11				I/O	SPI-A Clock
ERRORSTS	13				O	Error Status Output. This signal requires an external pulldown.
I2CA_SDA	14				I/OD	I2C-A Open-Drain Bidirectional Data
GPIO29	0, 4, 8, 12				I/O	General-Purpose Input Output 29
SCIA_TX	1				O	SCI-A Transmit Data
MCPWM1_2A	2				O	MCPWM-1 Output 2A
MCPWM3_1B	3				O	MCPWM-3 Output 1B
OUTPUTXBAR6	5				O	Output X-BAR Output 6
EQEP1_B	6	1	31	31	I	eQEP-1 Input B
EQEP1_INDEX	9				I/O	eQEP-1 Index
UARTA_RX	10				I	UART-A Receive Data
SPIA_PTE	11				I/O	SPI-A Peripheral Transmit Enable (PTE)
ERRORSTS	13				O	Error Status Output. This signal requires an external pulldown.
I2CA_SCL	14				I/OD	I2C-A Open-Drain Bidirectional Clock

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
GPIO30	0, 4, 8, 12				I/O	General-Purpose Input Output 30
OUTPUTXBAR7	5				O	Output X-BAR Output 7
EQEP1_STROBE	6				I/O	eQEP-1 Strobe
MCPWM1_1A	11				O	MCPWM-1 Output 1A
GPIO32	0, 4, 8, 12	32	20	20	I/O	General-Purpose Input Output 32
I2CA_SDA	1				I/OD	I2C-A Open-Drain Bidirectional Data
EQEP1_INDEX	2				I/O	eQEP-1 Index
SPIA_CLK	3				I/O	SPI-A Clock
UARTA_RX	6				I	UART-A Receive Data
ADCSOCBO	13				O	ADC Start of Conversion B for External ADC
GPIO33	0, 4, 8, 12	25			I/O	General-Purpose Input Output 33
I2CA_SCL	1				I/OD	I2C-A Open-Drain Bidirectional Clock
OUTPUTXBAR4	5				O	Output X-BAR Output 4
UARTA_TX	6				O	UART-A Transmit Data
EQEP1_B	11				I	eQEP-1 Input B
ADCSOCAO	13				O	ADC Start of Conversion A for External ADC
GPIO35	0, 4, 8, 12	31	19	19	I/O	General-Purpose Input Output 35
SCIA_RX	1				I	SCI-A Receive Data
SPIA_POCI	2				I/O	SPI-A Peripheral Out, Controller In (POCI)
I2CA_SDA	3				I/OD	I2C-A Open-Drain Bidirectional Data
UARTA_RX	7				I	UART-A Receive Data
EQEP1_A	9				I	eQEP-1 Input A
TDI	15				I	JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input.
GPIO37	0, 4, 8, 12	29	17	17	I/O	General-Purpose Input Output 37
OUTPUTXBAR2	1				O	Output X-BAR Output 2
SPIA_PTE	2				I/O	SPI-A Peripheral Transmit Enable (PTE)
I2CA_SCL	3				I/OD	I2C-A Open-Drain Bidirectional Clock
SCIA_TX	5				O	SCI-A Transmit Data
UARTA_TX	7				O	UART-A Transmit Data
EQEP1_B	9				I	eQEP-1 Input B
SYNCOUT	13				O	External MCPWM Synchronization Pulse
TDO	15				O	JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input.
GPIO39	0, 4, 8, 12				I/O	General-Purpose Input Output 39
EQEP1_INDEX	9, 14				I/O	eQEP-1 Index
SYNCOUT	13				O	External MCPWM Synchronization Pulse

Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
GPIO40	0, 4, 8, 12				I/O	General-Purpose Input Output 40
MCPWM1_2B	5				O	MCPWM-1 Output 2B
SCIB_TX	9				O	SCI-B Transmit Data
EQEP1_A	10				I	eQEP-1 Input A
GPIO41	0, 4, 8, 12				I/O	General-Purpose Input Output 41
MCPWM3_1A	1				O	MCPWM-3 Output 1A
SPIA_CLK	2				I/O	SPI-A Clock
MCPWM1_2A	5				O	MCPWM-1 Output 2A
SCIB_RX	9				I	SCI-B Receive Data
EQEP1_B	10				I	eQEP-1 Input B
GPIO43	0, 4, 8, 12				I/O	General-Purpose Input Output 43
OUTPUTXBAR6	3				O	Output X-BAR Output 6
I2CA_SCL	6	36		24	I/OD	I2C-A Open-Drain Bidirectional Clock
UARTA_TX	7				O	UART-A Transmit Data
EQEP1_INDEX	10				I/O	eQEP-1 Index
GPIO45	0, 4, 8, 12				I/O	General-Purpose Input Output 45
OUTPUTXBAR8	3	45			O	Output X-BAR Output 8
SPIA_POCI	6				I/O	SPI-A Peripheral Out, Controller In (POCI)
GPIO46	0, 4, 8, 12				I/O	General-Purpose Input Output 46
GPIO224	0, 4, 8, 12				I/O	General-Purpose Input Output 224 This pin also has analog functions which are described in the ANALOG section of this table.
OUTPUTXBAR3	5				O	Output X-BAR Output 3
SPIA_PICO	6	6	4	4	I/O	SPI-A Peripheral In, Controller Out (PICO)
MCPWM1_1A	9				O	MCPWM-1 Output 1A
EQEP1_A	11				I	eQEP-1 Input A
UARTA_TX	14				O	UART-A Transmit Data
GPIO226	0, 4, 8, 12				I/O	General-Purpose Input Output 226 This pin also has analog functions which are described in the ANALOG section of this table.
SPIA_CLK	6	4	2	2	I/O	SPI-A Clock
MCPWM1_1B	9				O	MCPWM-1 Output 1B
EQEP1_STROBE	11				I/O	eQEP-1 Strobe
UARTA_RX	14				I	UART-A Receive Data
GPIO227	0, 4, 8, 12				I/O	General-Purpose Input Output 227 This pin also has analog functions which are described in the ANALOG section of this table.
I2CA_SCL	1	20	13	13	I/OD	I2C-A Open-Drain Bidirectional Clock
MCPWM1_3A	3				O	MCPWM-1 Output 3A
OUTPUTXBAR1	5				O	Output X-BAR Output 1
MCPWM1_2B	6				O	MCPWM-1 Output 2B
GPIO228	0, 4, 8, 12				I/O	General-Purpose Input Output 228 This pin also has analog functions which are described in the ANALOG section of this table.
ADCSOCAO	3	4	2	2	O	ADC Start of Conversion A for External ADC
SPIA_POCI	6				I/O	SPI-A Peripheral Out, Controller In (POCI)
MCPWM1_2B	9				O	MCPWM-1 Output 2B
EQEP1_B	11				I	eQEP-1 Input B

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
GPIO230	0, 4, 8, 12	21	13	13	I/O	General-Purpose Input Output 230 This pin also has analog functions which are described in the ANALOG section of this table.
I2CA_SDA	1, 7				I/OD	I2C-A Open-Drain Bidirectional Data
MCPWM1_3B	3				O	MCPWM-1 Output 3B
MCPWM1_2A	6				O	MCPWM-1 Output 2A
GPIO242	0, 4, 8, 12	5	3	3	I/O	General-Purpose Input Output 242 This pin also has analog functions which are described in the ANALOG section of this table.
MCPWM1_2A	3				O	MCPWM-1 Output 2A
OUTPUTXBAR2	5				O	Output X-BAR Output 2
SPIA_PTE	6				I/O	SPI-A Peripheral Transmit Enable (PTE)
EQEP1_INDEX	11				I/O	eQEP-1 Index
GPIO243	0, 4, 8, 12				I/O	General-Purpose Input Output 243
XCLKOUT	1				O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.
TEST, JTAG, AND RESET						
TCK		28	16	16	I	JTAG test clock with internal pullup.
TMS		30	18	18	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.
XRSn		3	1	1	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.
POWER AND GROUND						
VDDA		18	11	11		3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor on each pin. On the 32 QFN package, VREFHI is internally tied to VDDA. See the Power Management Module (PMM) section for usage details.
VDDIO		35, 46	23	23		3.3-V Digital I/O Power Pins. See the Power Management Module (PMM) section for usage details.
VSS		22, 37, 44	24, 29	PAD		Digital Ground. For QFN packages, the ground pad on the bottom of the package must be soldered to the ground plane of the PCB.

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Table 5-1. Pin Attributes (continued)

SIGNAL NAME	MUX POSITION	48 PT	32 VFC	32 RHB	PIN TYPE	DESCRIPTION
VSSA		17	10	10		Analog Ground

5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	48 PT	32 VFC	32 RHB
A0	I	ADC-A Input 0	11	7	7
A1	I	ADC-A Input 1	10	7	7
A2	I	ADC-A Input 2	6	4	4
A3	I	ADC-A Input 3	5	3	3
A4	I	ADC-A Input 4	19	12	12
A5	I	ADC-A Input 5	9	6	6
A6	I	ADC-A Input 6	4	2	2
A7	I	ADC-A Input 7	15	8	8
A8	I	ADC-A Input 8	16	9	9
A9	I	ADC-A Input 9	20	13	13
A10	I	ADC-A Input 10	21	13	13
A11	I	ADC-A Input 11	8	6	6
A12	I	ADC-A Input 12	14	8	8
A14	I	ADC-A Input 14	7	5	5
A15	I	ADC-A Input 15	7	5	5
A16	I	ADC-A Input 16	2	32	32
A19	I	ADC-A Input 19	23		
A20	I	ADC-A Input 20	24		
AIO225	I	Analog Pin Used For Digital Input 225	19	12	12
AIO231	I	Analog Pin Used For Digital Input 231	11	7	7
AIO232	I	Analog Pin Used For Digital Input 232	10	7	7
AIO233	I	Analog Pin Used For Digital Input 233	7	5	5
AIO237	I	Analog Pin Used For Digital Input 237	8	6	6
AIO238	I	Analog Pin Used For Digital Input 238	14	8	8
AIO239	I	Analog Pin Used For Digital Input 239	7	5	5
AIO241	I	Analog Pin Used For Digital Input 241	16	9	9
AIO244	I	Analog Pin Used For Digital Input 244	9	6	6
AIO245	I	Analog Pin Used For Digital Input 245	15	8	8
CMP1_HN0	I	CMPSS-1 High Comparator Negative Input 0	7	5	5
CMP1_HN1	I	CMPSS-1 High Comparator Negative Input 1	8	6	6
CMP1_HP0	I	CMPSS-1 High Comparator Positive Input 0	6	4	4
CMP1_HP1	I	CMPSS-1 High Comparator Positive Input 1	8	6	6
CMP1_HP2	I	CMPSS-1 High Comparator Positive Input 2	4	2	2
CMP1_HP3	I	CMPSS-1 High Comparator Positive Input 3	7	5	5
CMP1_HP4	I	CMPSS-1 High Comparator Positive Input 4	10	7	7
CMP1_LN0	I	CMPSS-1 Low Comparator Negative Input 0	7	5	5

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	48 PT	32 VFC	32 RHB
CMP1_LN1	I	CMPSS-1 Low Comparator Negative Input 1	8	6	6
CMP1_LP0	I	CMPSS-1 Low Comparator Positive Input 0	6	4	4
CMP1_LP1	I	CMPSS-1 Low Comparator Positive Input 1	8	6	6
CMP1_LP2	I	CMPSS-1 Low Comparator Positive Input 2	4	2	2
CMP1_LP3	I	CMPSS-1 Low Comparator Positive Input 3	7	5	5
CMP1_LP4	I	CMPSS-1 Low Comparator Positive Input 4	10	7	7
CMP2_HN0	I	CMPSS-2 High Comparator Negative Input 0	21	13	13
CMP2_HN1	I	CMPSS-2 High Comparator Negative Input 1	14	8	8
CMP2_HP0	I	CMPSS-2 High Comparator Positive Input 0	19	12	12
CMP2_HP1	I	CMPSS-2 High Comparator Positive Input 1	14	8	8
CMP2_HP2	I	CMPSS-2 High Comparator Positive Input 2	20	13	13
CMP2_HP3	I	CMPSS-2 High Comparator Positive Input 3	21	13	13
CMP2_HP4	I	CMPSS-2 High Comparator Positive Input 4	16	9	9
CMP2_LN0	I	CMPSS-2 Low Comparator Negative Input 0	21	13	13
CMP2_LN1	I	CMPSS-2 Low Comparator Negative Input 1	14	8	8
CMP2_LP0	I	CMPSS-2 Low Comparator Positive Input 0	19	12	12
CMP2_LP1	I	CMPSS-2 Low Comparator Positive Input 1	14	8	8
CMP2_LP2	I	CMPSS-2 Low Comparator Positive Input 2	20	13	13
CMP2_LP3	I	CMPSS-2 Low Comparator Positive Input 3	21	13	13
CMP2_LP4	I	CMPSS-2 Low Comparator Positive Input 4	16	9	9
CMP3_HN0	I	CMPSS-3 High Comparator Negative Input 0	5	3	3
CMP3_HN1	I	CMPSS-3 High Comparator Negative Input 1	9	6	6
CMP3_HP0	I	CMPSS-3 High Comparator Positive Input 0	4	2	2
CMP3_HP1	I	CMPSS-3 High Comparator Positive Input 1	9	6	6
CMP3_HP2	I	CMPSS-3 High Comparator Positive Input 2	11	7	7
CMP3_HP3	I	CMPSS-3 High Comparator Positive Input 3	5	3	3

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	48 PT	32 VFC	32 RHB
CMP3_HP4	I	CMPSS-3 High Comparator Positive Input 4	7	5	5
CMP3_LN0	I	CMPSS-3 Low Comparator Negative Input 0	5	3	3
CMP3_LN1	I	CMPSS-3 Low Comparator Negative Input 1	9	6	6
CMP3_LP0	I	CMPSS-3 Low Comparator Positive Input 0	4	2	2
CMP3_LP1	I	CMPSS-3 Low Comparator Positive Input 1	9	6	6
CMP3_LP2	I	CMPSS-3 Low Comparator Positive Input 2	11	7	7
CMP3_LP3	I	CMPSS-3 Low Comparator Positive Input 3	5	3	3
CMP3_LP4	I	CMPSS-3 Low Comparator Positive Input 4	7	5	5
CMP4_HN0	I	CMPSS-4 High Comparator Negative Input 0	19	12	12
CMP4_HN1	I	CMPSS-4 High Comparator Negative Input 1	15	8	8
CMP4_HP0	I	CMPSS-4 High Comparator Positive Input 0	20	13	13
CMP4_HP1	I	CMPSS-4 High Comparator Positive Input 1	15	8	8
CMP4_HP2	I	CMPSS-4 High Comparator Positive Input 2	14	8	8
CMP4_HP3	I	CMPSS-4 High Comparator Positive Input 3	19	12	12
CMP4_HP4	I	CMPSS-4 High Comparator Positive Input 4	16	9	9
CMP4_LN0	I	CMPSS-4 Low Comparator Negative Input 0	19	12	12
CMP4_LN1	I	CMPSS-4 Low Comparator Negative Input 1	15	8	8
CMP4_LP0	I	CMPSS-4 Low Comparator Positive Input 0	20	13	13
CMP4_LP1	I	CMPSS-4 Low Comparator Positive Input 1	15	8	8
CMP4_LP2	I	CMPSS-4 Low Comparator Positive Input 2	14	8	8
CMP4_LP3	I	CMPSS-4 Low Comparator Positive Input 3	19	12	12
CMP4_LP4	I	CMPSS-4 Low Comparator Positive Input 4	16	9	9
PGA1_INM1	I	PGA-1 Minus 1	19	12	12
PGA1_INM2	I	PGA-1 Minus 2	11	7	7
PGA1_INP1	I	PGA-1 Plus 1	8	6	6
PGA1_INP2	I	PGA-1 Plus 2	2	32	32
PGA1_INP3	I	PGA-1 Plus 3	4	2	2
PGA1_OUT	O	PGA-1 Output	16	9	9

Table 5-2. Analog Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	48 PT	32 VFC	32 RHB
VREFHI	I	ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2-µF capacitor and a 10Ohm resistor in series on this pin. This capacitor and resistor should be placed as close to the device as possible between the VREFHI and VREFLO pins. On the 32 QFN package, VREFHI is internally tied to VDDA.	12	11	11
VREFLO	I	ADC Low Reference, should be tied to VSSA	13	10	10

5.3.2 Digital Signals

Table 5-3. Digital Signals

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	48 PT	32 VFC	32 RHB
ADCSOCAO	O	ADC Start of Conversion A for External ADC	8, 33, 228	4, 25	2	2
ADCSOCBO	O	ADC Start of Conversion B for External ADC	10, 32	32	20	20
EQEP1_A	I	eQEP-1 Input A	6, 10, 11, 18, 20, 24, 28, 35, 40, 224	2, 6, 27, 31, 33, 48	4, 14, 15, 19, 21, 32	4, 14, 15, 19, 21, 32
EQEP1_B	I	eQEP-1 Input B	7, 11, 16, 19, 21, 29, 33, 37, 41, 228	1, 4, 25, 26, 29, 34, 43	2, 14, 17, 22, 31	2, 14, 17, 22, 29, 31
EQEP1_INDEX	I/O	eQEP-1 Index	0, 9, 13, 17, 23, 29, 32, 39, 43, 242	1, 5, 23, 32, 36, 42	3, 20, 28, 31	3, 20, 24, 28, 31
EQEP1_STROBE	I/O	eQEP-1 Strobe	1, 4, 8, 12, 16, 22, 28, 30, 226	2, 4, 24, 26, 38, 41	2, 25, 27, 32	2, 25, 27, 32
ERRORSTS	O	Error Status Output. This signal requires an external pulldown.	24, 28, 29	1, 2, 27	15, 31, 32	15, 31, 32
GPIO0	I/O	General-Purpose Input Output 0	0	42	28	28
GPIO1	I/O	General-Purpose Input Output 1	1	41	27	27
GPIO2	I/O	General-Purpose Input Output 2	2	40		
GPIO3	I/O	General-Purpose Input Output 3	3	39	26	26
GPIO4	I/O	General-Purpose Input Output 4	4	38	25	25
GPIO5	I/O	General-Purpose Input Output 5	5	47	30	30
GPIO6	I/O	General-Purpose Input Output 6	6	48		
GPIO7	I/O	General-Purpose Input Output 7	7	43		29
GPIO8	I/O	General-Purpose Input Output 8	8			
GPIO9	I/O	General-Purpose Input Output 9	9			
GPIO10	I/O	General-Purpose Input Output 10	10			
GPIO11	I/O	General-Purpose Input Output 11	11		14	14
GPIO12	I/O	General-Purpose Input Output 12	12	24		
GPIO13	I/O	General-Purpose Input Output 13	13	23		
GPIO16	I/O	General-Purpose Input Output 16	16	26		
GPIO17	I/O	General-Purpose Input Output 17	17			
GPIO18	I/O	General-Purpose Input Output 18	18	33	21	21
GPIO19	I/O	General-Purpose Input Output 19	19	34	22	22
GPIO20	I/O	General-Purpose Input Output 20	20			
GPIO21	I/O	General-Purpose Input Output 21	21			
GPIO22	I/O	General-Purpose Input Output 22	22			
GPIO23	I/O	General-Purpose Input Output 23	23			
GPIO24	I/O	General-Purpose Input Output 24	24	27	15	15
GPIO28	I/O	General-Purpose Input Output 28	28	2	32	32
GPIO29	I/O	General-Purpose Input Output 29	29	1	31	31
GPIO30	I/O	General-Purpose Input Output 30	30			
GPIO32	I/O	General-Purpose Input Output 32	32	32	20	20
GPIO33	I/O	General-Purpose Input Output 33	33	25		
GPIO35	I/O	General-Purpose Input Output 35	35	31	19	19
GPIO37	I/O	General-Purpose Input Output 37	37	29	17	17
GPIO39	I/O	General-Purpose Input Output 39	39			
GPIO40	I/O	General-Purpose Input Output 40	40			
GPIO41	I/O	General-Purpose Input Output 41	41			
GPIO43	I/O	General-Purpose Input Output 43	43	36		24
GPIO45	I/O	General-Purpose Input Output 45	45	45		
GPIO46	I/O	General-Purpose Input Output 46	46			
GPIO224	I/O	General-Purpose Input Output 224	224	6	4	4
GPIO226	I/O	General-Purpose Input Output 226	226	4	2	2
GPIO227	I/O	General-Purpose Input Output 227	227	20	13	13
GPIO228	I/O	General-Purpose Input Output 228	228	4	2	2
GPIO230	I/O	General-Purpose Input Output 230	230	21	13	13
GPIO242	I/O	General-Purpose Input Output 242	242	5	3	3

Table 5-3. Digital Signals (continued)

SIGNAL NAME	PIN TYPE	DESCRIPTION	GPIO	48 PT	32 VFC	32 RHB
GPIO243	I/O	General-Purpose Input Output 243	243			
I2CA_SCL	I/OD	I2C-A Open-Drain Bidirectional Clock	1, 3, 4, 8, 9, 18, 20, 29, 33, 37, 43, 227	1, 20, 25, 29, 33, 36, 38, 39, 41	13, 17, 21, 25, 26, 27, 31	13, 17, 21, 24, 25, 26, 27, 31
I2CA_SDA	I/OD	I2C-A Open-Drain Bidirectional Data	0, 2, 5, 10, 19, 21, 28, 32, 35, 230	2, 21, 31, 32, 34, 40, 42, 47	13, 19, 20, 22, 28, 30, 32	13, 19, 20, 22, 28, 30, 32
MCPWM1_1A	O	MCPWM-1 Output 1A	0, 4, 30, 224	6, 38, 42	4, 25, 28	4, 25, 28
MCPWM1_1B	O	MCPWM-1 Output 1B	1, 5, 9, 226	4, 41, 47	2, 27, 30	2, 27, 30
MCPWM1_2A	O	MCPWM-1 Output 2A	2, 6, 7, 29, 41, 230, 242	1, 5, 21, 40, 43, 48	3, 13, 31	3, 13, 29, 31
MCPWM1_2B	O	MCPWM-1 Output 2B	3, 7, 10, 40, 227, 228	4, 20, 39, 43	2, 13, 26	2, 13, 26, 29
MCPWM1_3A	O	MCPWM-1 Output 3A	0, 4, 6, 227	20, 38, 42, 48	13, 25, 28	13, 25, 28
MCPWM1_3B	O	MCPWM-1 Output 3B	1, 5, 230	21, 41, 47	13, 27, 30	13, 27, 30
MCPWM3_1A	O	MCPWM-3 Output 1A	7, 12, 28, 41	2, 24, 43	32	29, 32
MCPWM3_1B	O	MCPWM-3 Output 1B	11, 13, 29	1, 23	14, 31	14, 31
OUTPUTXBAR1	O	Output X-BAR Output 1	2, 24, 227	20, 27, 40	13, 15	13, 15
OUTPUTXBAR2	O	Output X-BAR Output 2	3, 37, 242	5, 29, 39	3, 17, 26	3, 17, 26
OUTPUTXBAR3	O	Output X-BAR Output 3	4, 5, 224	6, 38, 47	4, 25, 30	4, 25, 30
OUTPUTXBAR4	O	Output X-BAR Output 4	1, 6, 33	25, 41, 48	27	27
OUTPUTXBAR5	O	Output X-BAR Output 5	7, 28	2, 43	32	29, 32
OUTPUTXBAR6	O	Output X-BAR Output 6	9, 29, 43	1, 36	31	24, 31
OUTPUTXBAR7	O	Output X-BAR Output 7	0, 11, 16, 30	26, 42	14, 28	14, 28
OUTPUTXBAR8	O	Output X-BAR Output 8	17, 28, 45	2, 45	32	32
SCIA_RX	I	SCI-A Receive Data	0, 3, 5, 9, 28, 35	2, 31, 39, 42, 47	19, 26, 28, 30, 32	19, 26, 28, 30, 32
SCIA_TX	O	SCI-A Transmit Data	1, 2, 7, 8, 16, 24, 29, 37	1, 26, 27, 29, 40, 41, 43	15, 17, 27, 31	15, 17, 27, 29, 31
SCIB_RX	I	SCI-B Receive Data	11, 13, 19, 23, 41	23, 34	14, 22	14, 22
SCIB_TX	O	SCI-B Transmit Data	9, 10, 12, 18, 22, 40	24, 33	21	21
SPIA_CLK	I/O	SPI-A Clock	3, 9, 12, 18, 28, 32, 41, 226	2, 4, 24, 32, 33, 39	2, 20, 21, 26, 32	2, 20, 21, 26, 32
SPIA_PICO	I/O	SPI-A Peripheral In, Controller Out (PICO)	2, 7, 8, 11, 16, 20, 24, 224	6, 26, 27, 40, 43	4, 14, 15	4, 14, 15, 29
SPIA_POCI	I/O	SPI-A Peripheral Out, Controller In (POCI)	1, 4, 5, 10, 13, 17, 21, 35, 45, 228	4, 23, 31, 38, 41, 45, 47	2, 19, 25, 27, 30	2, 19, 25, 27, 30
SPIA_PTE	I/O	SPI-A Peripheral Transmit Enable (PTE)	0, 5, 11, 19, 23, 24, 29, 37, 242	1, 5, 27, 29, 34, 42, 47	3, 14, 15, 17, 22, 28, 30, 31	3, 14, 15, 17, 22, 28, 30, 31
SYNCOUT	O	External MCPWM Synchronization Pulse	6, 37, 39	29, 48	17	17
TDI	I	JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input.	35	31	19	19
TDO	O	JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input.	37	29	17	17
UARTA_RX	I	UART-A Receive Data	21, 29, 32, 35, 226	1, 4, 31, 32	2, 19, 20, 31	2, 19, 20, 31
UARTA_TX	O	UART-A Transmit Data	20, 28, 33, 37, 43, 224	2, 6, 25, 29, 36	4, 17, 32	4, 17, 24, 32
X1	I/O	Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock.	19	34	22	22
X2	I/O	Crystal oscillator output.	18	33	21	21
XCLKOUT	O	External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device.	16, 18, 243	26, 33	21	21

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5.3.3 Power and Ground

Table 5-4. Power and Ground

SIGNAL NAME	DESCRIPTION	48 PT	32 VFC	32 RHB
VDDA	3.3-V Analog Power Pins. Place a minimum 2.2-µF decoupling capacitor on each pin. On the 32 QFN package, VREFHI is internally tied to VDDA. See the Power Management Module (PMM) section for usage details.	18	11	11
VDDIO	3.3-V Digital I/O Power Pins. See the Power Management Module (PMM) section for usage details.	35, 46	23	23
VSS	Digital Ground. For QFN packages, the ground pad on the bottom of the package must be soldered to the ground plane of the PCB.	22, 37, 44	24, 29	PAD
VSSA	Analog Ground	17	10	10

5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

SIGNAL NAME	PIN TYPE	DESCRIPTION	48 PT	32 VFC	32 RHB
TCK	I	JTAG test clock with internal pullup.	28	16	16
TMS	I/O	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation.	30	18	18
XRSn	I/OD	Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device.	3	1	1

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5.4 Pin Multiplexing

The following section lists the GPIO muxed pins.

5.4.1 GPIO Muxed Pins

Table 5-6. GPIO Muxed Pins

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO0	MCPWM1_1A		OUTPUTXBAR7	SCIA_RX	I2CA_SDA	SPIA_PTE				EQEP1_INDEX		MCPWM1_3A	
GPIO1	MCPWM1_1B		OUTPUTXBAR4	SCIA_TX	I2CA_SCL	SPIA_POCI	EQEP1_STROBE					MCPWM1_3B	
GPIO2	MCPWM1_2A			OUTPUTXBAR1		SPIA_PICO	SCIA_TX		I2CA_SDA				
GPIO3	MCPWM1_2B	OUTPUTXBAR2		OUTPUTXBAR2		SPIA_CLK	SCIA_RX		I2CA_SCL				
GPIO4	MCPWM1_3A	I2CA_SCL		OUTPUTXBAR3			EQEP1_STROBE				SPIA_POCI	MCPWM1_1A	
GPIO5	MCPWM1_3B	I2CA_SDA	OUTPUTXBAR3			SPIA_PTE	SPIA_POCI		SCIA_RX			MCPWM1_1B	
GPIO6		OUTPUTXBAR4	SYNCOUT	EQEP1_A				MCPWM1_3A				MCPWM1_2A	
GPIO7		MCPWM1_2A	OUTPUTXBAR5	EQEP1_B		SPIA_PICO	MCPWM3_1A		SCIA_TX			MCPWM1_2B	
GPIO8			ADCSOCAO	EQEP1_STROBE	SCIA_TX	SPIA_PICO	I2CA_SCL						
GPIO9		SCIB_TX	OUTPUTXBAR6	EQEP1_INDEX	SCIA_RX	SPIA_CLK	MCPWM1_1B				I2CA_SCL		
GPIO10		MCPWM1_2B	ADCSOCBO	EQEP1_A	SCIB_TX	SPIA_POCI	I2CA_SDA						
GPIO11			OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_PTE	MCPWM3_1B		EQEP1_A	SPIA_PICO			
GPIO12	MCPWM3_1A			EQEP1_STROBE	SCIB_TX				SPIA_CLK				
GPIO13	MCPWM3_1B			EQEP1_INDEX	SCIB_RX				SPIA_POCI				
GPIO16	SPIA_PICO		OUTPUTXBAR7		SCIA_TX		EQEP1_STROBE		XCLKOUT	EQEP1_B			
GPIO17	SPIA_POCI		OUTPUTXBAR8		SCIA_RX		EQEP1_INDEX						
GPIO18	SPIA_CLK	SCIB_TX			I2CA_SCL		EQEP1_A		XCLKOUT				X2
GPIO19	SPIA_PTE	SCIB_RX			I2CA_SDA		EQEP1_B						X1
GPIO20	EQEP1_A				SPIA_PICO				I2CA_SCL			UARTA_TX	
GPIO21	EQEP1_B				SPIA_POCI				I2CA_SDA			UARTA_RX	
GPIO22	EQEP1_STROBE		SCIB_TX										
GPIO23	EQEP1_INDEX	SPIA_PTE	SCIB_RX										
GPIO24	OUTPUTXBAR1	EQEP1_A	SPIA_PTE		SPIA_PICO				SCIA_TX	ERRORSTS			
GPIO28	SCIA_RX	OUTPUTXBAR8	MCPWM3_1A	OUTPUTXBAR5	EQEP1_A		EQEP1_STROBE	UARTA_TX	SPIA_CLK	ERRORSTS	I2CA_SDA		
GPIO29	SCIA_TX	MCPWM1_2A	MCPWM3_1B	OUTPUTXBAR6	EQEP1_B		EQEP1_INDEX	UARTA_RX	SPIA_PTE	ERRORSTS	I2CA_SCL		
GPIO30				OUTPUTXBAR7	EQEP1_STROBE				MCPWM1_1A				
GPIO32	I2CA_SDA	EQEP1_INDEX	SPIA_CLK		UARTA_RX					ADCSOCBO			
GPIO33	I2CA_SCL			OUTPUTXBAR4	UARTA_TX				EQEP1_B	ADCSOCAO			
GPIO35	SCIA_RX	SPIA_POCI	I2CA_SDA			UARTA_RX	EQEP1_A					TDI	
GPIO37	OUTPUTXBAR2	SPIA_PTE	I2CA_SCL	SCIA_TX		UARTA_TX	EQEP1_B			SYNCOUT		TDO	
GPIO39							EQEP1_INDEX			SYNCOUT	EQEP1_INDEX		
GPIO40				MCPWM1_2B			SCIB_TX	EQEP1_A					
GPIO41	MCPWM3_1A	SPIA_CLK		MCPWM1_2A			SCIB_RX	EQEP1_B					
GPIO43			OUTPUTXBAR6		I2CA_SCL	UARTA_TX		EQEP1_INDEX					
GPIO45			OUTPUTXBAR8		SPIA_POCI								
GPIO46													
GPIO224				OUTPUTXBAR3	SPIA_PICO		MCPWM1_1A		EQEP1_A		UARTA_TX		

Table 5-6. GPIO Muxed Pins (continued)

0, 4, 8, 12	1	2	3	5	6	7	9	10	11	13	14	15	ALT
GPIO226					SPIA_CLK		MCPWM1_1B		EQEP1_STROBE		UARTA_RX		
GPIO227	I2CA_SCL		MCPWM1_3A	OUTPUTXBAR1	MCPWM1_2B								
GPIO228			ADCSOCAO		SPIA_POCI		MCPWM1_2B		EQEP1_B				
GPIO230	I2CA_SDA		MCPWM1_3B		MCPWM1_2A	I2CA_SDA							
GPIO242			MCPWM1_2A	OUTPUTXBAR2	SPIA_PTE				EQEP1_INDEX				
GPIO243	XCLKOUT												
AIO225													
AIO231													
AIO232													
AIO233													
AIO237													
AIO238													
AIO239													
AIO241													
AIO244													
AIO245													

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5.4.2 Digital Inputs on ADC Pins (AIOs)

GPIOs on port H are multiplexed with analog pins. These are also referred to as AIOs. These pins can only function in input mode. By default, these pins will function as analog pins and the GPIOs are in a high-Z state. The GPHAMSEL register is used to configure these pins for digital or analog operation.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AIOs, cross-talk can occur with adjacent analog signals. The user should therefore limit the edge rate of signals connected to AIOs if adjacent channels are being used for analog functions.

5.4.3 Digital Inputs and Outputs on ADC Pins (AGPIOs)

Some GPIOs are multiplexed with analog pins and have digital input and output functionality. These are also referred to as AGPIOs. Unlike AIOs, AGPIOs have full input and output capability. By default, the AGPIOs are not connected and must be configured. Table 5-7 shows how to configure the AGPIOs. To enable the analog functionality, set the register AGPIOCTRLx from analog subsystem. To enable the digital functionality, set the register GPxAMSEL from the *General-Purpose Input/Output (GPIO)* chapter.

Table 5-7. AGPIO Configuration

AGPIOCTRLx.GPIOy (Default = 0)	GPxAMSEL.GPIOy (Default = 1)	Pin Connected To:	
		ADC	GPIOy
0	0	-	Yes
0	**1**	**-** (1)	**-** (1)
1	0	-	Yes
1	1	Yes	-

(1) By default there are no signals connected to AGPIO pins. One of the other rows in the table must be chosen for pin functionality.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AGPIOs, cross-talk can occur with adjacent analog signals. The user must therefore limit the edge rate of signals connected to AGPIOs, if adjacent channels are being used for analog functions.

5.4.4 GPIO Input X-BAR

The Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADCs, eCAPs, MCPWMs, and external interrupts (see Figure 5-4). The *Input X-BAR Destinations* table lists the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *F28E12x Real-Time Microcontrollers Technical Reference Manual*.

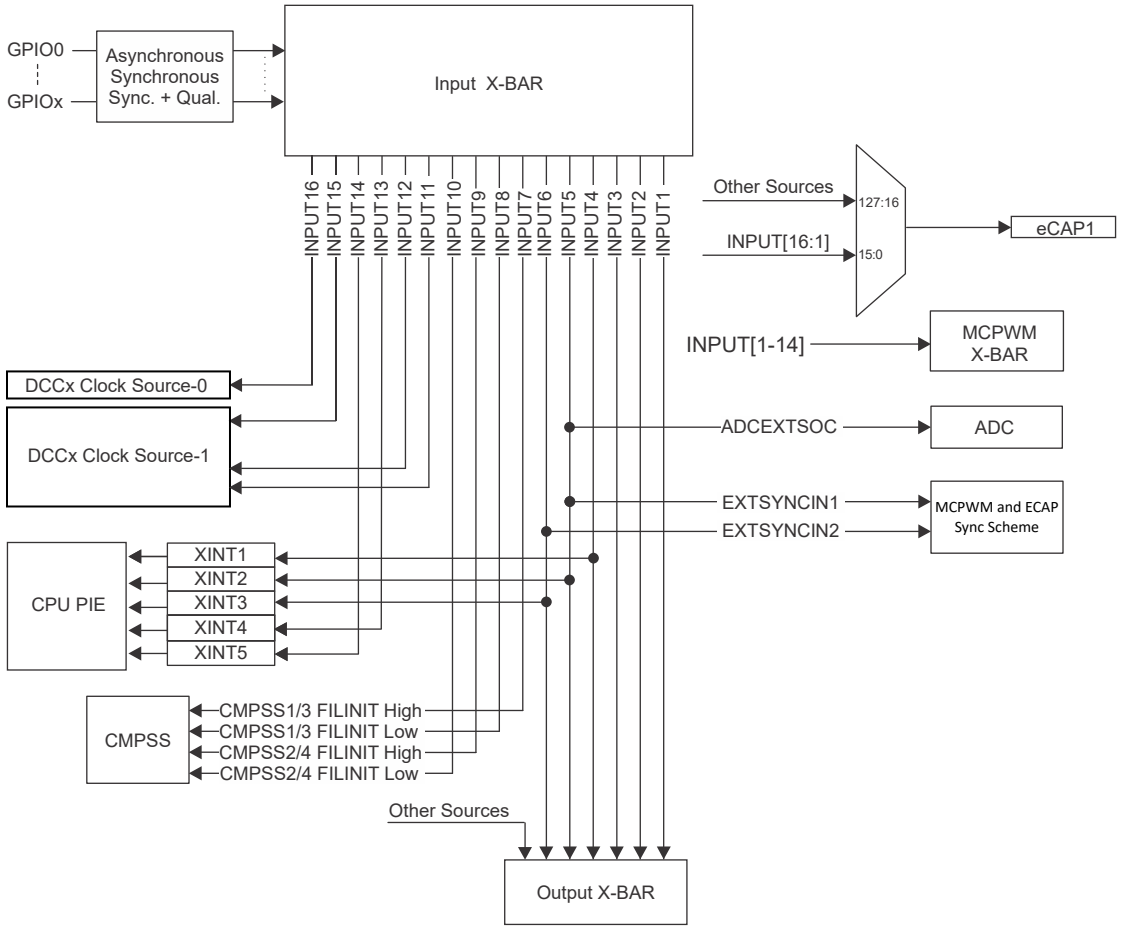

Figure 5-4. Input X-BAR

Table 5-8. Input X-BAR Destinations

INPUT	ECAP	PWM XBAR	OUTPUT XBAR	CPU XINT	ADC START OF CONVERSION	PWM / ECAP SYNC	DCCx	CMPSS
1	Yes	Yes	Yes	-	-	-	-	-
2	Yes	Yes	Yes	-	-	-	-	-
3	Yes	Yes	Yes	-	-	-	-	-
4	Yes	Yes	Yes	XINT1	-	-	-	-
5	Yes	Yes	Yes	XINT2	ADCEXTSOC	EXTSYNCIN1	-	-
6	Yes	Yes	Yes	XINT3	-	EXTSYNCIN2	-	-
7	Yes	Yes	-	-	-	-	-	CMPSS1_EXT_FILTIN_H[1] / CMPSS3_EXT_FILTIN_H[1]
8	Yes	Yes	-	-	-	-	-	CMPSS1_EXT_FILTIN_L[1] / CMPSS3_EXT_FILTIN_L[1]
9	Yes	Yes	-	-	-	-	-	CMPSS2_EXT_FILTIN_H[1] / CMPSS4_EXT_FILTIN_H[1]
10	Yes	Yes	-	-	-	-	-	CMPSS2_EXT_FILTIN_L[1] / CMPSS4_EXT_FILTIN_L[1]
11	Yes	Yes	-	-	-	-	CLK1	-
12	Yes	Yes	-	-	-	-	CLK1	-

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Table 5-8. Input X-BAR Destinations (continued)

INPUT	ECAP	PWM XBAR	OUTPUT XBAR	CPU XINT	ADC START OF CONVERSION	PWM / ECAP SYNC	DCCx	CMPSS
13	Yes	Yes	-	XINT4	-	-	-	-
14	Yes	Yes	-	XINT5	-	-	-	-
15	Yes	-	-	-	-	-	CLK1	-
16	Yes	-	-	-	-	-	CLK0	-

5.4.5 GPIO Output X-BAR and PWM X-BAR

The Output X-BAR has eight outputs that can be selected on the GPIO mux as OUTPUTXBARx. The PWM X-BAR has eight outputs that are connected to the TRIPx inputs of the MCPWM. The sources for the Output X-BAR and PWM X-BAR are shown in Figure 5-5.

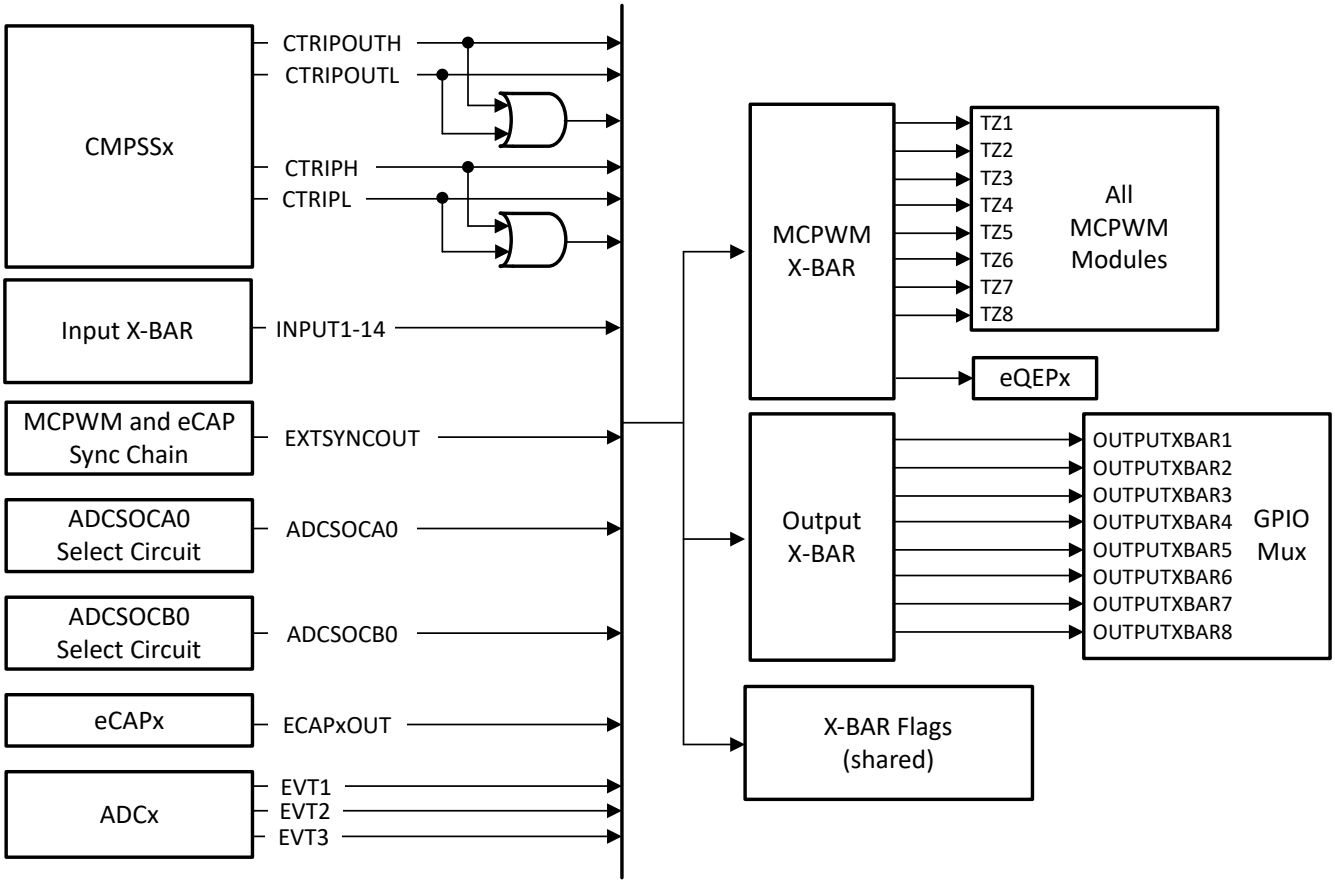

Figure 5-5. GPIO Output X-BAR and PWM X-BAR Sources

5.4.6 GPIO and ADC Allocation

Table 5-9. GPIO and ADC Allocation

FEATURE	48 PT	32 RHB	32 VFC
GPIO			
GPIO	15	11	9
AGPIO	8	5	5
JTAG and Oscillator GPIO	4 (TDI, TDO, X1, X2)		
Total GPIO	27	20	18
AIO	9	6	6
Total GPIO and AIO	36	26	24
ADC			
ADC channels	9	6	6
AGPIO	8	5	5
Total ADC channels (single-ended)	17	11	11

5.5 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. Table 5-10 lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in Table 5-10 with pullups and pulldowns are always on and cannot be disabled.

Table 5-10. Pins With Internal Pullup and Pulldown

PIN	RESET (XRSn = 0)	DEVICE BOOT	APPLICATION
GPIOx	Pullup disabled	Pullup disabled(1)	Application defined
GPIO35/TDI	Pullup disabled		Application defined
GPIO37/TDO	Pullup disabled		Application defined
TCK	Pullup active		
TMS	Pullup active		
XRSn	Pullup active		
Other pins (including AIOs)	No pullup or pulldown present		

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, Table 5-11 lists acceptable conditioning for any unused pins. When multiple options are listed in Table 5-11, any option is acceptable. Pins not listed in Table 5-11 must be connected according to Section 5.

Table 5-11. Connections for Unused Pins

SIGNAL NAME	ACCEPTABLE PRACTICE
ANALOG	
VREFHI	Tie to VDDA (applies only if ADC is not used in the application)
VREFLO	Tie to VSSA
Analog input pins	• No Connect • Tie to VSSA • Tie to VSSA through resistor
Analog input pins (shared with GPIO)	• No Connect • Tie to VSSA through resistor
DIGITAL	
GPIOx	• No connection (input mode with internal pullup enabled) • No connection (output mode with internal pullup disabled) • Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled)
GPIO35/TDI	When TDI mux option is selected (default), the GPIO is in Input mode. • Internal pullup enabled • External pullup resistor
GPIO37/TDO	When TDO mux option is selected (default), the GPIO is in Output mode only during JTAG activity; otherwise, it is in a tri-state condition. The pin must be biased to avoid extra current on the input buffer. • Internal pullup enabled • External pullup resistor
TCK	• No Connect • Pullup resistor
TMS	Pullup resistor
GPIO19/X1	Turn XTAL off and: • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled
GPIO18/X2	Turn XTAL off and: • Input mode with internal pullup enabled • Input mode with external pullup or pulldown resistor • Output mode with internal pullup disabled
POWER AND GROUND	
VDDA	If a dedicated analog supply is not used, tie to VDDIO.
VDDIO	All VDDIO pins must be connected per Section 5.3.
VSS	All VSS pins must be connected to board ground.
VSSA	If an analog ground is not used, tie to VSS.

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6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating conditions (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDDIO with respect to VSS	–0.3	4.6	V
	VDDA with respect to VSSA	–0.3	4.6	
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital/analog input (per pin), I_{IK} (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/VDDA)(4)	–20	20	mA
	Total for all inputs, $I_{IKTOTAL}$ (V_{IN} < VSS/VSSA or V_{IN} > VDDIO/VDDA)	–20	20	
Output current	Digital output (per pin), I_{OUT}	–20	20	mA
Operating junction temperature	T_J	–40	125	°C
Storage temperature(3)	T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSS, unless otherwise noted.
(3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(4) Continuous clamp current per pin is ±2 mA. Do not operate in this condition continuously as V_{DDIO}/V_{DDA} voltage may internally rise and impact other electrical specifications.

6.2 ESD Ratings

				VALUE	UNIT
F28E120SC, F28E120SB in 48-pin PT package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 48-pin PT: 1, 12, 13, 24, 25, 36, 37, 48	±750	
F28E120SC, F28E120SB in 32-pin VFC package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 32-pin VFC: 1, 8, 9, 16, 17, 24, 25, 32	±750	
F28E120SC, F28E120SB in 32-pin RHB package					
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	
			Corner pins on 32-pin RHB: 1, 8, 9, 16, 17, 24, 25, 32	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, VDDIO and VDDA	Internal BOR enabled(3)	$V_{BOR-VDDIO}$(MAX) + V_{BOR-GB} (2)	3.3	3.63	V
	Internal BOR disabled	2.8	3.3	3.63	
Device ground, VSS			0		V
Analog ground, VSSA			0		V
SR_{SUPPLY}	Supply ramp rate of VDDIO, VDD, VDDA with respect to VSS.(4)				
V_{IN}	Digital input voltage	VSS – 0.3		VDDIO + 0.3	V
	Analog input voltage	VSSA – 0.3		VDDA + 0.3	V
Junction temperature, T_J (1)		–40		125	°C
Free-Air temperature, T_A		–40		105	°C

(1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See *Calculating Useful Lifetimes of Embedded Processors* for more information.
(2) See the *Power Management Module (PMM)* section.
(3) Internal BOR is enabled by default.
(4) See the Power Management Module Operating Conditions table.

ADVANCE INFORMATION

6.4 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations. Section 6.4.1 lists the system current consumption values.

6.4.1 System Current Consumption - Internal Supply

Over recommended operating conditions (unless otherwise noted)
TYP : V_{nom}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPERATING MODE							
I_{DDIO} (3)	VDDIO current consumption during operational usage	This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low	30 ℃		32		mA
			85 ℃			TBD	mA
			125 ℃			TBD	mA
I_{DDA}	VDDA current consumption during operational usage		30 ℃		2.5		mA
			85 ℃			TBD	mA
			105 ℃			TBD	mA
IDLE MODE							
I_{DDIO}	VDDIO current consumption while device is in Idle mode	- CPU is in IDLE mode - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		TBD		mA
			85 ℃			TBD	mA
			125 ℃			27	mA
I_{DDA}	VDDA current consumption while device is in Idle mode		30 ℃		0.01		mA
			85 ℃			TBD	mA
			125 ℃			TBD	mA
STANDBY MODE (PLL Enabled)							
I_{DDIO}	VDDIO current consumption while device is in Standby mode	- CPU is in STANDBY mode - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		TBD		mA
			85 ℃			TBD	mA
			125 ℃			TBD	mA
I_{DDA}	VDDA current consumption while device is in Standby mode		30 ℃		TBD		mA
			85 ℃			TBD	mA
			125 ℃			0.1	mA

6.4.1 System Current Consumption - Internal Supply (continued)

Over recommended operating conditions (unless otherwise noted)
TYP : V_{nom}

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STANDBY MODE (PLL Disabled)							
I_{DDIO}	VDDIO current consumption while device is in Standby mode	- CPU is in STANDBY mode - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		TBD		mA
			85 ℃			TBD	mA
			125 ℃			TBD	mA
I_{DDA}	VDDA current consumption while device is in Standby mode		30 ℃		TBD		mA
			85 ℃			TBD	mA
			125 ℃			TBD	mA
HALT MODE							
I_{DDIO}	VDDIO current consumption while device is in Halt mode	- CPU is in HALT mode - PLL is Disabled, SYSCLK and CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low	30 ℃		TBD		mA
			85 ℃			TBD	mA
			125 ℃			TBD	mA
I_{DDA}	VDDA current consumption while device is in Halt mode		30 ℃		TBD		mA
			85 ℃			TBD	mA
			125 ℃			TBD	mA
FLASH ERASE/PROGRAM							
I_{DDIO}	VDDIO current consumption during Erase/Program cycle(1)	- CPU is running from RAM - Flash going through continuous Program/Erase operation - PLL is enabled, SYSCLK at 120 MHz. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low			TBD	TBD	mA
I_{DDA}	VDDA current consumption during Erase/Program cycle				TBD	TBD	mA
RESET MODE							
I_{DDIO}	VDDIO current consumption while reset is active(2)	Device is under Reset	30 ℃		8		mA
			85 ℃		TBD		mA
			125 ℃		TBD		mA
I_{DDA}	VDDA current consumption while reset is active(2)		30 ℃		0.01		mA
			85 ℃		TBD		mA
			125 ℃		TBD		mA

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
(2) This is the current consumption while reset is active (that is, XRSn is low).
(3) *While this value represents the peak current draw under the listed operating conditions, please refer to the VREG In-rush current specification in the Power Management Module Characteristics section for the max current budget needed for proper operation of the device*

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6.4.2 Operating Mode Test Description

Section 6.4.1 lists the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- All CPUs are actively executing code.
- All analog peripherals are powered up. ADC is periodically converting.

6.4.3 Current Consumption Graphs

The below graphs show a typical representation of the relationship between frequency, temperature, supply, and current consumption on the device. Actual results vary based on the system implementation and conditions.

Figure 6-1 shows the typical operating current profile across temperature and operating mode for internal supply, with data based on the *System Current Consumption - VREG Enable - Internal Supply* table (30 °C data is taken at VNOM with higher temperature data points taken at VMAX).

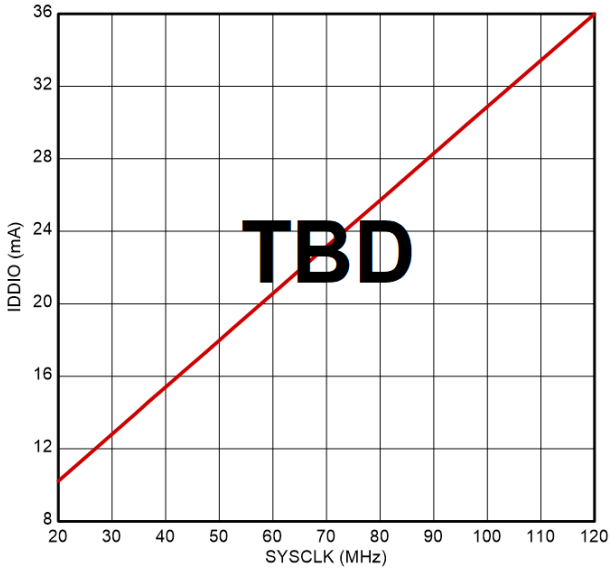

Figure 6-1. Operating Current Versus Frequency

6.4.4 Reducing Current Consumption

The F28E12x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the *F28E12x Real-Time Microcontrollers Technical Reference Manual* to ensure each module is powered down as well.

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6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital and Analog IO							
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MIN	VDDIO * 0.8			V
			I_{OH} = –100 µA	VDDIO – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX			0.4	V
			I_{OL} = 100 µA			0.2	
I_{OH}	High-level output source current for all output pins			–4			mA
I_{OL}	Low-level output sink current for all output pins					4	mA
R_{OH}	High-level output impedance for all output pins		VOH=VDDS-0.4V	50	65	96	Ω
R_{OL}	Low-level output impedance for all output pins		VOL=0.4V	48	60	84	Ω
V_{IH}	High-level input voltage			2.0			V
V_{IL}	Low-level input voltage					0.8	V
$V_{HYSTERESIS}$	Input hysteresis (AIO)			125			mV
	Input hysteresis (GPIO)			125			
$I_{PULLDOWN}$	Input current	Pins with pulldown	VDDIO = 3.3 V V_{IN} = VDDIO		120		µA
I_{PULLUP}	Input current	Digital inputs with pullup enabled(1)	VDDIO = 3.3 V V_{IN} = 0 V		160		µA
$R_{PULLDOWN}$	Weak pulldown resistance			22.66	31.49	61.55	kΩ
R_{PULLUP}	Weak pullup resistance			19.89	29.45	53.63	kΩ
I_{LEAK}	Pin leakage	Digital inputs	Pullups and outputs disabled 0 V ≤ V_{IN} ≤ VDDIO			0.1	µA
		Analog pins	Analog drivers disabled 0 V ≤ V_{IN} ≤ VDDA			0.1	
C_I	Input capacitance	Digital inputs			2		pF
		Analog pins(2)					
BOR							
POR, BOR(3)							

(1) See Pins With Internal Pullup and Pulldown table for a list of pins with a pullup or pulldown.
(2) The analog pins are specified separately; see the Per-Channel Parasitic Capacitance tables that are in the ADC Input Model section.
(3) See the *Power Management Module (PMM)* section.

6.6 Thermal Resistance Characteristics for PT Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance	22.9
$R\Theta_{JB}$	Junction-to-board thermal resistance	36.8
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	61.8
Psi_{JT}	Junction-to-package top	1.2
Psi_{JB}	Junction-to-board	36.5

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.7 Thermal Resistance Characteristics for VFC Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	23.2
$R\Theta_{JB}$	Junction-to-board thermal resistance	37.0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	63.7
Psi_{JT}	Junction-to-package top	1.3
Psi_{JB}	Junction-to-board	36.5

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.8 Thermal Resistance Characteristics for RHB Package

		°C/W(1)
$R\Theta_{JC}$	Junction-to-case thermal resistance, top	25.2
	Junction-to-case thermal resistance, bottom	4.1
$R\Theta_{JB}$	Junction-to-board thermal resistance	14.0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	33.1
Psi_{JT}	Junction-to-package top	0.4
Psi_{JB}	Junction-to-board	13.9

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

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6.9 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

6.10 System

6.10.1 Power Management Module (PMM)

6.10.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.10.1.2 Overview

The block diagram of the PMM is shown in Figure 6-2. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

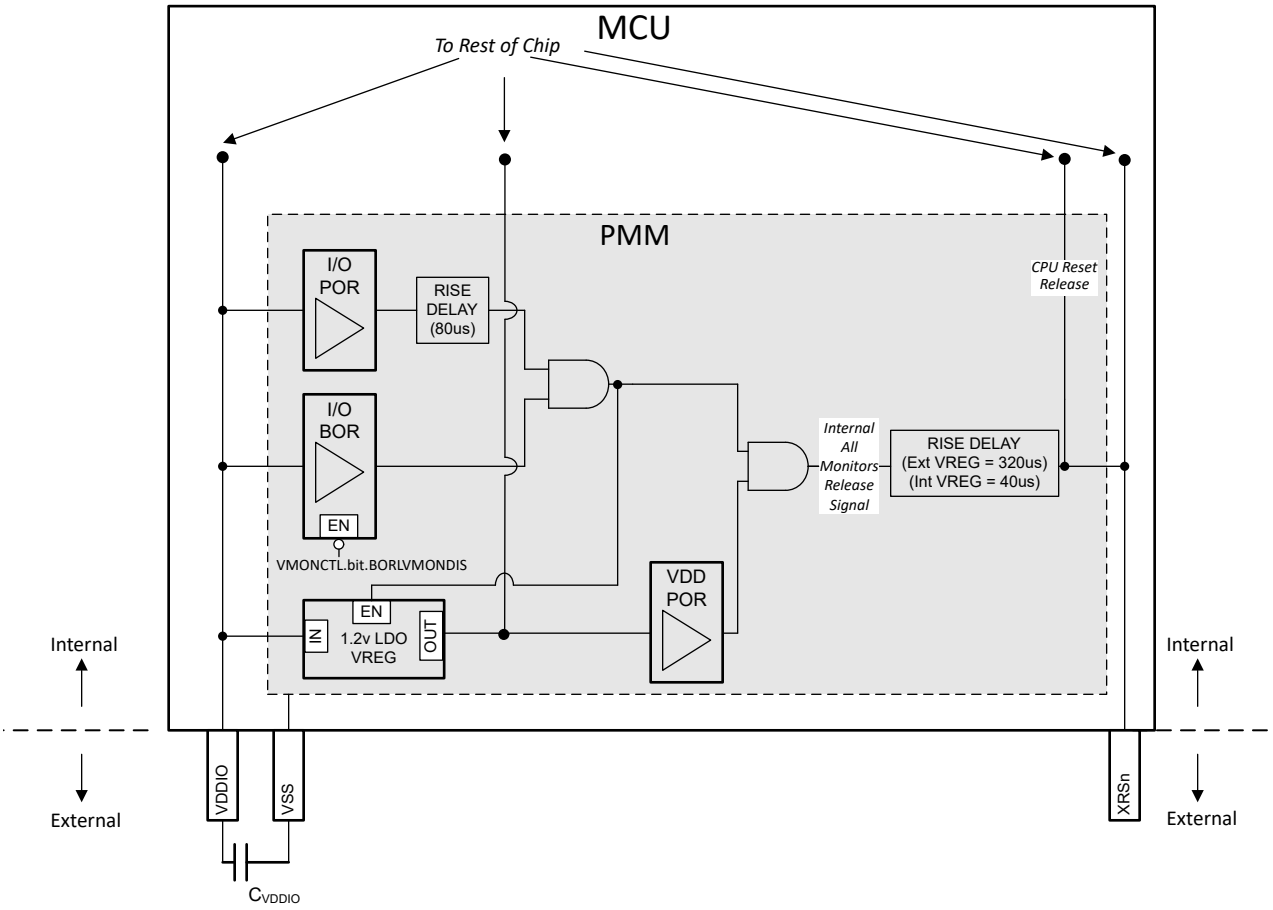

Figure 6-2. PMM Block Diagram

6.10.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

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6.10.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

6.10.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Figure 6-3 shows the operating region of the I/O BOR.

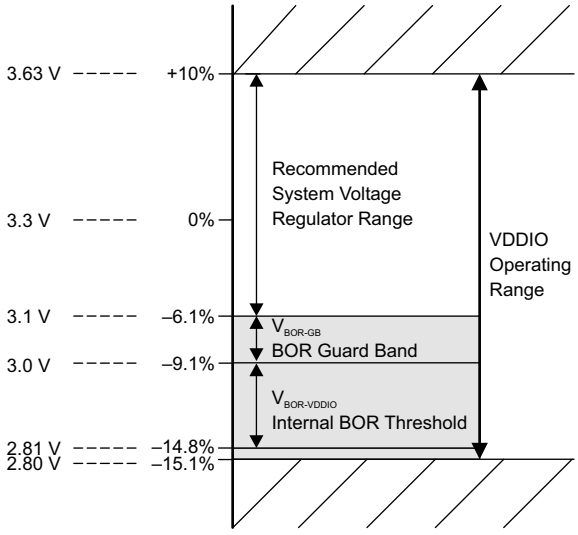

Figure 6-3. I/O BOR Operating Region

6.10.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.10.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR feature can be used for I/O rail monitoring as long as it meets the application requirement.

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.

Note

The use of an external supervisor with the internal VREG is not supported.

6.10.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. This is to ensure that the voltages are stable when XRSn releases. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in Power Management Module Electrical Data and Timing for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.10.1.2.4 Internal VDD LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the required output to power the VDD.

6.10.1.3 External Components

6.10.1.3.1 Decoupling Capacitors

VDDIO requiresdecoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.10.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in Power Management Module Electrical Data and Timing. The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of C_{VDDIO} * VDDIO pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.10.1.4 Power Sequencing

6.10.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally.

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6.10.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI). This sequencing is still required even if VDDIO and VDDA are not tied together.

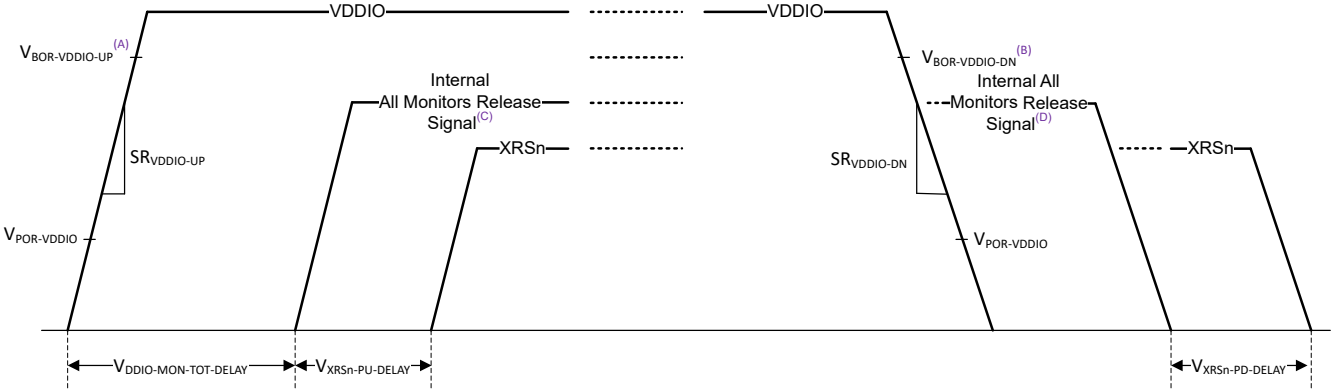
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

6.10.1.4.3 Supply Pins Power Sequence

6.10.1.4.3.1 Internal VREG/VDD Mode Sequence

Figure 6-4 depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in Power Management Module Electrical Data and Timing.



A. This trip point is the trip point before XRSn releases. See the *Power Management Module Characteristics* table.
B. This trip point is the trip point after XRSn releases. See the *Power Management Module Characteristics* table.
C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the *PMM Block Diagram*.
D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the *PMM Block Diagram*.

Figure 6-4. Internal VREG Power Up Sequence

- **For Power Up:**
  1. VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
  2. The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
  3. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PU-DELAY}$, XRSn will be released and the device starts the boot-up sequence.
  4. The I/O BOR monitor has different release points during power up and power down.
- **For Power Down:**
  1. The only requirement on VDDIO during power down is the slew rate.
  2. The I/O BOR monitor has different release points during power up and power down.
  3. The I/O BOR tripping will cause XRSn to go low after $V_{XRSN-PD-DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.10.1.4.3.2 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION

Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in Supply Pins Power Sequence is recommended.

Table 6-1. Internal VREG Sequence Summary

CASE	RAILS POWER-UP ORDER		ACCEPTABLE
	VDDIO	VDDA	
A	1	2	Yes
B	2	1	No
C	1	1	Yes

Note

The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.10.1.4.3.3 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note

The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

6.10.1.5 Recommended Operating Conditions Applicability to the PMM

As noted in the *Recommended Operating Conditions* table, the voltage (V_{IN}) of all pins on the device should be kept above VSS – 0.3 V. Negative voltages below this value will inject current into the device, which could cause abnormal operation. Specific care should be taken for pins near the PMM. A negative voltage on these pins can cause the POR or BOR blocks to unexpectedly assert XRSn or disable the internal VREG (see the *PMM Block Diagram*). Pins near the PMM on this device are shown in the *Pins Near PMM* table below.

Table 6-2. Pins Near PMM

PIN NAME	PIN NUMBER		
	48 PT	32 VFC	32 RHB
A0/AIO231	11	7	7

Methods to avoid negative noise on pins include (in order of importance):

1. Reduce or eliminate noise at the source.
2. Avoid coupling between noise sources on these pins.
3. Filters near the device pin to isolate any noise.

ADVANCE INFORMATION

6.10.1.6 Power Management Module Electrical Data and Timing

6.10.1.6.1 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
C_{VDDIO} (1) (2)	VDDIO Capacitance Per Pin(5)		0.1			uF
C_{VDDA} (1) (2)	VDDA Capacitance Per Pin(5)		2.2			uF
SR_{VDD33} (3)	Supply Ramp Rate of 3.3V Rails (VDDIO, VDDA)		20		100	mV/us
$V_{BOR-VDDIO-GB}$ (4)	VDDIO Brown Out Reset Voltage Guardband			0.1		V

(1) A bulk capacitor should also be used. The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
(2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
(3) See the *Supply Slew Rate* section. Supply ramp rate faster than the maximum can trigger the on-chip ESD protection.
(4) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR-VDDIO-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
(5) Max capacitor tolerance should be 20%.

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6.10.1.6.2 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VREG}	Internal Voltage Regulator Output		1.152	1.2	1.248	V
$V_{VREG-PU}$	Internal Voltage Regulator Power Up Time				350	us
$V_{VREG-INRUSH}$ (4)	Internal Voltage Regulator Inrush Current			80		mA
$V_{POR-VDDIO}$	VDDIO Power on Reset Voltage	Before and After XRSn Release		2.3		V
$V_{BOR-VDDIO-UP}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Up	Before XRSn Release		2.7		V
$V_{BOR-VDDIO-DOWN}$ (1)	VDDIO Brown Out Reset Voltage on Ramp Down	After XRSn Release	2.81		3.0	V
$V_{XRSn-PU-DELAY}$ (2)	XRSn Release Delay after Supplies are Ramped Up During Power-Up			40		us
$V_{XRSn-PD-DELAY}$ (3)	XRSn Trip Delay after Supplies are Ramped Down During Power-Down			2		us
$V_{DDIO-MON-TOT-DELAY}$	Total Delays in Path of VDDIO Monitors (POR, BOR)			80		us
$V_{XRSn-MON-RELEASE-DELAY}$	XRSn Release Delay after a VDD POR Event	Supplies Within Operating Range		40		us
	XRSn Release Delay after a VDDIO BOR Event			40		us
	XRSn Release Delay after a VDDIO POR Event			120		us

(1) See the *I/O BOR Operating Region* figure.
(2) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect. RC network delay will add to this.
(3) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply. RC network delay will add to this.
(4) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

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6.10.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR) and brown-out reset (BOR) monitors. During power up, the monitor circuits keep the XRSn pin low. For more details, see the *Power Management Module (PMM)* section. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-5 shows the recommended reset circuit.

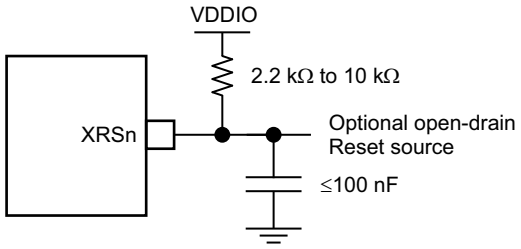


Figure 6-5. Reset Circuit

6.10.2.1 Reset Sources

The *Reset Signals* table summarizes the various reset signals and their effect on the device.

Table 6-3. Reset Signals

Reset Source	CPU Core Reset (C28x, FPU,)	Peripherals Reset	JTAG / Debug Logic Reset	IOs	$\overline{\text{XRS}}$ Output
POR	Yes	Yes	Yes	Hi-Z	Yes
BOR	Yes	Yes	Yes	Hi-Z	Yes
$\overline{\text{XRS}}$ Pin	Yes	Yes	No	Hi-Z	-
$\overline{\text{WDRS}}$	Yes	Yes	No	Hi-Z	Yes
$\overline{\text{NMIWDRS}}$	Yes	Yes	No	Hi-Z	Yes
$\overline{\text{SYSRS}}$ (Debugger Reset)	Yes	Yes	No	Hi-Z	No
$\overline{\text{SCCRESET}}$	Yes	Yes	No	Hi-Z	No
SIMRESET. $\overline{\text{XRS}}$	Yes	Yes	No	Hi-Z	Yes
SIMRESET. $\overline{\text{CPU1RS}}$	Yes	Yes	No	Hi-Z	No

The parameter $t_{h(boot\text{-}mode)}$ must account for a reset initiated from any of these sources.

See the *Resets* section of the System Control chapter in the *F28E12x Real-Time Microcontrollers Technical Reference Manual*.

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP.

6.10.2.2 Reset Electrical Data and Timing

6.10.2.2.1 Reset - XRSn - Timing Requirements

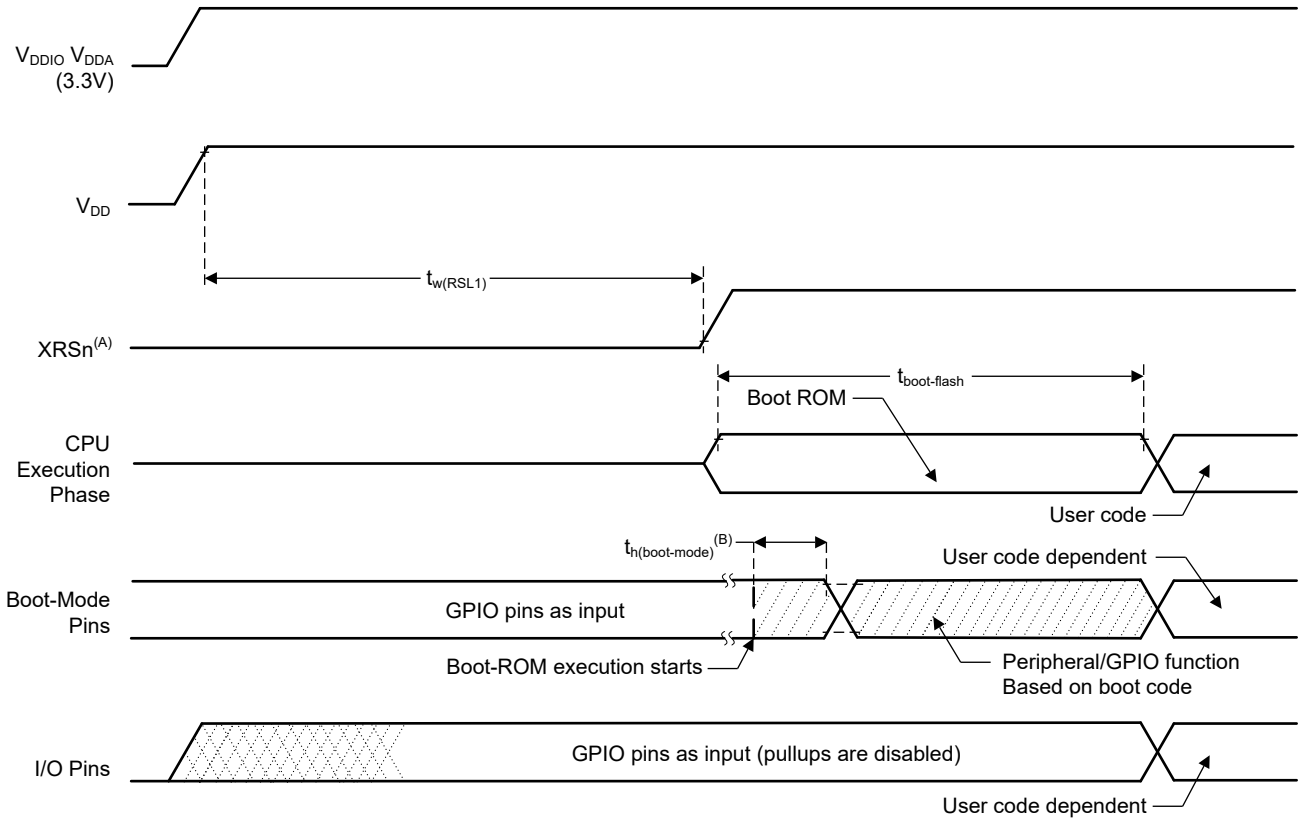
		MIN	MAX	UNIT
$t_{h(boot-mode)}$	Hold time for boot-mode pins	1.5		ms
$t_{w(RSL2)}$	Pulse duration, XRSn low on warm reset	3.2		µs

6.10.2.2.2 Reset - XRSn - Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, XRSn driven low by device after supplies are stable		100		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{boot-flash}$	Boot-ROM execution time to first instruction fetch in flash			1.2	ms

6.10.2.2.3 Reset Timing Diagrams

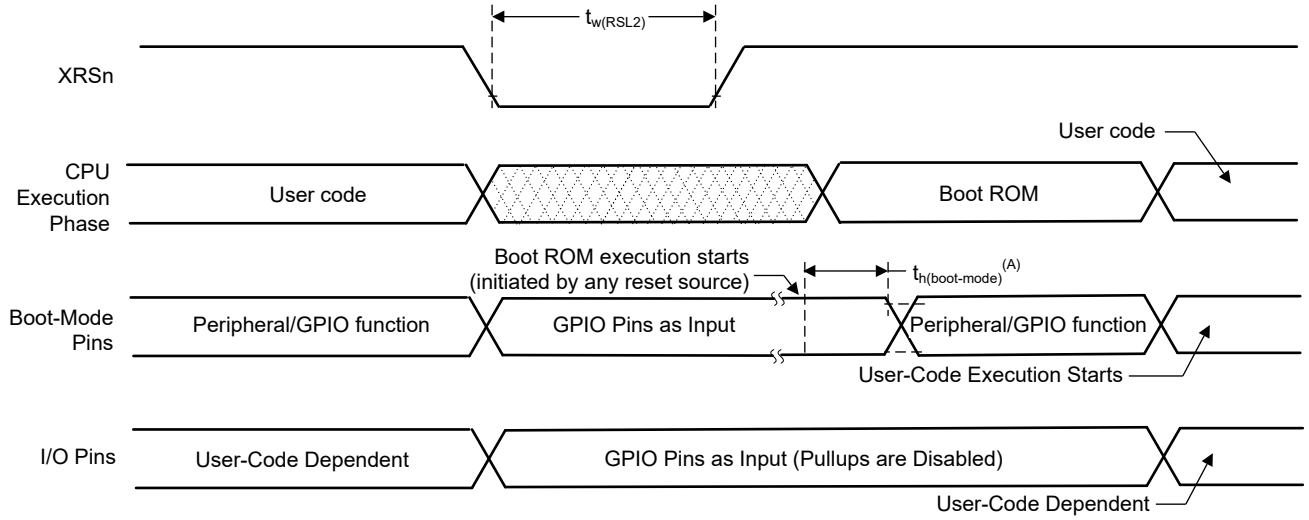


A. The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the *Pin Attributes* table. On-chip monitors will hold this pin low until the supplies are in a valid range.

B. After reset from any source (see the *Reset Sources* section), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-6. Power-on Reset

ADVANCE INFORMATION



A. After reset from any source (see the *Reset Sources* section), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-7. Warm Reset

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6.10.3 Clock Specifications

6.10.3.1 Clock Sources

This section explains the clock sources and clock domains on this device, and how to configure them for application use. The clock sources are given in Table 6-4. Figure 6-8 and Figure 6-9 provide an overview of the device's clocking system. The relation between PLLRAWCLK and OSCCLK is given in Equation 1.

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK} \times (\text{QDIV})}{(\text{PDIV}) \times (\text{RDIVCLK0})} \quad (1)$$

Table 6-4. Possible Reference Clock Sources

CLOCK SOURCE	DESCRIPTION
WROSC	Internal 20MHz to 70MHz oscillator
SYSOSC(1)	Internal 4MHz to 32MHz oscillator
X1 (XTAL)	External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin.

(1) On reset, SYSOSC is the default clock source for the PLL (OSCCLK).

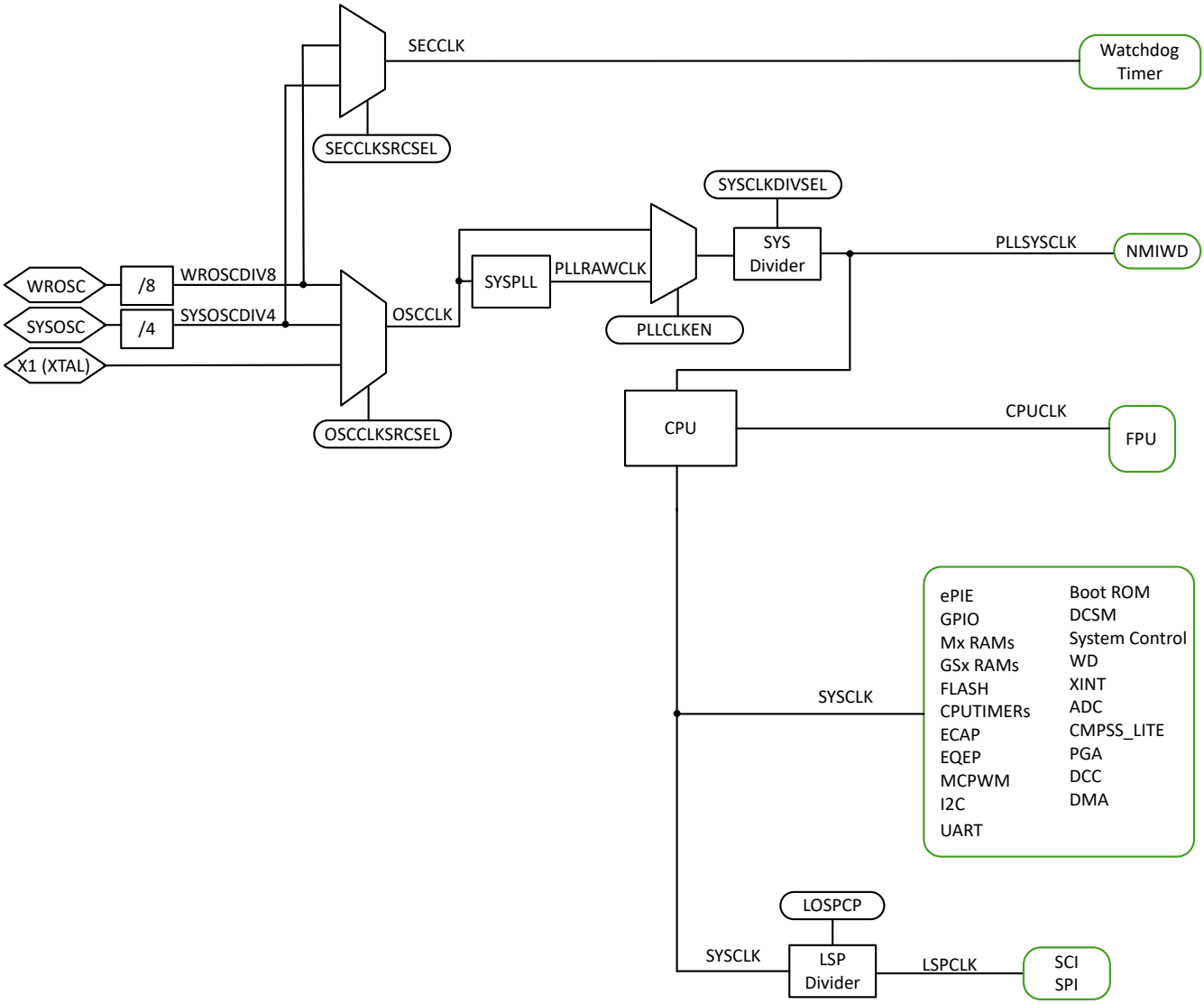

Figure 6-8. Clocking System

ADVANCE INFORMATION

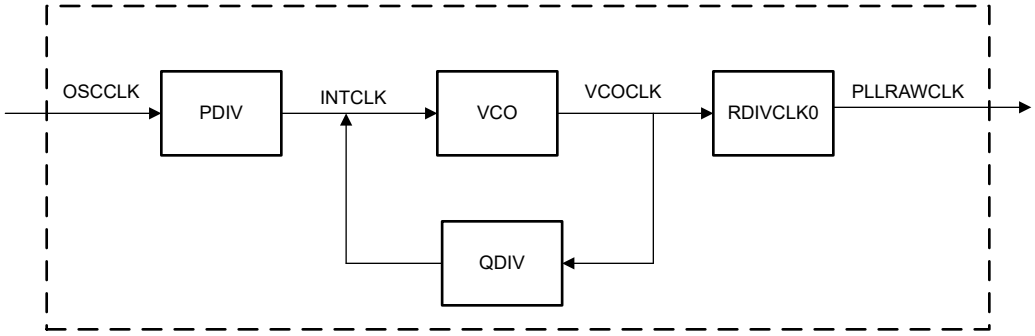

Figure 6-9. System PLL

6.10.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.10.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

6.10.3.2.1.1 Input Clock Frequency

		MIN	MAX	UNIT
$f_{(XTAL)}$	Frequency, X1/X2, from external crystal or resonator	10	20	MHz
$f_{(X1)}$	Frequency, X1, from external oscillator	10	25	MHz

6.10.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
X1 V_{IL}	Valid low-level input voltage	–0.3		0.3 * VDDIO	V
X1 V_{IH}	Valid high-level input voltage	0.7 * VDDIO		VDDIO + 0.3	V

6.10.3.2.1.3 X1 Timing Requirements

		MIN	MAX	UNIT
$t_{f(X1)}$	Fall time, X1		6	ns
$t_{r(X1)}$	Rise time, X1		6	ns
$t_{w(X1L)}$	Pulse duration, X1 low as a percentage of $t_{c(X1)}$	45%	55%	
$t_{w(X1H)}$	Pulse duration, X1 high as a percentage of $t_{c(X1)}$	45%	55%	

6.10.3.2.1.4 PLL Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
PLL Lock time				
SYS PLL Lock Time(1)		15		us

(1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

6.10.3.2.1.5 XCLKOUT Switching Characteristics - PLL Bypassed or Enabled

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		MIN	MAX	UNIT
$t_{f(XCO)}$	Fall time, XCLKOUT		6	ns
$t_{r(XCO)}$	Rise time, XCLKOUT		6	ns
$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2(2)	H + 2(2)	ns
$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2(2)	H + 2(2)	ns
$f_{(XCO)}$	Frequency, XCLKOUT		50	MHz

(1) A load of 6 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$

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6.10.3.2.1.6 Internal Clock Frequencies

		MIN	NOM	MAX	UNIT
$f_{(SYSCLK)}$	Frequency, device (system) clock	2		160	MHz
$t_{c(SYSCLK)}$	Period, device (system) clock	6.25		500	ns
$f_{(INTCLK)}$	Frequency, system PLL going into VCO (after PDIV)	2		20	MHz
$f_{(VCOCLK)}$	Frequency, system PLL VCO (before ODIV)	220		600	MHz
$f_{(PLLRAWCLK)}$	Frequency, system PLL output (before SYSCLK divider)	6		240	MHz
$f_{(PLL)}$	Frequency, PLLSYSCLK	2		160	MHz
$f_{(PLL\_LIMP)}$	Frequency, PLL Limp Frequency (1)		45/(ODIV+1)		MHz
$f_{(LSP)}$	Frequency, LSPCLK	2		160	MHz
$t_{c(LSPCLK)}$	Period, LSPCLK	8.33		500	ns
$f_{(OSCCLK)}$	Frequency, OSCCLK (WROSCDIV8 or SYSOSCDIV4 or XTAL or X1)		See respective clock		MHz
$f_{(MCPWM)}$	Frequency, MCPWMCLK			160	MHz

(1) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp).

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6.10.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, three types of external clock sources are supported:

- A single-ended 3.3-V external clock. The clock signal should be connected to X1, as shown in Figure 6-10, with the XTALCR.SE bit set to 1.
- An external crystal. The crystal should be connected across X1 and X2 with its load capacitors connected to VSS as shown in Figure 6-11.
- An external resonator. The resonator should be connected across X1 and X2 with its ground connected to VSS as shown in Figure 6-12.

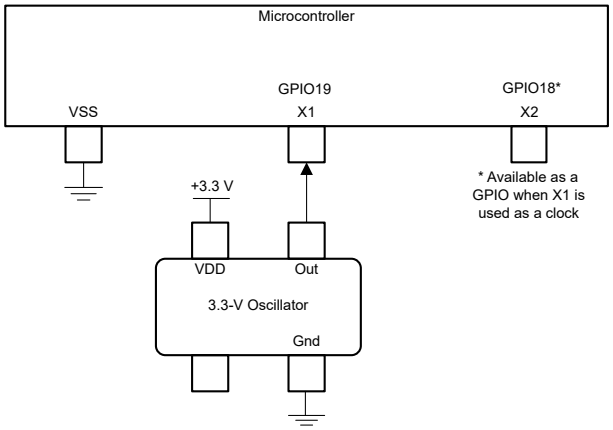

Figure 6-10. Single-ended 3.3-V External Clock

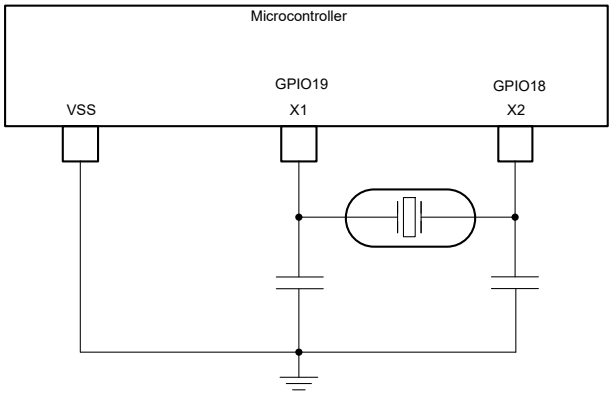

Figure 6-11. External Crystal

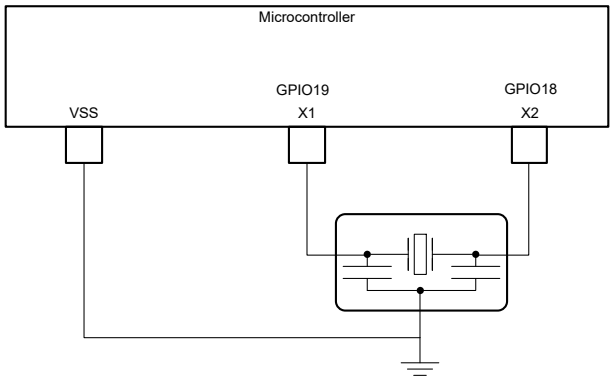

Figure 6-12. External Resonator

6.10.3.4 XTAL Oscillator

6.10.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.10.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.10.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). Figure 6-13 illustrates the components of the electrical oscillator and the tank circuit.

ADVANCE INFORMATION

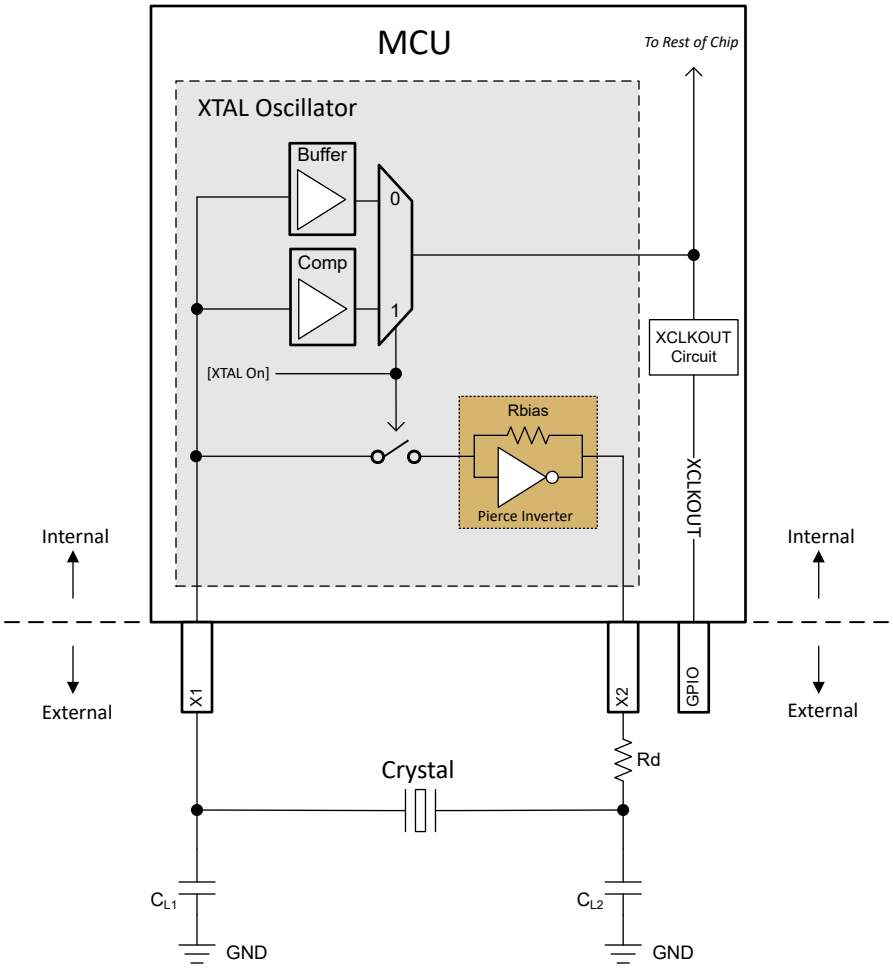

Figure 6-13. Electrical Oscillator Block Diagram

6.10.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.10.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when [XTAL On] = 1, which is achieved by setting XTALCR.OSCOFF = 0 and XTALCR.SE = 0. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal Rbias, moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the VIH and VIL of the comparator. See the *XTAL Oscillator Characteristics* table for the VIH and VIL requirements of the comparator.

6.10.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

This mode is enabled when [XTAL On] = 0, which can be achieved by setting XTALCR.OSCOFF = 1 and XTALCR.SE = 1.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.10.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the *GPIO Muxed Pins* table for a list of GPIOs that XCLKOUT comes out on.

6.10.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in Figure 6-14 and explained below.

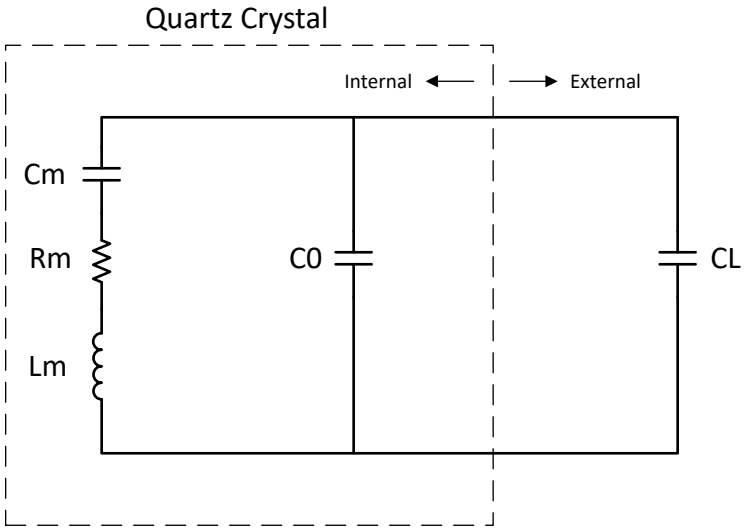

Figure 6-14. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From Figure 6-13, CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to [CL1]/2 if CL1 = CL2.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.10.3.4.3 Functional Operation

6.10.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = Rm * \left(1 + \frac{C0}{CL}\right)^2 \quad (2)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.10.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

Figure 6-15 and Figure 6-16 show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to Table 6-5 for minimum and maximum values for design considerations.

6.10.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the *Rneg – Negative Resistance* section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to the *Crystal Oscillator Specifications* section for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.10.3.4.3.3.1 X1/X2 Precondition

On this device, the GPIO19/18 alternate functionality on X1/X2 can be used to speed up the start-up time of the crystal if needed. This functionality is achieved by preconditioning the load capacitors CL1 and CL2 to a known state before the XTAL is turned on. See the for details.

6.10.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (Rd) should be installed to limit the current and reduce the power dissipated by the crystal. Note that Rd reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.10.3.4.4 How to Choose a Crystal

Using Crystal Oscillator Specifications as a reference:

1. Pick a crystal frequency (for example, 20 MHz).
2. Check that the ESR of the crystal <=50 Ω per specifications for 20 MHz.
3. Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
   - As mentioned, CL1 and CL2 are in series; so, provided CL1 = CL2, effective load capacitance CL = [CL1]/2.
   - Adding board parasitics to this results in CL = [CL1]/2 + Cstray
4. Check that the maximum drive level of the crystal >= 1 mW. If this requirement is not met, a dampening resistor Rd can be used. Refer to DL – Drive Level on other points to consider when using Rd.

6.10.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

1. Bring out the XTAL on XCLKOUT.
2. Measure this frequency as the crystal frequency.

Negative Resistance

1. Bring out the XTAL on XCLKOUT.
2. Place a potentiometer in series with the crystal between the load capacitors.
3. Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
4. This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

1. Turn off the XTAL.
2. Bring out the XTAL on XCLKOUT.
3. Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.10.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the *How to Choose a Crystal* section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor Rd is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

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6.10.3.4.7 Crystal Oscillator Specifications

6.10.3.4.7.1 Crystal Oscillator Parameters

		MIN	MAX	UNIT
CL1, CL2	Load capacitance	12	24	pF
C0	Crystal shunt capacitance		7	pF

6.10.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the Crystal Equivalent Series Resistance (ESR) Requirements table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. ESR = Negative Resistance/3

Table 6-5. Crystal Equivalent Series Resistance (ESR) Requirements

CRYSTAL FREQUENCY (MHz)	MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF)	MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF)
10	55	110
12	50	95
14	50	90
16	45	75
18	45	65
20	45	50

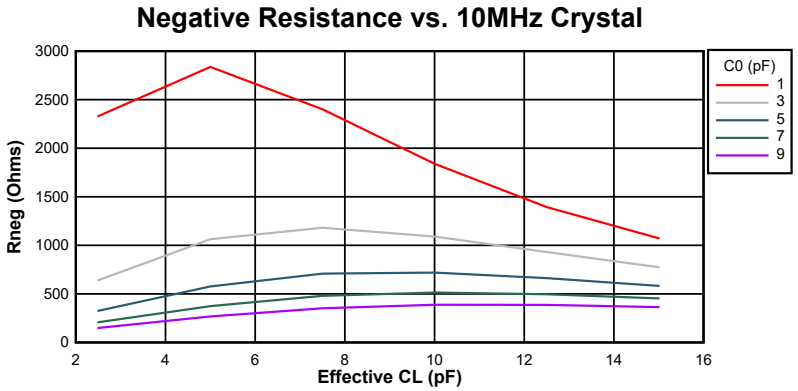

Figure 6-15. Negative Resistance Variation at 10 MHz

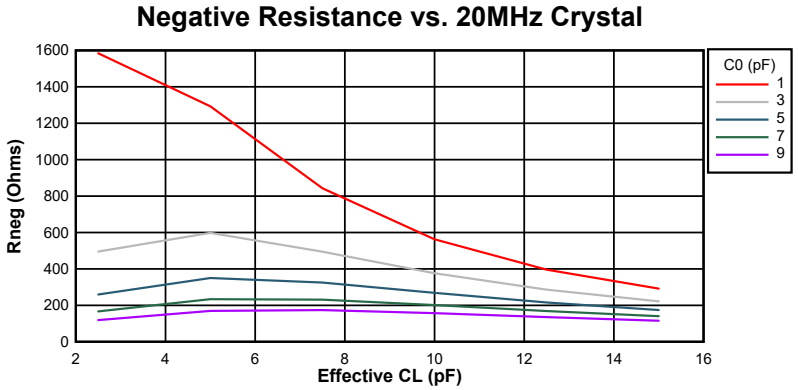

Figure 6-16. Negative Resistance Variation at 20 MHz

ADVANCE INFORMATION

6.10.3.4.7.3 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time(1)	f = 10 MHz	ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF		4		ms
	f = 20 MHz	ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF		2		ms
Crystal drive level (DL)					1	mW

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

ADVANCE INFORMATION

6.10.3.5 Internal Oscillators

To reduce production board costs and application development time, all devices contain two independent internal oscillators, referred to as SYSOSC and WROSC. By default, SYSOSC is set as the source for the system reference clock (OSCCLK) and WROSC is set as the backup clock source.

Applications requiring tighter **SCI baud rate matching** can use the SCI baud tuning example (baud_tune_via_uart) available in C2000Ware.

6.10.3.5.1 System Oscillator SYSOSC

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SYSOSC}	Factory trimmed SYSOSC frequency	SYSOSCCFG.FREQ=00 (BASE)		32.2		MHz
f_{SYSOSC}	SYSOSC frequency accuracy when frequency correction loop (FCL) is enabled when the internal ROSC resistor is used (1)	SETUSEFCL=1, T_a = 25 ℃	TBD		TBD	%
		SETUSEFCL=1, 0 ℃ < T_a < 85 ℃	TBD		TBD	
		SETUSEFCL=1 -40 ℃ < T_a < 125 ℃	TBD		TBD	
f_{SYSOSC}	SYSOSC accuracy when frequency correction loop (FCL) is disabled, 24MHz	SETUSEFCL=0, SYSOSCCFG.FREQ=00, -40 ℃ < T_a < 125 ℃	TBD		TBD	%
$t_{settle, SYSOSC}$	Settling time to target accuracy (2)	SETUSEFCL=1			TBD	us

(1) The SYSOSC frequency correction loop (FCL) enables high SYSOSC accuracy via an internal reference resistor when using the FCL. See the SYSOSC section of the technical reference manual for details on computing SYSOSC accuracy.

(2) When SYSOSC is enabled from a disabled state, the SYSOSC output will be released to the device within the time specified by $t_{start, SYSOSC}$. Once the output is released, the SYSOSC worst-case accuracy is specified by f_{settle}, SYSOSC. After the time specified by $t_{settle, SYSSOSC}$, the SYSOSC will have settled to the target f_{SYSOSC} accuracy.

6.10.4 Flash Parameters

Table 6-6 lists the minimum required Flash wait states with different clock sources and frequencies. Wait state is the value set in register FRDCNTL[RWAIT].

Table 6-6. Minimum Required Flash Wait States with Different Clock Sources and Frequencies

CPUCLK (MHz)	Wait States (FRDCNTL[RWAIT](1))
120 < CPUCLK ≤ 160	3
80 < CPUCLK ≤ 120	2
0 < CPUCLK ≤ 80	1

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

The F28E12x devices have an improved 128-bit prefetch buffer that provides high flash code execution efficiency across wait states. Figure 6-17 and Figure 6-18 illustrate typical efficiency across wait-state settings compared to previous-generation devices with a 64-bit prefetch buffer. Wait-state execution efficiency with a prefetch buffer will depend on how many branches are present in application software. Two examples of linear code and if-then-else code are provided.

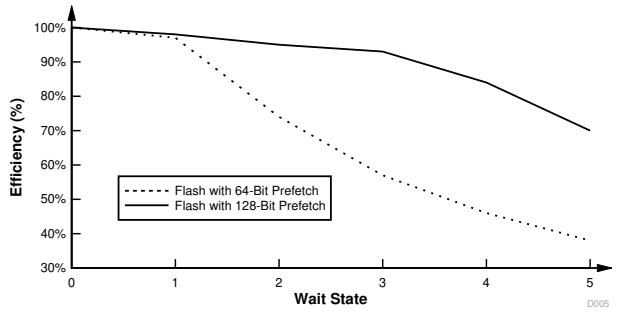

Figure 6-17. Application Code With Heavy 32-Bit Floating-Point Math Instructions

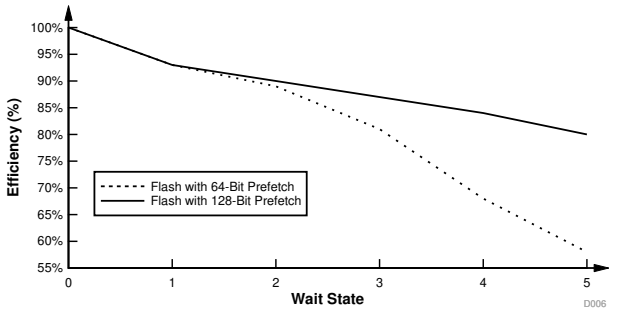

Figure 6-18. Application Code With 16-Bit If-Else Instructions

Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle.

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6.10.4.1 Flash Parameters

PARAMETER		MIN	TYP	MAX	UNIT
Program Time(1)	128 data bits + 16 ECC bits		62.5	625	µs
	2KB (Sector)		8	80	ms
Erase Time(2) (3) at < 25 cycles	2KB (Sector)		15	55	ms
	64KB		17	61	ms
	128KB		18	66	ms
Erase Time(2) (3) at 1000 cycles	2KB (Sector)		25	130	ms
	64KB		28	143	ms
	128KB		30	157	ms
Erase Time(2) (3) at 2000 cycles	2KB (Sector)		30	221	ms
	64KB		33	243	ms
	128KB		36	265	ms
Erase Time(2) (3) at 20K cycles	2KB (Sector)		120	1003	ms
	64KB		132	1102	ms
	128KB		145	1205	ms
N_{wec} Write/Erase Cycles per Bank(4)				100000	cycles
$t_{retention}$ Data retention duration at T_J = 85°C		20			years

(1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
- Flash API itself
- Flash data to be programmed

In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used.
Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does.
Erase time includes Erase verify by the CPU and does not involve any data transfer.

(2) Erase time includes Erase verify by the CPU.

(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

(4) The combined total of bank and sector write/erase cycles is limited to this number.

6.10.5 RAM Specifications

Table 6-7. RAM Parameters

RAM TYPE	SIZE EACH	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	SUPPORTED BUS WIDTHS (BITS)	HOST ACCESS LIST	WAIT STATES	BURST ACCESS SUPPORT
GS RAM	12KB	2	2	1	16/32	C28x	0	No
M0	2KB							
M1								

6.10.6 ROM Specifications

Table 6-8. ROM Parameters

RAM TYPE	SIZE EACH	FETCH TIME (CYCLES)	READ TIME (CYCLES)	STORE TIME (CYCLES)	SUPPORTED BUS WIDTHS (BITS)	HOST ACCESS LIST	WAIT STATES	BURST ACCESS SUPPORT
Boot ROM + Secure ROM	64KB	2	2	1	16/32	C28x	0	No

6.10.7 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22-Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) pin of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND pins should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output pin back to the RTCK input pin of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 kΩ to 4.7 kΩ (depending on the drive strength of the debugger ports). Typically, a 2.2-kΩ value is used.

Header pin $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). Figure 6-19 shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. Figure 6-20 shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header pins EMU2, EMU3, and EMU4 are not used and should be grounded.

For more information about hardware breakpoints and watchpoints, see Hardware Breakpoints and Watchpoints in CCS for C2000 devices.

For more information about JTAG emulation, see the *XDS Target Connection Guide*.

Note

JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.

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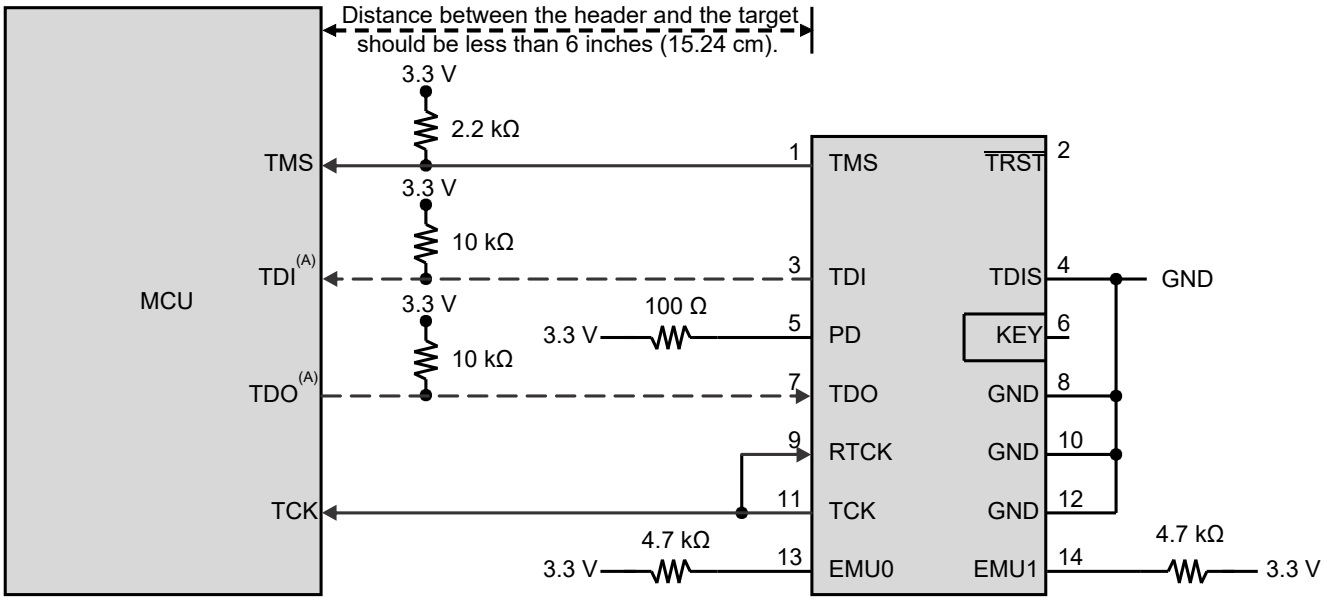
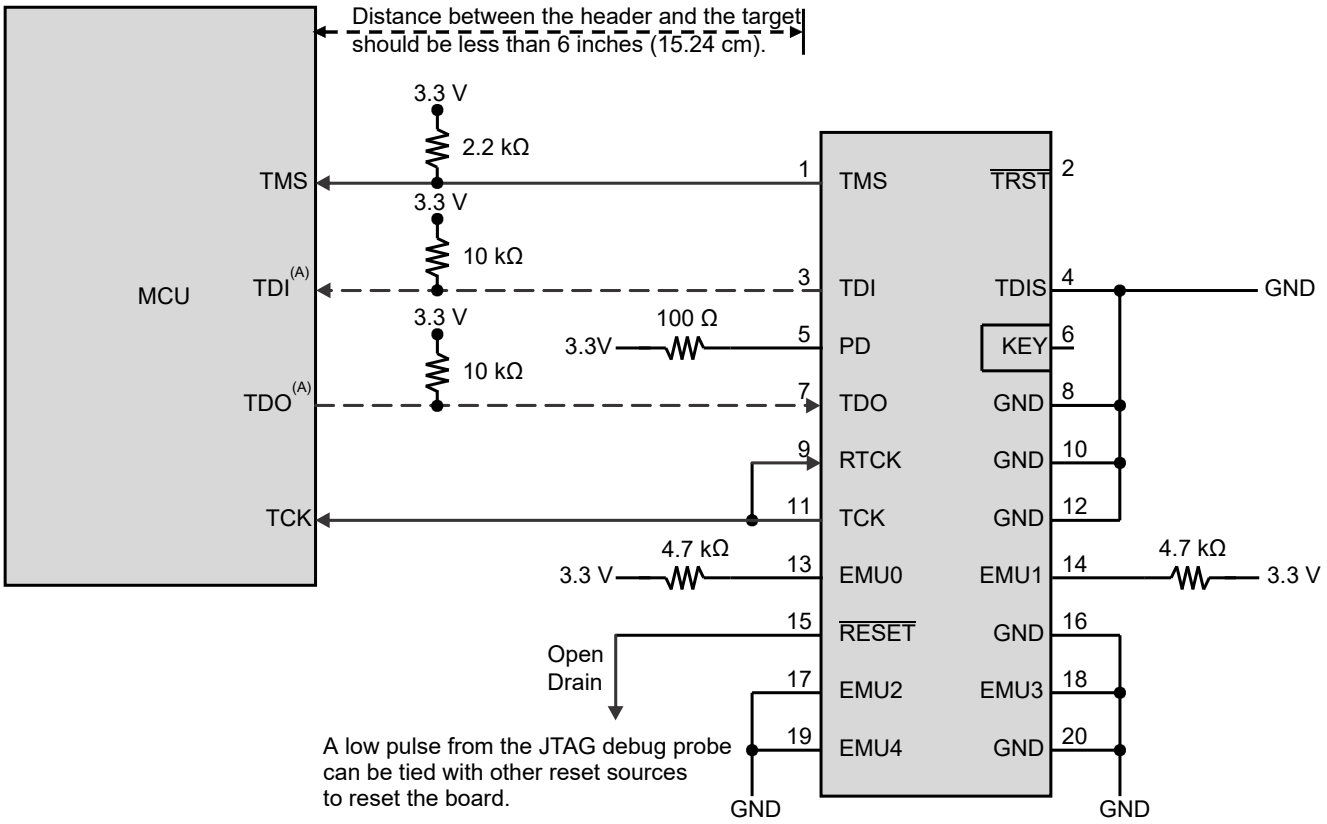


A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-19. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-20. Connecting to the 20-Pin JTAG Header

6.10.7.1 JTAG Electrical Data and Timing

6.10.7.1.1 JTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	66.66		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	26.66		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	26.66		ns
3	$t_{su(TDI-TCKH)}$	Input setup time, TDI valid to TCK high	7		ns
	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	7		
4	$t_{h(TCKH-TDI)}$	Input hold time, TDI valid from TCK high	7		ns
	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	7		

6.10.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TDO)}$	Delay time, TCK low to TDO valid	6	21	ns

6.10.7.1.3 JTAG Timing Diagram

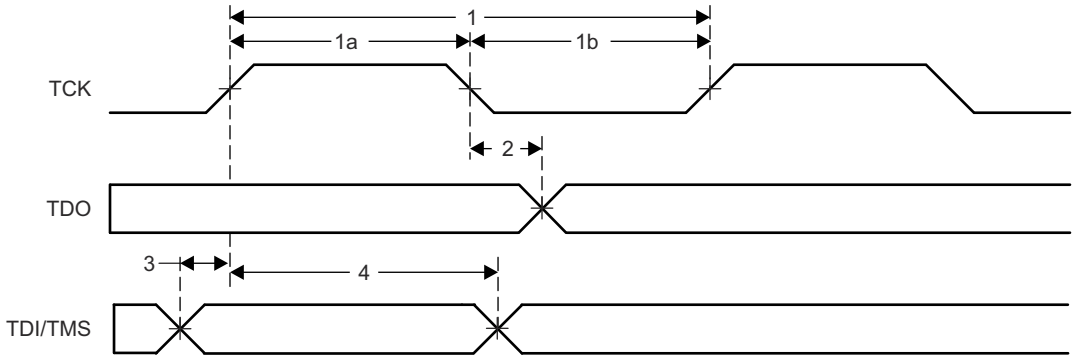


Figure 6-21. JTAG Timing

ADVANCE INFORMATION

6.10.7.2 cJTAG Electrical Data and Timing

6.10.7.2.1 cJTAG Timing Requirements

NO.			MIN	MAX	UNIT
1	$t_{c(TCK)}$	Cycle time, TCK	100		ns
1a	$t_{w(TCKH)}$	Pulse duration, TCK high (40% of t_c)	40		ns
1b	$t_{w(TCKL)}$	Pulse duration, TCK low (40% of t_c)	40		ns
3	$t_{su(TMS-TCKH)}$	Input setup time, TMS valid to TCK high	7		ns
	$t_{su(TMS-TCKL)}$	Input setup time, TMS valid to TCK low	7		ns
4	$t_{h(TCKH-TMS)}$	Input hold time, TMS valid from TCK high	2		ns
	$t_{h(TCKL-TMS)}$	Input hold time, TMS valid from TCK low	2		ns

6.10.7.2.2 cJTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MIN	MAX	UNIT
2	$t_{d(TCKL-TMS)}$	Delay time, TCK low to TMS valid	6	20	ns
5	$t_{dis(TCKH-TMS)}$	Delay time, TCK high to TMS disable		25	ns

6.10.7.2.3 cJTAG Timing Diagram

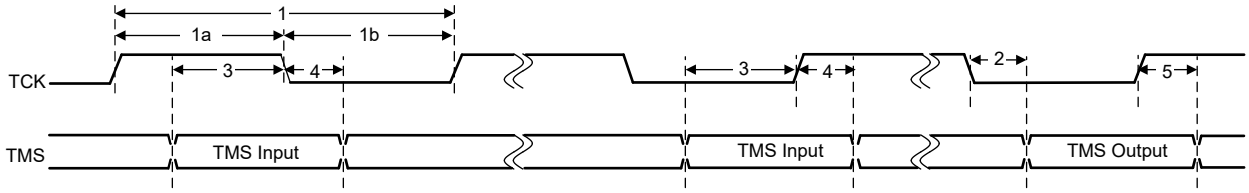


Figure 6-22. cJTAG Timing

6.10.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

Many GPIOs have mux options for Output X-BAR which allows an assortment of internal signals to be routed to a GPIO. All of the GPIOs are connected to each Input X-BAR which can route the GPIO's high or low state to different IP blocks, such as the ADCs, eCAPs, MCPWMs, and external interrupts. For more details, see the X-BAR chapter in the *F28E12x Real-Time Microcontrollers Technical Reference Manual*.

6.10.8.1 GPIO – Output Timing

6.10.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		6(1)	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		6(1)	ns
t_{fGPO}	Toggling frequency, GPIO pins			50	MHz

(1) Rise time and fall time vary with load. These values assume a 6-pF load.

6.10.8.1.2 General-Purpose Output Timing Diagram

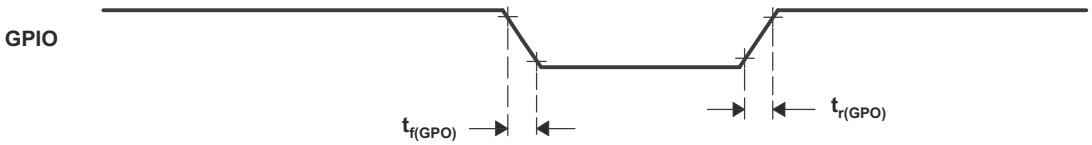


Figure 6-23. General-Purpose Output Timing

ADVANCE INFORMATION

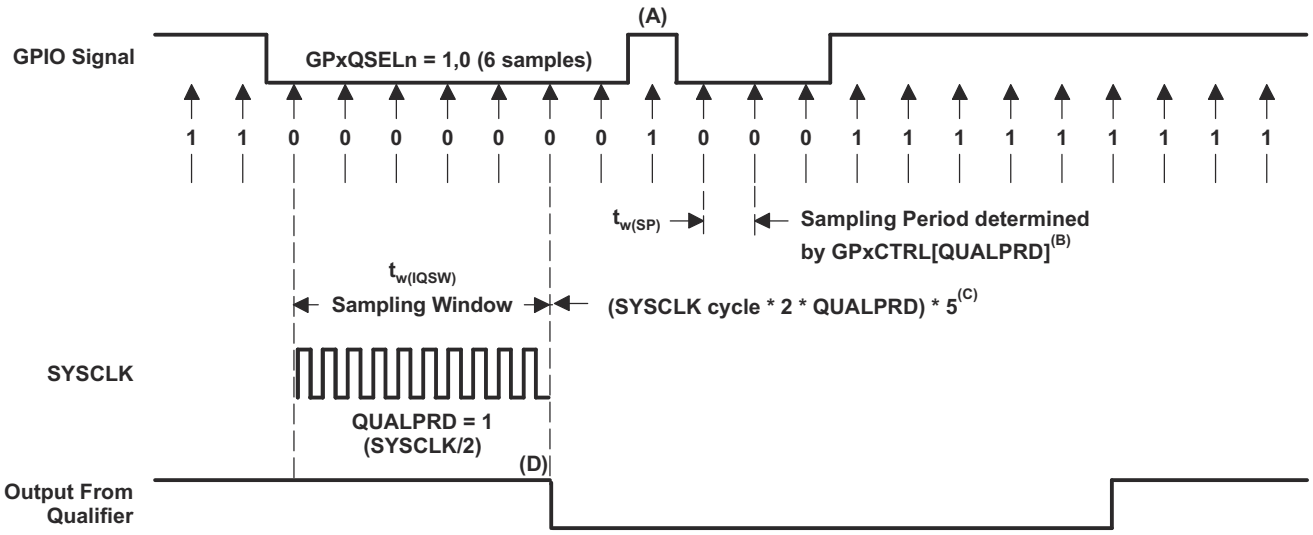
6.10.8.2 GPIO – Input Timing

6.10.8.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SYSCLK)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SYSCLK)}$ * QUALPRD		cycles
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.10.8.2.2 Sampling Mode



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period in 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 6-24. Sampling Mode

6.10.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = SYSCLK/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLK, if QUALPRD = 0

Sampling period = SYSCLK cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLK cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLK cycle) × 5, if QUALPRD = 0

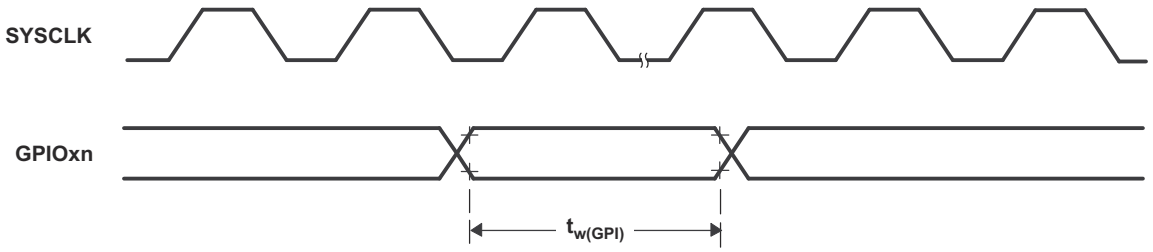


Figure 6-25. General-Purpose Input Timing

ADVANCE INFORMATION

6.10.9 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to four peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 6-26 shows the interrupt architecture for this device.

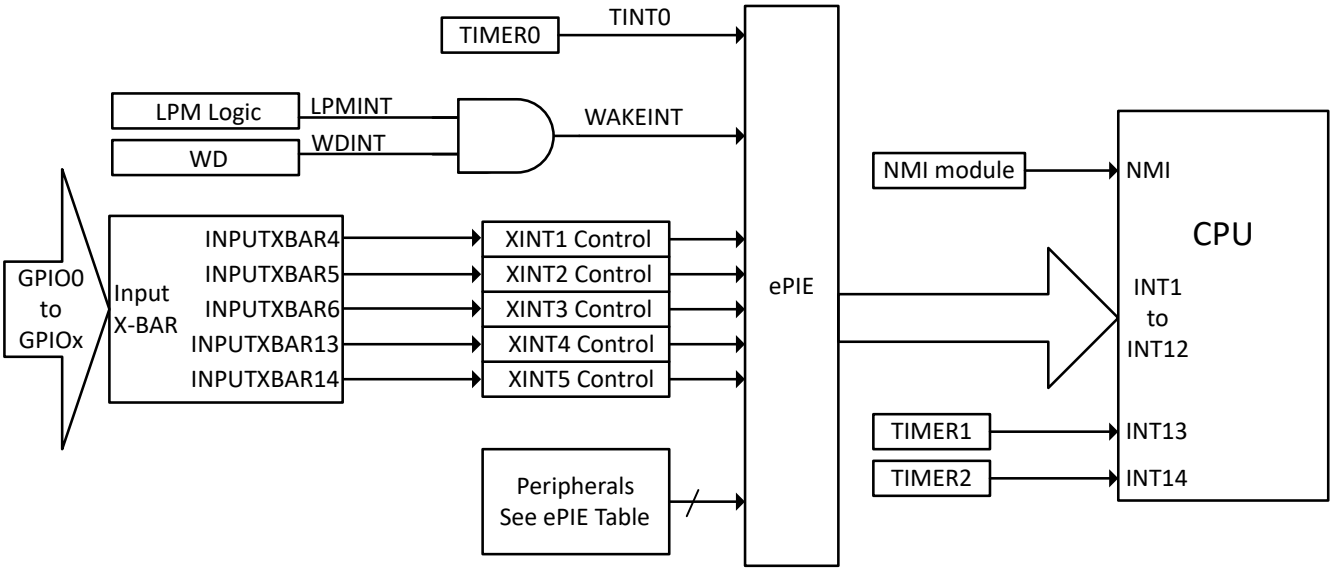


Figure 6-26. Device Interrupt Architecture

6.10.9.1 External Interrupt (XINT) Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.10.9.1.1 External Interrupt Timing Requirements

			MIN	MAX	UNIT
$t_{w(INT)}$	Pulse duration, INT input low/high	Synchronous	$2t_{c(SYSCLK)}$		cycles
		With qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$		cycles

6.10.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch[1]	$t_{w(IQSW)} + 14t_{c(SYSCLK)}$	$t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCLK)}$	cycles

(1) This assumes that the ISR is in a single-cycle memory.

6.10.9.1.3 External Interrupt Timing

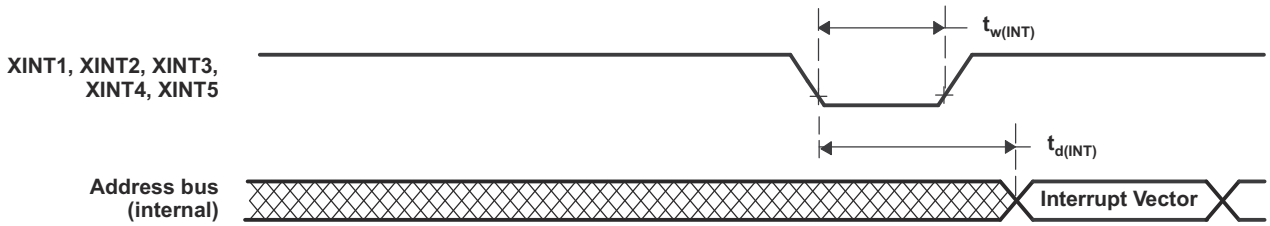


Figure 6-27. External Interrupt Timing

ADVANCE INFORMATION

6.10.10 Low-Power Modes

This device has HALT, IDLE and STANDBY as clock-gating low-power modes.

6.10.10.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. Table 6-9 describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-9. Effect of Clock-Gating Low-Power Modes on the Device

MODULES/ CLOCK DOMAIN	IDLE	STANDBY	HALT
SYSCLK	Active	Gated	Gated
CPUCLK	Gated	Gated	Gated
WDCLK	Active	Active	Gated if CLKSRCCTL1.WDHALTI = 0
PLL	Powered	Powered	Software must power down PLL before entering HALT.
WROSC	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
SYSOSC	Powered	Powered	Powered down if CLKSRCCTL1.WDHALTI = 0
Flash(1)	Powered	Powered	Powered
XTAL(2)	Powered	Powered	Powered

(1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application.
(2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

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6.10.10.2 Low-Power Mode Wake-up Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.10.10.2.1 IDLE Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SYSCLK)}$		cycles
		With input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

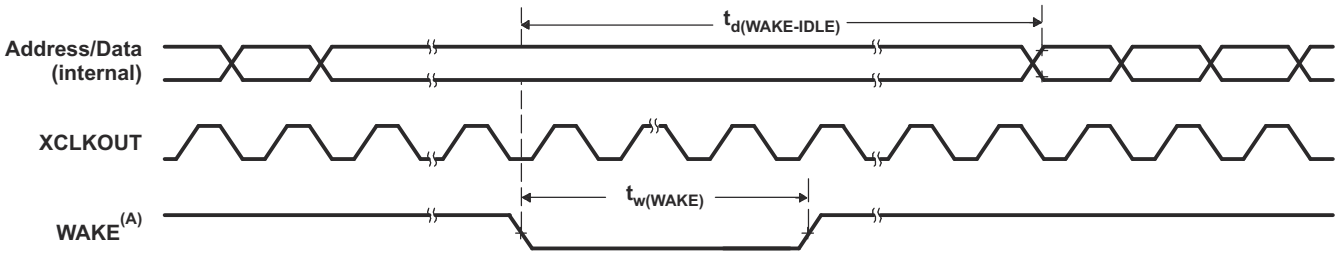
6.10.10.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume(1)	From Flash (active state)	Without input qualifier		$40t_{c(SYSCLK)}$	cycles
			With input qualifier		$40t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles
		From RAM	Without input qualifier		$25t_{c(SYSCLK)}$	cycles
			With input qualifier		$25t_{c(SYSCLK)} + t_{w(WAKE)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.10.10.2.3 IDLE Entry and Exit Timing Diagram



A. WAKE can be any enabled interrupt, $\overline{\text{WDINT}}$ or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-28. IDLE Entry and Exit Timing Diagram

ADVANCE INFORMATION

6.10.10.2.4 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	QUALSTDBY = 0 | $2t_{c(OSCCLK)}$	$3t_{c(OSCCLK)}$		cycles
		QUALSTDBY > 0 | (2 + QUALSTDBY)$t_{c(OSCCLK)}$ (1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

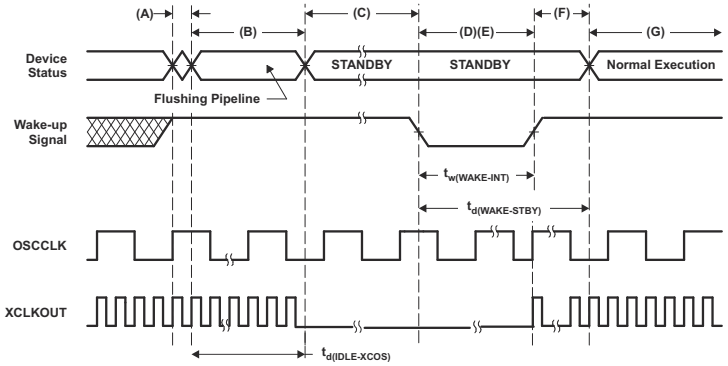
6.10.10.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop			$16t_{c(SYSOSC)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)	Wakeup from flash (Flash module in active state)		$175t_{c(SYSCLK)}$ + $t_{w(WAKE-INT)}$	cycles
$t_{d(WAKE-STBY)}$		Wakeup from RAM		$3t_{c(OSC)}$ + $15t_{c(SYSCLK)}$ + $t_{w(WAKE-INT)}$	cycles

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.10.10.2.6 STANDBY Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into STANDBY mode.
B. The LPM block responds to the STANDBY signal, SYSCLK is held for a maximum 16 SYSOSCDIV4 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. The external wake-up signal is driven active.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-29. STANDBY Entry and Exit Timing Diagram

6.10.10.2.7 HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal[1]	t_{oscst} + $2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal[1]	t_{oscst} + $8t_{c(OSCCLK)}$		cycles

(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See *Crystal Oscillator (XTAL)* section for more information. For applications using SYSOSC or WROSC for OSCCLK, see the Internal Oscillators section for t_{oscst}. Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

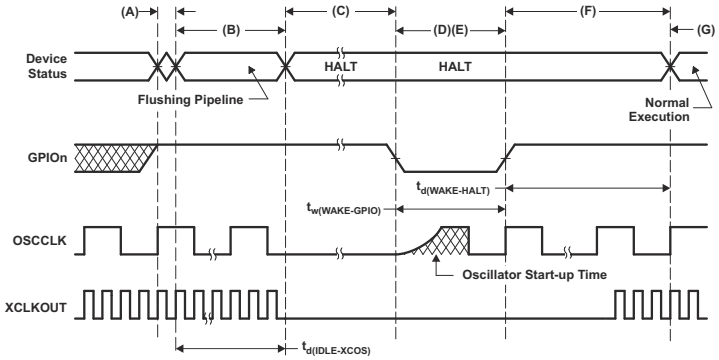
6.10.10.2.8 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOS)}$	Delay time, IDLE instruction executed to XCLKOUT stop		$16t_{c(SYSOSC)}$	cycles
$t_{d(WAKE-HALT)}$	Delay time, external wake signal end to CPU1 program execution resume			cycles
	Wakeup from Flash - Flash module in active state		$75t_{c(OSCCLK)}$	
	Wakeup from RAM		$75t_{c(OSCCLK)}$	

ADVANCE INFORMATION

6.10.10.2.9 HALT Entry and Exit Timing Diagram



A. IDLE instruction is executed to put the device into HALT mode.
B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 SYSOSCDIV4clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the internal oscillator (SYSOSC) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.
E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
G. Normal operation resumes.
H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-30. HALT Entry and Exit Timing Diagram

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6.11 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the Analog-to-Digital Converter (ADC), Temperature Sensor, Programmable Gain Amplifier (PGA), and Lite Comparator Subsystem variant (CMPSS_LITE).

The analog subsystem has the following features:

- Flexible voltage references
  - The ADC is referenced to VREFHI and VSSA pins
    - VREFHI pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
    - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V
  - The comparator DACs are referenced to VDDA and VSSA
- Flexible pin usage
  - Comparator subsystem inputs and digital inputs (AIOs)/outputs (AGPIOs) are multiplexed with ADC inputs
  - Low comparator DAC (CMP3_LITE_DACL) can optionally be brought out to a multiplexed ADC pin for external use (mutually exclusive with use of CMPSS compare functions and only available on some CMPSS instances)
  - Internal connection to VREFLO on ADC for offset self-calibration

Figure 6-31 shows the Analog Subsystem Block Diagram for all packages. Figure 6-32 shows the analog group connections. Section 6.11.1 lists the analog pins and internal connections, as well as the descriptions of analog signals.

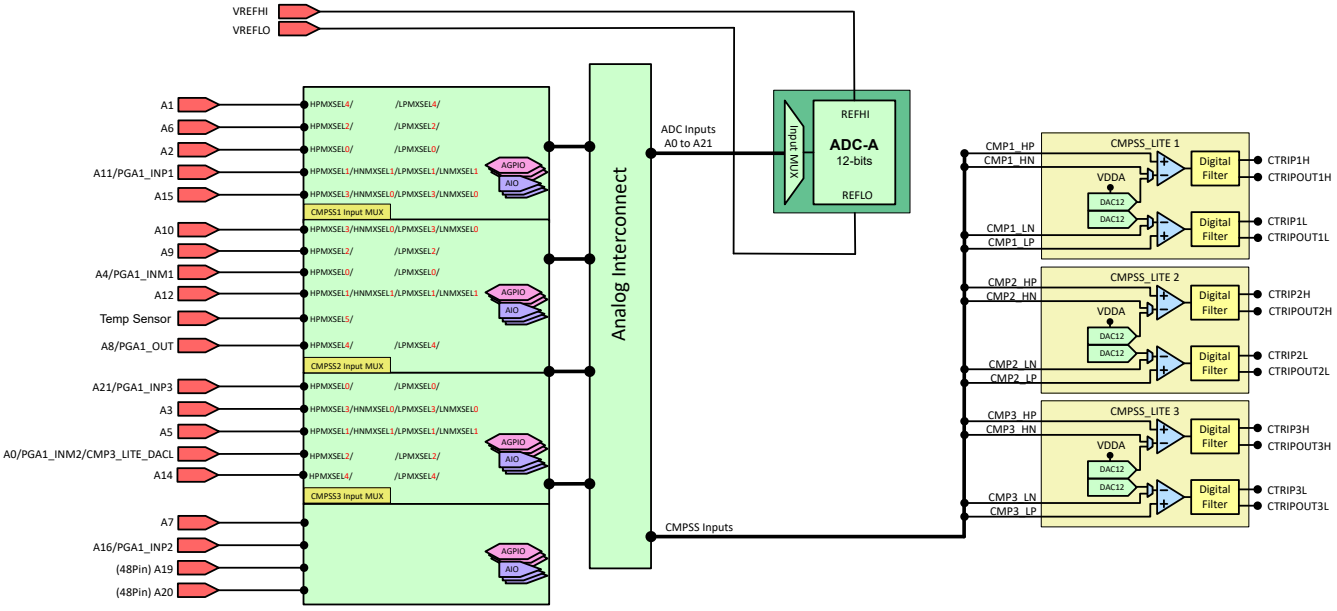
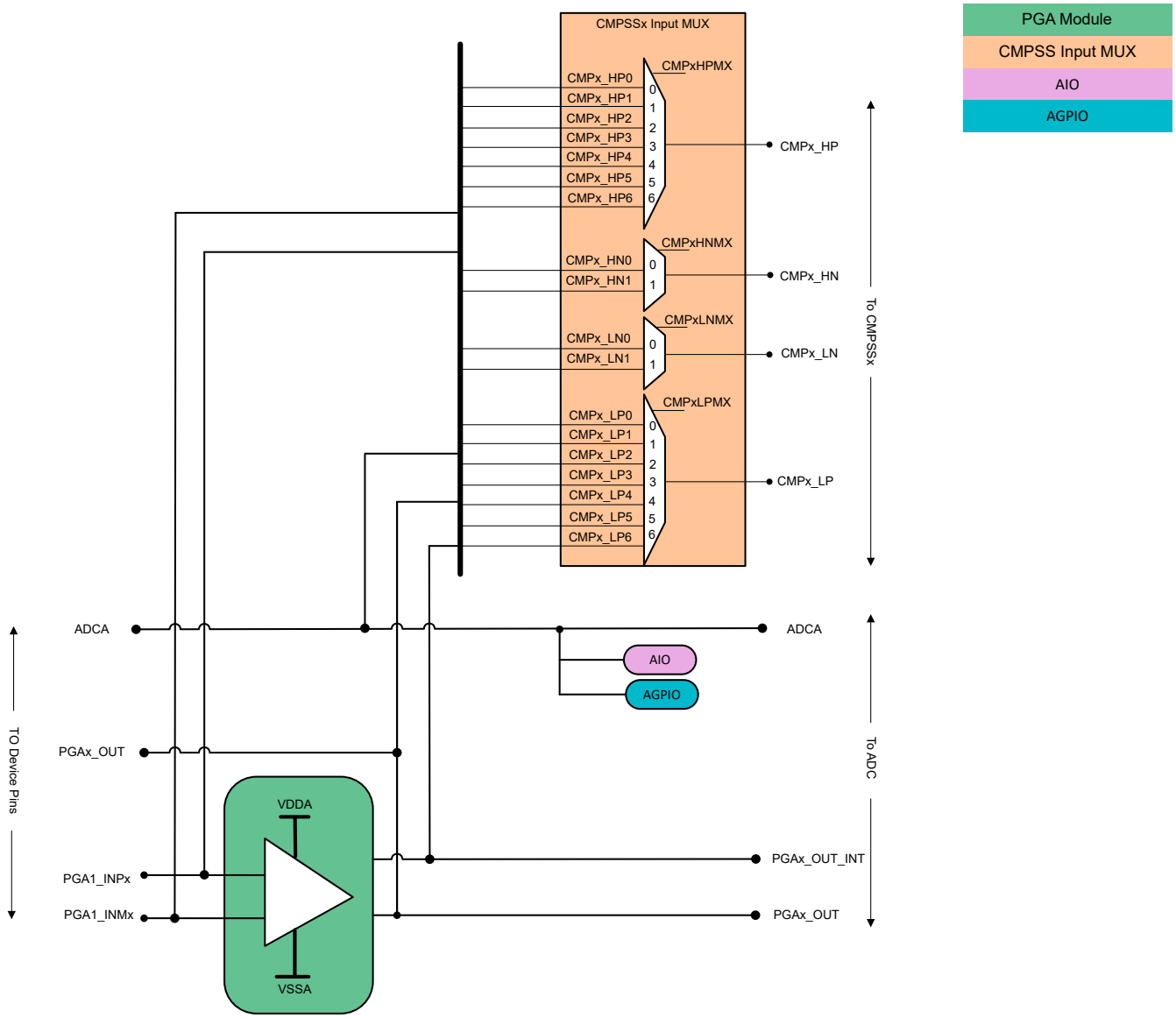


Figure 6-31. Analog Subsystem Block Diagram

ADVANCE INFORMATION



Note: AIOs support digital input mode only.

Figure 6-32. Analog Group Connections

6.11.1 Analog Pins and Internal Connections

Table 6-10. Analog Pins and Internal Connections

Pin Name	Pins/Package			ADC	DAC	PGA	Comparator Subsystem (Mux)				AIO Input/GPIO
	48 QFP	32 QFP	32 QFN				High Positive	High Negative	Low Positive	Low Negative	
VREFHI	12	-(4)	-(4)								
VREFLO	13	-(4)	-(4)								
Analog Group 1							**CMP1**				
A6	4(1)	2(1)	2(1)	A6			CMP1 (HPMXSEL=2)		CMP1 (LPMXSEL=2)		GPIO228(3)
A2	6	4	4	A2			CMP1 (HPMXSEL=0)		CMP1 (LPMXSEL=0)		GPIO224(3)
A15	7(1)	5(1)	5(1)	A15			CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP1 (LNMXSEL=0)	AIO233
A11	8	6(1)	6(1)	A11		PGA_INP1	CMP1 (HPMXSEL=1)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=1)	CMP1 (LNMXSEL=1)	AIO237
A1	10	7(1)	7(1)	A1			CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		AIO232
Analog Group 2							**CMP2**				
A10	21	13(1)	13(1)	A10			CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP2 (LNMXSEL=0)	GPIO230(3)
A12	14	8(1)	8(1)	A12		PGA_INN3	CMP2 (HPMXSEL=1)	CMP2 (HNMXSEL=1)	CMP2 (LPMXSEL=1)	CMP2 (LNMXSEL=1)	AIO238
A8/PGA1_OUT	16	9	9	A8		PGA_OUT	CMP2 (HPMXSEL=4)		CMP2 (LPMXSEL=4)		AIO241
A4/PGA1_INM1	19	12	12	A4		PGA_INM1	CMP2 (HPMXSEL=0)		CMP2 (LPMXSEL=0)		AIO225
A9	20	13(1)	13(1)	A9			CMP2 (HPMXSEL=2)		CMP2 (LPMXSEL=2)		GPIO227(3)
Analog Group 3							**CMP3**				
A3	5	3	3	A3			CMP3 (HPMXSEL=3)	CMP3 (HNMXSEL=0)	CMP3 (LPMXSEL=3)	CMP3 (LNMXSEL=0)	GPIO242(3)
A14	7(1)	5(1)	5(1)	A14			CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO239
A5	9	6(1)	6(1)	A5			CMP3 (HPMXSEL=1)	CMP3 (HNMXSEL=1)	CMP3 (LPMXSEL=1)	CMP3 (LNMXSEL=1)	AIO244
A0/ CMP3_LITE_DACL/ PGA1_INM2	11	7(1)	7(1)	A0	CMP3_LITE_DACL	PGA1_INM2	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO231
A21/PGA1_INP3	4(1)	2(1)	2(1)	A21			CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		GPIO 226(3)

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Table 6-10. Analog Pins and Internal Connections (continued)

Pin Name	Pins/Package			ADC	DAC	PGA	Comparator Subsystem (Mux)				AIO Input/GPIO
	48 QFP	32 QFP	32 QFN				High Positive	High Negative	Low Positive	Low Negative	
Other Analog											
A16/PGA1_INP2	2	32	32	A16		PGA1_INP2					GPIO28[3]
A19	23	-	-	A19							GPIO13[3]
A20	24	-	-	A20							GPIO12[3]
A7	15	8[1]	8[1]	A7							AIO245
TempSensor[2]	-	-	-	A22			CMP1 (HPMXSEL=5)				
PGA1_OUT_INT[2]	-	-	-	A25			CMP2 (HPMXSEL=6)		CMP2 (LPMXSEL=6)		

(1) Signal is bonded together with another signal as a single pin on this package.
(2) Internal connection only; does not come to a device pin.
(3) The GPIOs on these analog pins support full digital input and output functionality and are referred to as AGPIOs. By default, the AGPIOs are unconnected; that is, the analog and digital functions are both disabled. For configuration details, see the *Digital Inputs and Outputs on ADC Pins (AGPIOs)* section.
(4) On 32 RHB and 32 VFC package, VREFHI is internally connected to VDDA and VREFLO is internally connected to VSSA.

Note

The GPIOs on the analog pins support full digital input and output functionality and are referred to as AGPIOs. By default, the AGPIOs are unconnected; that is, the analog and digital functions are both disabled. For configuration details, see the *Digital Inputs and Outputs on ADC Pins (AGPIOs)* section.

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Table 6-11. Analog Signal Descriptions

Signal Name	Description
AIOx	Digital input on ADC pin
AGPIOx	Digital input/output pin with ADC functionality
Ax	ADC A Input
CMPx_HNy	Comparator subsystem high comparator negative input
CMPx_HPy	Comparator subsystem high comparator positive input
CMPx_LNy	Comparator subsystem low comparator negative input
CMPx_LPy	Comparator subsystem low comparator positive input
CMP3_LITE_DACL	DAC output from the lower CMPSS3_LITE DAC (can be brought to an external pin)
PGAx_INPy	PGA module non-inverting pin
PGAx_INMy	PGA module inverting pin
PGAx_OUT	PGA module output
PGAx_OUT_INT	PGA module internal output connected to CMPSS and ADC modules
TempSensor	Internal temperature sensor

Table 6-12. Reference Summary

Module	Reference Option	Configured Where?	Register	Driverlib Function	Notes
ADC	Internal	Analog System	AnalogSubsysRegs. ANAREFCTL.bit. ANAREFxSEL	ADC_setVREF	Both options require use of the VREFHI pin.
	External	Analog System	1) AnalogSubsysRegs. ANAREFCTL.bit. ANAREFxSEL2) AnalogSubsysRegs. REFCONFIGA.bit. CONFIG8	ADC_setVREF	Both options require use of the VREFHI pin.
	3.3V or 2.5V Internal Reference Range	Analog System	AnalogSubsysRegs. ANAREFCTL.bit. ANAREFx2P5SEL	ADC_setVREF	Only applicable when using internal reference mode.
CMPSS DACs	VDDA	CMPSS Module	Not configurable		

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6.11.2 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC wrapper is start-of-conversion (SOC)-based (see the *SOC Principle of Operation* section of the Analog-to-Digital Converter (ADC) chapter in the *F28E12x Real-Time Microcontrollers Technical Reference Manual*).

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signal mode
- Input multiplexer with up to 21 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- Multiple trigger sources
  - Software immediate start
  - All MCPWMs: ADCSOC A or B or C or D
  - GPIO XINT2
  - CPU Timers 0/1/2
  - ADCINT1/2
- Three flexible interrupts
- Hardware oversampling mode up to 8x, with configurable trigger spread delay
- Three post-processing blocks, each with:
  - Saturating offset calibration
  - Error from setpoint calculation
  - High, low, and zero-crossing compare, with interrupt and MCPWMs trip capability
  - 24-bit accumulation register for oversampling, with configurable binary shift

Note

Not every channel can be pinned out from all ADCs. See the *Pin Configuration and Functions* section to determine which channels are available.

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The block diagram for the ADC core and ADC wrapper are shown in Figure 6-33.

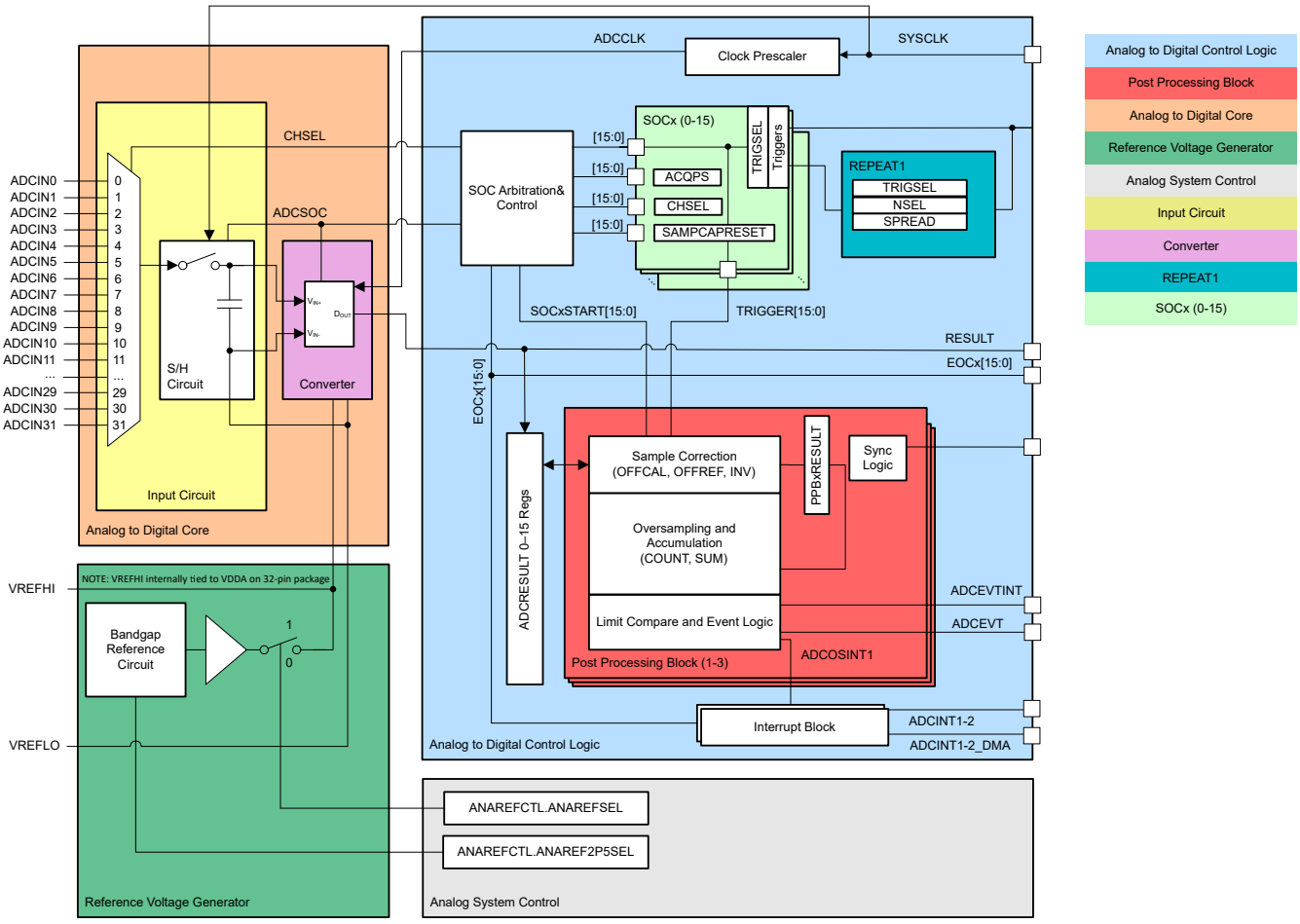

Figure 6-33. ADC Module Block Diagram

ADVANCE INFORMATION

6.11.2.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-13 summarizes the basic ADC options and their level of configurability.

Table 6-13. ADC Options and Configuration Levels

OPTIONS	CONFIGURABILITY
Clock	Per module
Resolution	Not configurable (12-bit resolution only)
Signal mode	Not configurable (single-ended signal mode only)
Reference voltage source	Either external or internal for all modules
Trigger source	Per SOC
Converted channel	Per SOC
Acquisition window duration	Per SOC
EOC location	Per module
Sample Capacitor Reset	Per SOC

6.11.2.1.1 Signal Mode

The ADC supports single-ended signaling. The input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO.

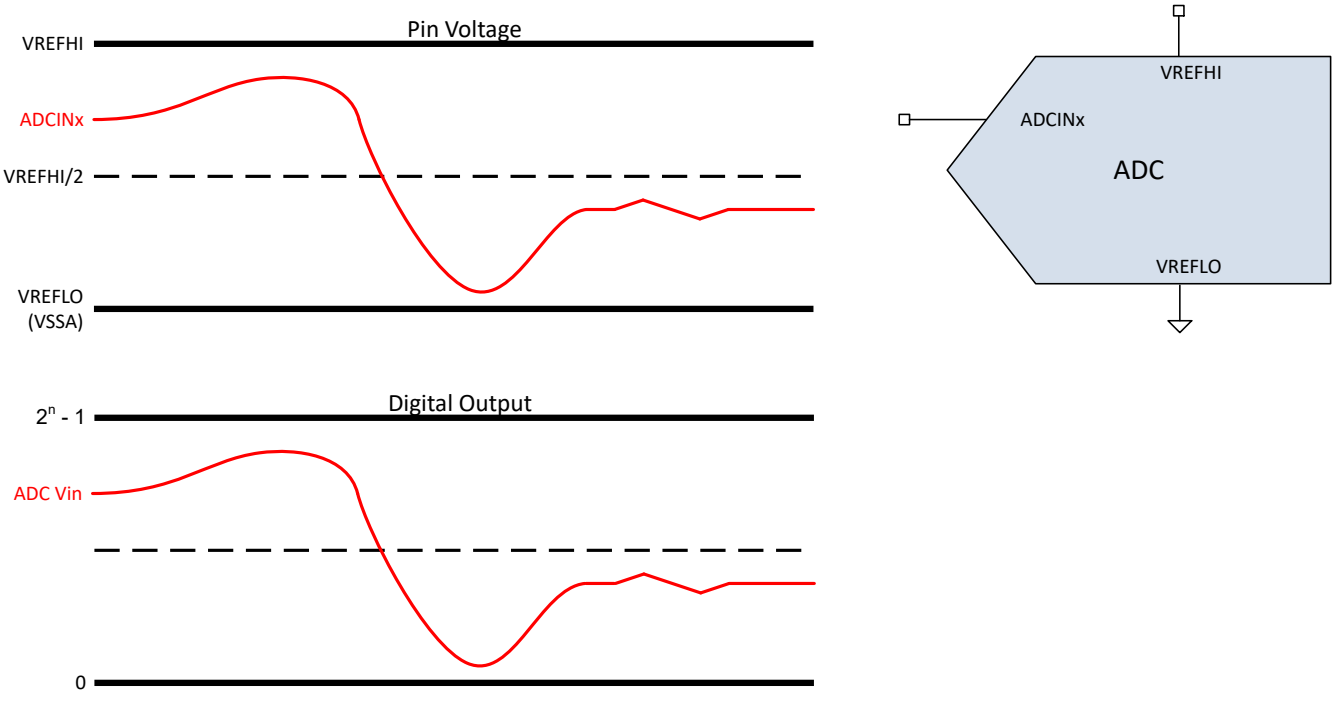

Figure 6-34. Single-ended Signaling Mode

6.11.2.2 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below VDDA + 0.3 V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, VREFHI will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The VREFHI pin must be kept below VDDA + 0.3 V to ensure proper functional operation. If the VREFHI pin exceeds this level, a blocking circuit may activate, and the internal value of VREFHI may float to 0 V internally, giving improper ADC conversion.

6.11.2.2.1 ADC Operating Conditions

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCCLK (derived from PERx.SYSCLK)		5		160	MHz
Sample rate(4) (5)	160-MHz ADCCLK(48-pin with 10Ω on VREFHI)			8.9	MSPS
	120-MHz ADCCLK(48-pin without 10Ω on VREFHI)(6)			7.2	
	80-MHz ADCCLK(32-pin)			5.5	
Sample window duration (set by ACQPS and PERx.SYSCLK)(1)	With 50 Ω or less R_s	37.5			ns
	Internal VREFLO Connection	37.5			
VREFHI	External Reference	2.4	2.5 or 3.0	VDDA	V
VREFHI(2)	Internal Reference = 3.3V Range		1.65		V
	Internal Reference = 2.5V Range		2.5		V
VREFHI	Package = 32QFN, 32QFP	VDDA	VDDA	VDDA	V
VREFLO		VSSA		VSSA	V
VREFHI - VREFLO		2.4		VDDA	V
Conversion range	Internal Reference = 3.3 V Range	0		3.3	V
	Internal Reference = 2.5 V Range	0		2.5	
	External Reference	VREFLO		VREFHI	
	Package = 32QFN, 32QFP	0		VDDA(3)	

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.
(2) In internal reference mode, the reference voltage is driven out of the VREFHI pin by the device. The user should not drive a voltage into the pin in this mode.
(3) On 32QFN package, VREFHI is internally tied to VDDA and VREFLO is internally tied to VSSA. Internal reference mode is not supported on 32QFN package.
(4) Non-integer ADC clock dividers are not supported: ADCCTL2.PRESCALE should only use even values
(5) Sample and hold cap reset feature to VREFHI/2 must be enabled; SAMPCAPRESETSEL = 1 and SAMPCAPRESETDISABLE = 0 inside the corresponding ADCSOCxCTL register
(6) For this value of ADCCLK, the device frequency would need to run at 120MHz as well.

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6.11.2.2.2 ADC Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
ADCCLK Conversion Cycles	160-MHz SYSCLK			11	ADCCLKs
Power Up Time	External Reference mode			500	µs
	Internal Reference mode			5000	µs
	Internal Reference mode, when switching between 2.5-V range and 3.3-V range.			5000	µs
VREFHI input current(1)			40		µA
Internal Reference Capacitor Value(2)		2.2			µF
External Reference Capacitor Value(2)		2.2			µF
DC Characteristics					
Gain Error	Internal reference	TBD	45	TBD	LSB
	External reference		±3		
Offset Error			±2		LSB
Channel-to-Channel Gain Error(4)			2		LSB
Channel-to-Channel Offset Error(4)			2		LSB
ADC-to-ADC Gain Error(5)	Identical VREFHI and VREFLO for all ADCs		4		LSB
ADC-to-ADC Offset Error(5)	Identical VREFHI and VREFLO for all ADCs		2		LSB
DNL Error			-0.999 to 1		LSB
INL Error			±2.0		LSB
ADC-to-ADC Isolation	VREFHI = 2.5 V, synchronous ADCs	–1		1	LSBs
AC Characteristics					
SNR(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		67.08		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from SYSOSCDIV4		TBD		
THD(3)	VREFHI = 2.5 V, fin = 100 kHz		–80		dB
SFDR(3)	VREFHI = 2.5 V, fin = 100 kHz		82		dB
SINAD(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1		66.8		dB
	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from SYSOSCDIV4		TBD		
ENOB(3)	VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC		10.8		bits
PSRR	VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz		60		dB
	VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz		57		
	VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz		60		
	VDDA = 3.3-V DC + 200 mV Sine at 900 kHz		57		

(1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
(2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
(3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
(4) Variation across all channels belonging to the same ADC module.
(5) Worst case variation compared to other ADC modules.

6.11.2.2.3 ADC INL and DNL

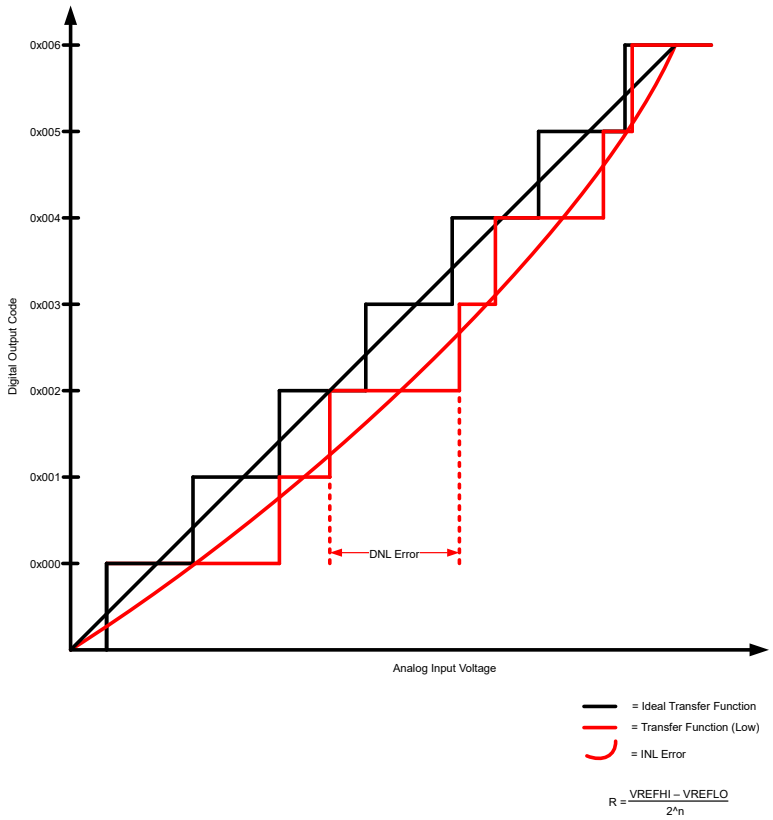


Figure 6-35. ADC INL and DNL

6.11.2.2.4 ADC Input Model

The ADC input characteristics are given by Table 6-14 and Figure 6-36.

Table 6-14. Input Model Parameters for 12-bit ADC

	DESCRIPTION	REFERENCE MODE	VALUE
C_p	Parasitic input capacitance	All	See Per-Channel Parasitic Capacitance for 48-Pin PT LQFP, Per-Channel Parasitic Capacitance for 32-Pin VFC LQFP, and Per-Channel Parasitic Capacitance for 32-Pin RHB VQFN
R_{on}	Sampling switch resistance	External Reference, 2.5-V Internal Reference	400Ω
		3.3-V Internal Reference	500Ω
C_h	Sampling capacitor	External Reference, 2.5-V Internal Reference	10pF
		3.3-V Internal Reference	8pF
R_s	Nominal source impedance	All	50 Ω

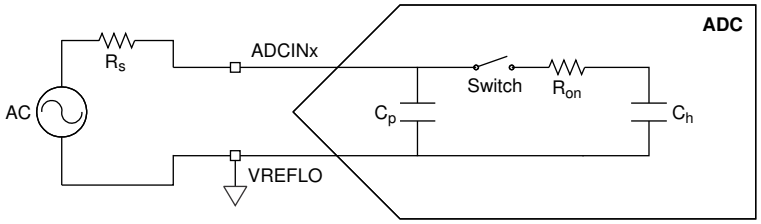


Figure 6-36. Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For recommendations on improving ADC input circuits, see the *ADC Input Circuit Evaluation for C2000 MCUs* Application Note.

Table 6-15. Per-Channel Parasitic Capacitance for 48-Pin PT LQFP

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/C15/CMP3_LITE_DACL	TBD	TBD
A1	TBD	TBD
A2/C9	TBD	TBD
A3/C5	TBD	TBD
A4/C14	TBD	TBD
A5/C2	TBD	TBD
A6/C6	TBD	TBD
A7/C3	TBD	TBD
A8/C11	TBD	TBD
A9/C8	TBD	TBD
A10/C10	TBD	TBD
A11/C0	TBD	TBD
A12/C1	TBD	TBD
A14/A15/C4/C7/ADCINCAL	TBD	TBD
A16/C16	TBD	TBD
A19/C19	TBD	TBD

Table 6-15. Per-Channel Parasitic Capacitance for 48-Pin PT LQFP (continued)

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A20/C20	TBD	TBD

Table 6-16. Per-Channel Parasitic Capacitance for 32-Pin RHB VQFN

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/A1/C15/CMP3_LITE_DACL	TBD	TBD
A2/C9	TBD	TBD
A3/C5	TBD	TBD
A4/C14	TBD	TBD
A5/C2/A11/C0	TBD	TBD
A6/C6	TBD	TBD
A7/C3/A12/C1	TBD	TBD
A8/C11	TBD	TBD
A9/C8/A10/C10	TBD	TBD
A14/A15/C4/C7/ADCINCAL	TBD	TBD
A16/C16	TBD	TBD

Table 6-17. Per-Channel Parasitic Capacitance for 32-Pin VFC LQFP

ADC CHANNEL	C_p (pF)	
	COMPARATOR DISABLED	COMPARATOR ENABLED
A0/A1/C15/CMP3_LITE_DACL	TBD	TBD
A2/C9	TBD	TBD
A3/C5	TBD	TBD
A4/C14	TBD	TBD
A5/C2/A11/C0	TBD	TBD
A6/C6	TBD	TBD
A7/C3/A12/C1	TBD	TBD
A8/C11	TBD	TBD
A9/C8/A10/C10	TBD	TBD
A14/A15/C4/C7/ADCINCAL	TBD	TBD
A16/C16	TBD	TBD

ADVANCE INFORMATION

6.11.2.2.5 ADC Timing Diagrams

the ADC conversion timings for two SOCs given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOCs are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the interrupt controller).

Table 6-18 lists the descriptions of the ADC timing parameters.

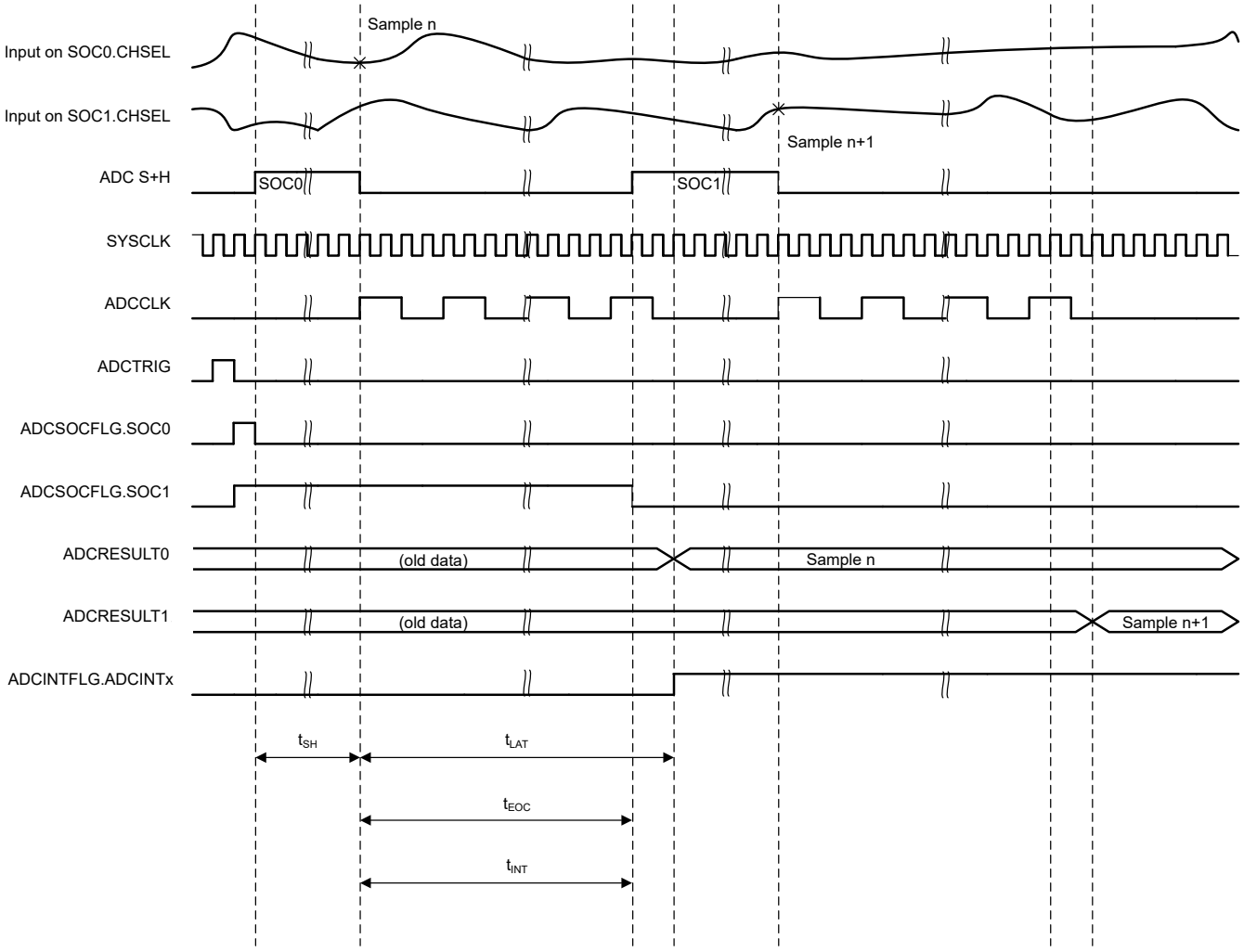


Figure 6-37. ADC Timings

Table 6-18. ADC Timing Parameter Descriptions

PARAMETER	DESCRIPTION
t_{SH}	The duration of the S+H window. At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by (ACQPS + 1) SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOCs. **Note:** The value on the S+H capacitor is captured approximately 5 ns before the end of the S+H window regardless of device clock settings.
t_{LAT}	The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register. If the ADCRESULTx register is read before this time, the previous conversion results are returned.
t_{EOC}	The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched.
t_{INT}	The time from the end of the S+H window until an ADCINT flag is set (if configured). If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal. If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read).
t_{DMA}	The time from the end of the S+H window until a DMA read of the ADC conversion result is triggered, when ADCCTL1.TDMAEN = 1. If TDMAEN is set to 0, then the DMA trigger occurs at T_{INT}. In certain conditions, the ADCINT flag can be set before the ADCRESULT value is latched. To make sure that the DMA read occurs after the ADCRESULT value has been latched, write 1 to ADCCTL1.TDMAEN to enable DMA timings.

Table 6-19. ADC Timings in 12-bit Mode with SAMPCAPRESETSEL = 0

ADCCLK Prescale		SYSCLK Cycles				
ADCCTL2.PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)(1)	t_{INT} (Late)	t_{DMA}
0	1	12	17	1	12	17
2	2	24	34	1	24	34
4	3	36	41	1	36	41
8	5	60	65	1	60	65
10	6	72	77	1	72	77
12	7	84	89	1	84	89
14	8	96	101	1	96	101

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

Table 6-20. ADC Timings in 12-bit Mode with SAMPCAPRESETSEL = 1

ADCCLK Prescale		SYSCLK Cycles				
ADCCTL2.PRESCALE	Prescale Ratio	t_{EOC}	t_{LAT}	t_{INT} (Early)(1)	t_{INT} (Late)	t_{DMA}
0	1	11	16	1	11	16
2	2	24	34	1	24	34
4	3	36	41	1	36	41
6	4	47	52	1	47	52
8	5	59	64	1	59	64
10	6	71	76	1	71	76
12	7	83	88	1	83	88
14	8	95	100	1	95	100

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

ADVANCE INFORMATION

6.11.3 Comparator Subsystem (CMPSS_LITE)

The Comparator Subsystem (CMPSS_LITE) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs (CMPSS_LITE instances are 9.5-bit effective reference DACs), and two digital filters. Comparators are denoted "H" or "L" within each module where “H” and “L” represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin (see the Analog Subsystem chapter of the for mux options available to the CMPSS). The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required.

Each CMPSS includes:

- Two analog comparators
- Two programmable reference 12-bit DACs (9.5-bit effective DACs on CMPSS_LITE instances)
- Two digital filters, 65536 max filter clock prescale
- Ability to synchronize submodules with MCPWMSYNCPER
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option for positive input of comparator to be driven by an external signal or by the PGA
- Option to use the low comparator DAC output, CMPx_DACL, on an external pin (select instances only, mutually exclusive with use of compare functionality)

6.11.3.1 COMPDACOUT

Some CMPSS module instances have support for DAC output buffered to a pin. This CMP3_LITE_DACL output from the CMPSS module uses the low-side DAC of the CMPSS module specified. When using DAC output from a CMPSS instance, all other CMPSS module features for that instance are unavailable.

For CMPx_LITE_DACL instance available for a particular device, please see the DAC column of the *Analog Pins and Internal Connections* table.

See the *Buffered Output from CMPx_LITE_DACL Electrical Characteristics* section for DAC output capabilities.

6.11.3.2 CMPSS Connectivity Diagram

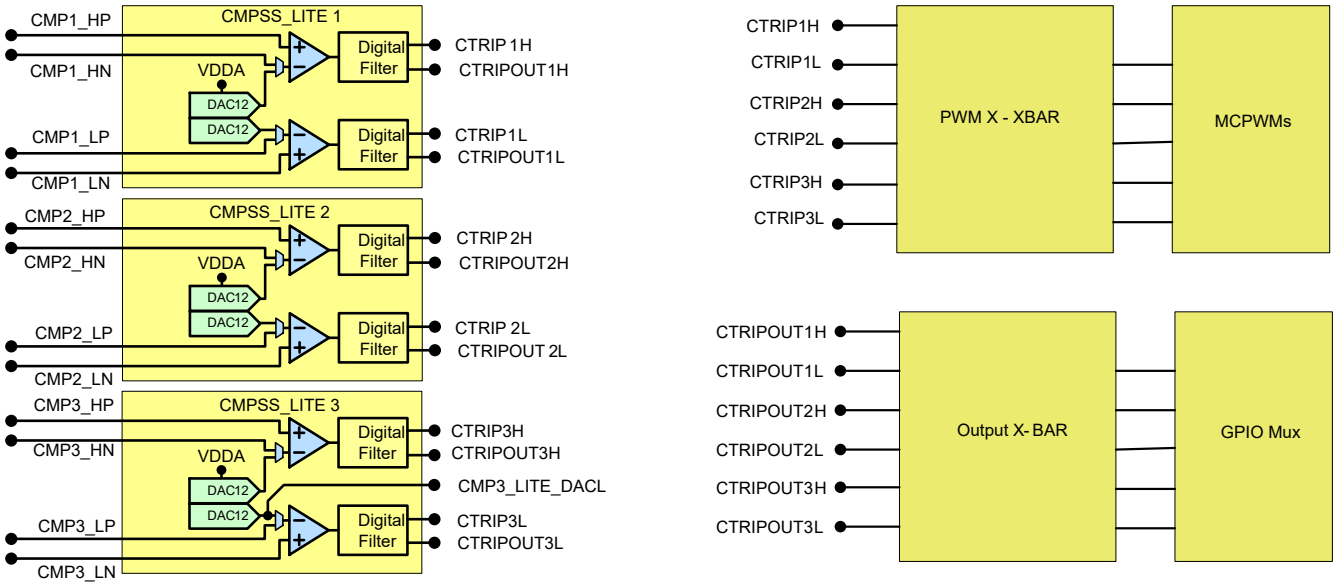


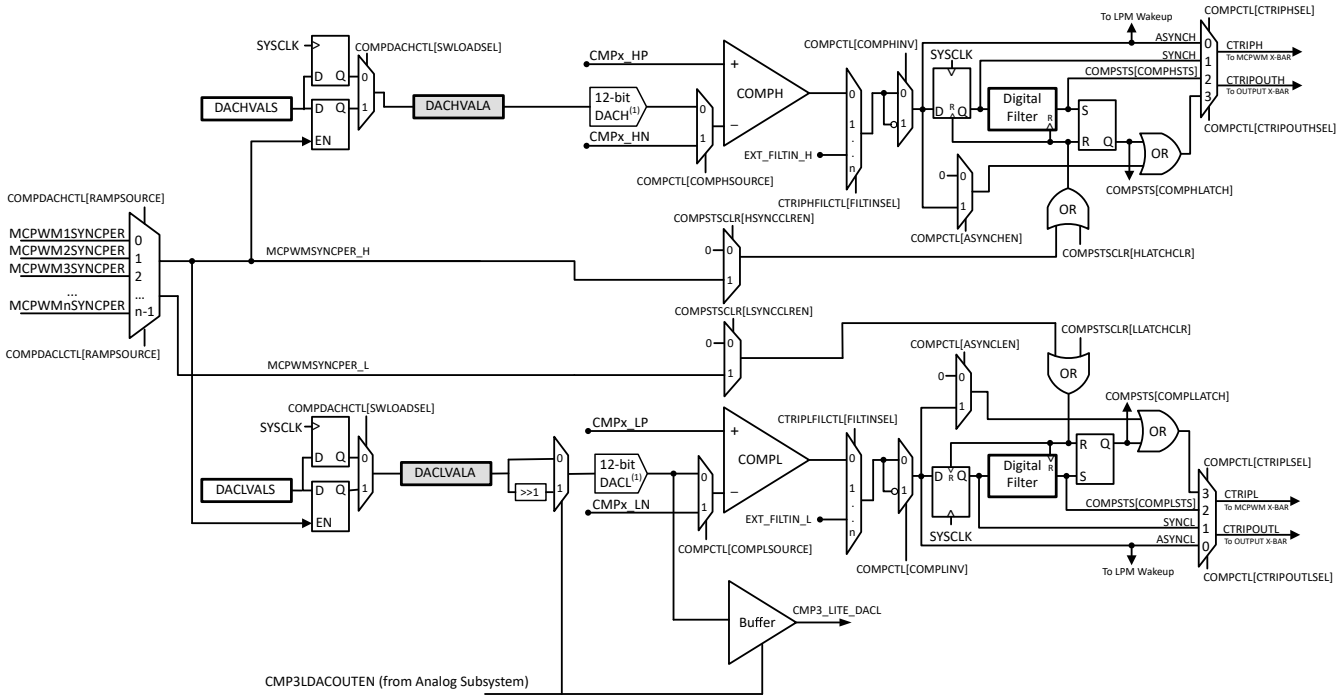
Figure 6-38. CMPSS Connectivity

ADVANCE INFORMATION

6.11.3.3 Block Diagram

The block diagram for the CMPSS_LITE is shown in Figure 6-39.

- CTRIPx (x= "H" or "L") signals are connected to the PWM X-BAR for MCPWM trip response. See the Multichannel Pulse Width Modulator (MCPWM) chapter of the *F28E12x Real-Time Microcontrollers Technical Reference Manual* for more details on the PWM X-BAR mux configuration.
- CTRIPxOUTx (x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the General-Purpose Input/Output (GPIO) chapter of the *F28E12x Real-Time Microcontrollers Technical Reference Manual* for more details on the Output X-BAR mux configuration.



A. CMP3_LITE_DACL only exists for the CMPSS 3 module on this device.

B. Enabling the DACL to a pin disables its functionality to the CMPL(low side comparator), the negative input to COMPL must be driven from a device pin in this case.

Figure 6-39. CMPSS Module Block Diagram

Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator. Some CMPSS instances also allow the low DAC output to be routed to a pin to act as an external DAC. In this case, the DAC output is not available to the COMPL. The negative input to COMPL needs to be driven from the device pin in this case.

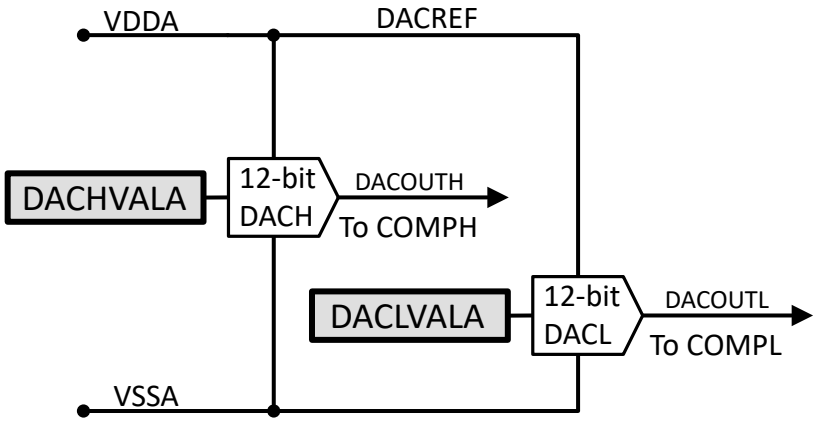


Figure 6-40. Reference DAC Block Diagram

ADVANCE INFORMATION

6.11.3.4 CMPSS Electrical Data and Timing

6.11.3.4.1 CMPSS_LITE Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPU	Power-up time	Bandgap Not Enabled			500	µs
Comparator input (CMPINxx) range			0		VDDA	V
Input referred offset error		Via AIO/AGPIO, Input common mode = 5% to 95% of VDDA	–20		20	mV
Hysteresis(1)		1x	2	10	19	mV
		2x	8	20	34	
		3x	15	30	51	
		4x	20	41	70	
		5x	26	52	88	
		6x	32	64	109	
		7x	38	77	131	
Response time (delay from CMPINx input change to output on MCPWM X-BAR or Output X-BAR)		Step response		21	40	ns
		Ramp response (1.65V/µs)		26		
		Ramp response (8.25mV/µs)		30		
PSRR	Power Supply Rejection Ratio	Up to 250 kHz		46		dB
CMRR	Common Mode Rejection Ratio		40			dB

(1) Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

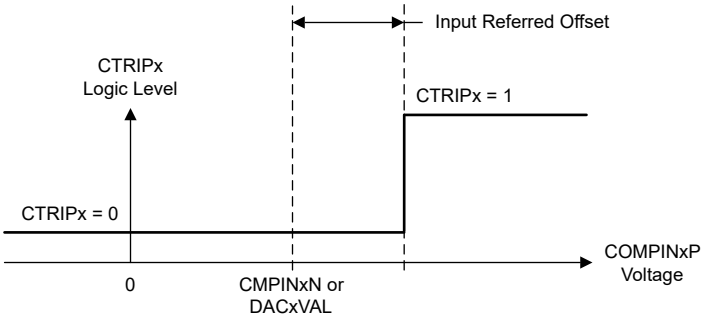


Figure 6-41. CMPSS Comparator Input Referred Offset

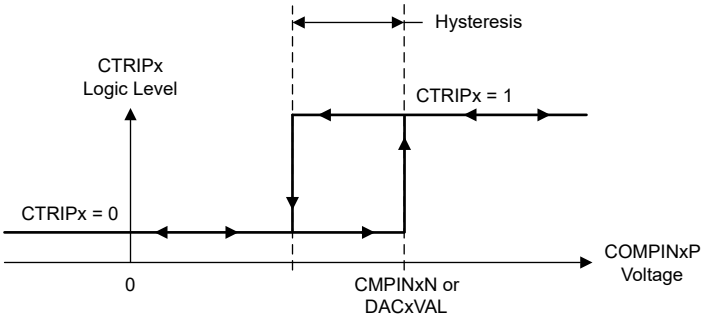


Figure 6-42. CMPSS Comparator Hysteresis

6.11.3.4.2 CMPSS_LITE DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMPSS_LITE DAC output range		0		VDDA	V
Static offset error(1)		–25		25	mV
Static gain error(1)		–0.5		0.5	% of FSR
Static DNL	Endpoint corrected	–5		5	LSB (12-bit)
Static INL	Endpoint corrected	–5		5	LSB (12-bit)
Static TUE (Total Unadjusted Error)				35	mV
Settling time	Settling to 1LSB after full-scale output change		1		µs
Resolution(2)			12		bits

(1) Includes comparator input referred errors.
(2) 9.5-bit effective resolution for monotonic response

6.11.3.4.3 CMPSS Illustrative Graphs

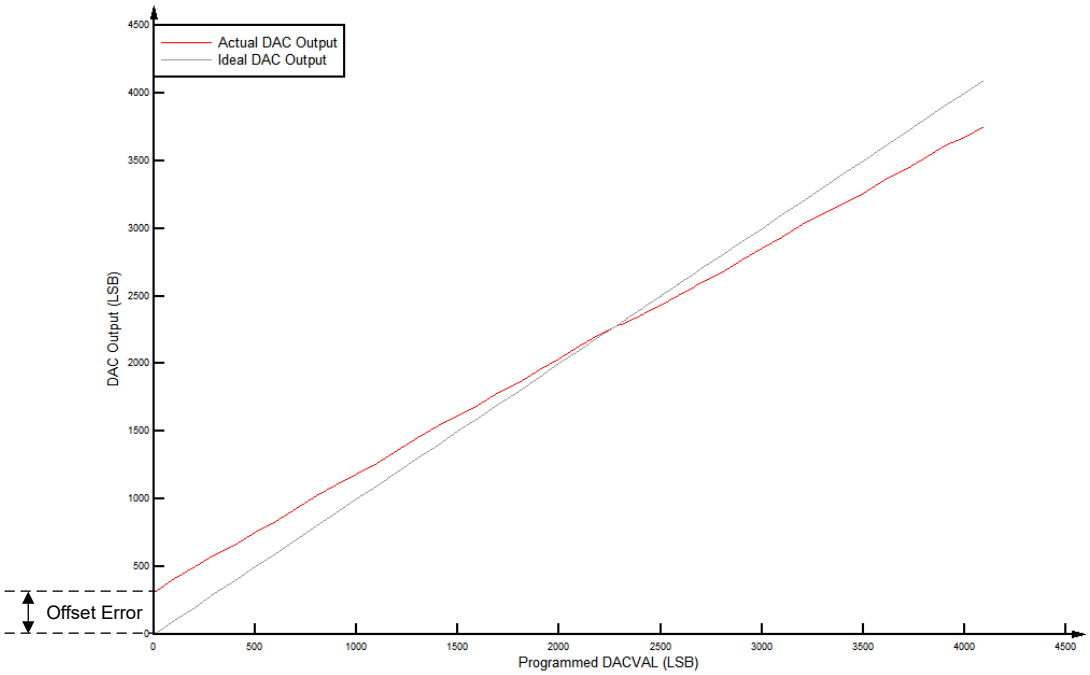


Figure 6-43. CMPSS DAC Static Offset

ADVANCE INFORMATION

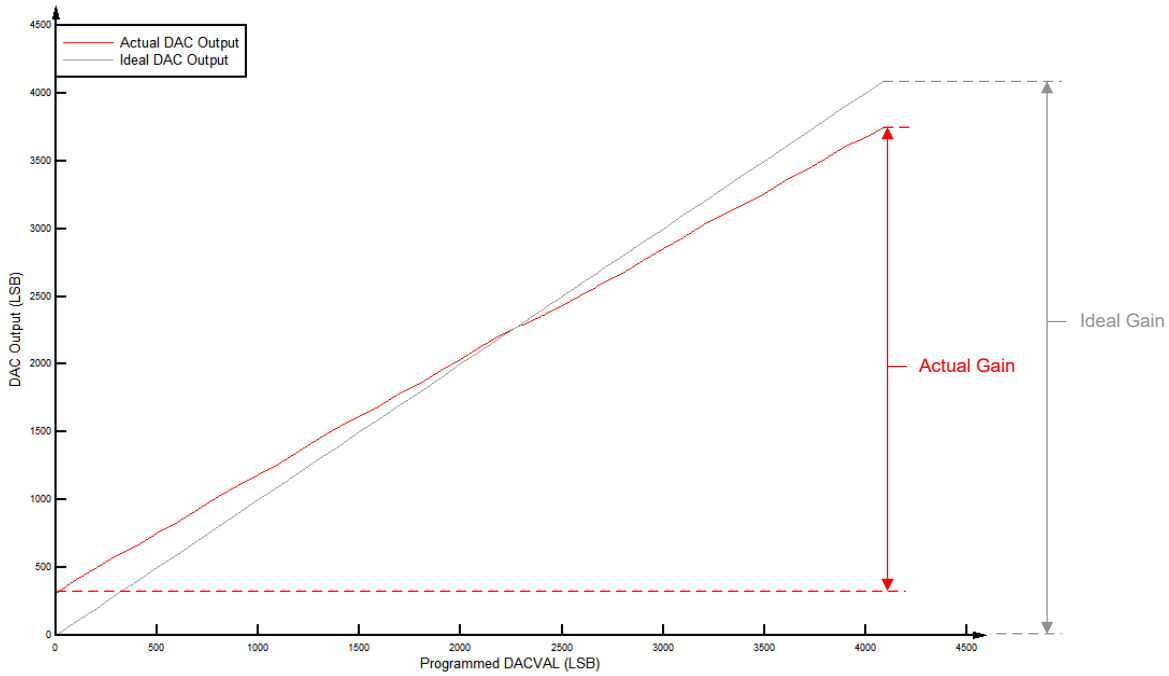


Figure 6-44. CMPSS DAC Static Gain

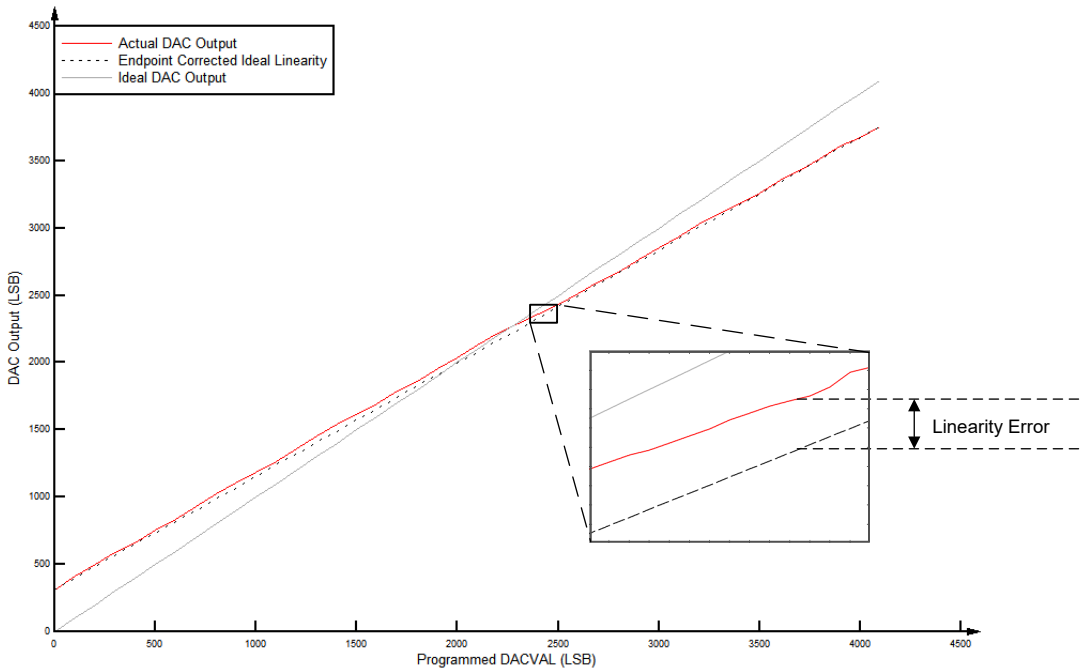


Figure 6-45. CMPSS DAC Static Linearity

6.11.3.4.4 Buffered Output from CMPx_LITE_DACL Operating Conditions

over recommended operating conditions (unless otherwise noted)[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_L	Resistive Load[(2)]		5			kΩ
C_L	Capacitive Load				100	pF

6.11.3.4.4 Buffered Output from CMPx_LITE_DACL Operating Conditions (continued)

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Valid Output Voltage Range(3)	R_L = 5 kΩ	0.3		VDDA – 0.3	V
		R_L = 1 kΩ	0.6		VDDA – 0.6	V
Reference Voltage(4)		VREFHI	2.4	2.5 or 3.0	VDDA	V

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
(3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
(4) For best PSRR performance, VREFHI should be less than VDDA.

6.11.3.4.5 Buffered Output from CMPx_LITE_DACL Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
Resolution(4)				12		bits
Load Regulation				±1		mV/V
Glitch Energy				1.5		V-ns
Voltage Output Settling Time Full-Scale		Settling to 2 LSBs after 0.3V-to-3V transition		2		µs
Voltage Output Settling Time 1/4th Full-Scale		Settling to 2 LSBs after 0.3V-to-0.75V transition		1.6		µs
Voltage Output Slew Rate		Slew rate from 0.3V-to-3V transition		2.8		V/µs
Load Transient Settling Time		5-kΩ Load		700		ns
DC Characteristics						
Offset	Offset Error			±100		mV
Gain	Gain Error(2)		–1.5		1.5	% of FSR
DNL	Differential Non Linearity	Endpoint corrected		±6		LSB (12-bit)
INL	Integral Non Linearity	Endpoint corrected		±7		LSB (12-bit)
AC Characteristics						
Output Noise		Integrated noise from 100 Hz to 100 kHz		TBD		µVrms
		Noise density at 10 kHz		TBD		nVrms/√Hz
SNR	Signal to Noise Ratio	1 kHz, 200 KSPS		TBD		dB
THD	Total Harmonic Distortion	1 kHz, 200 KSPS		TBD		dB
SFDR	Spurious Free Dynamic Range	1 kHz, 200 KSPS		TBD		dB
SINAD	Signal to Noise and Distortion Ratio	1 kHz, 200 KSPS		TBD		dB
PSRR	Power Supply Rejection Ratio(3)	DC		TBD		dB
		100 kHz		TBD		dB

(1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
(2) Gain error is calculated for linear output range.
(3) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.
(4) 11-bit effective (monotonic response).

ADVANCE INFORMATION

6.11.4 Programmable Gain Amplifier (PGA)

The Programmable Gain Amplifier (PGA) is used to amplify an input voltage for the purpose of increasing the effective resolution of the downstream ADC and CMPSS modules.

The integrated PGA helps to reduce cost and design effort for many control applications that traditionally require external, stand-alone amplifiers. On-chip integration ensures that the PGA is compatible with the downstream ADC and CMPSS modules. Software-selectable gain and filter settings make the PGA adaptable to various performance needs.

The PGA has the following features:

- Rail to rail input and output voltage within VDDA and VSSA range
- Programmable gain modes including unity gain and other values from 2X - 64X
- Standalone gain mode using off-chip passive components
- Post-gain filtering using on-chip resistors
- Differential input support
- Hardware assisted chopping for offset reduction
- Support for Kelvin ground connections using PGA_INM pins

The active component in the PGA is an embedded operational amplifier (op amp) that is configured as a non-inverting or inverting amplifier with internal feedback resistors. These internal feedback resistor values are paired to produce software selectable voltage gains.

Three PGA signals are available at the device pins:

- PGA_INP is the positive input to the PGA op-amp.
- PGA_INM is the negative input to the PGA op-amp. See the device data manual for more information.
- PGA_OUT supports op-amp output filtering with RC components. The filtered signal is available for sampling and monitoring by on-chip ADC and CMPSS modules.

PGA_OUT_INT is an internal signal at the op amp output. It is available for sampling and monitoring by the internal ADC and CMPSS modules. Figure 6-46 shows the PGA block diagram.

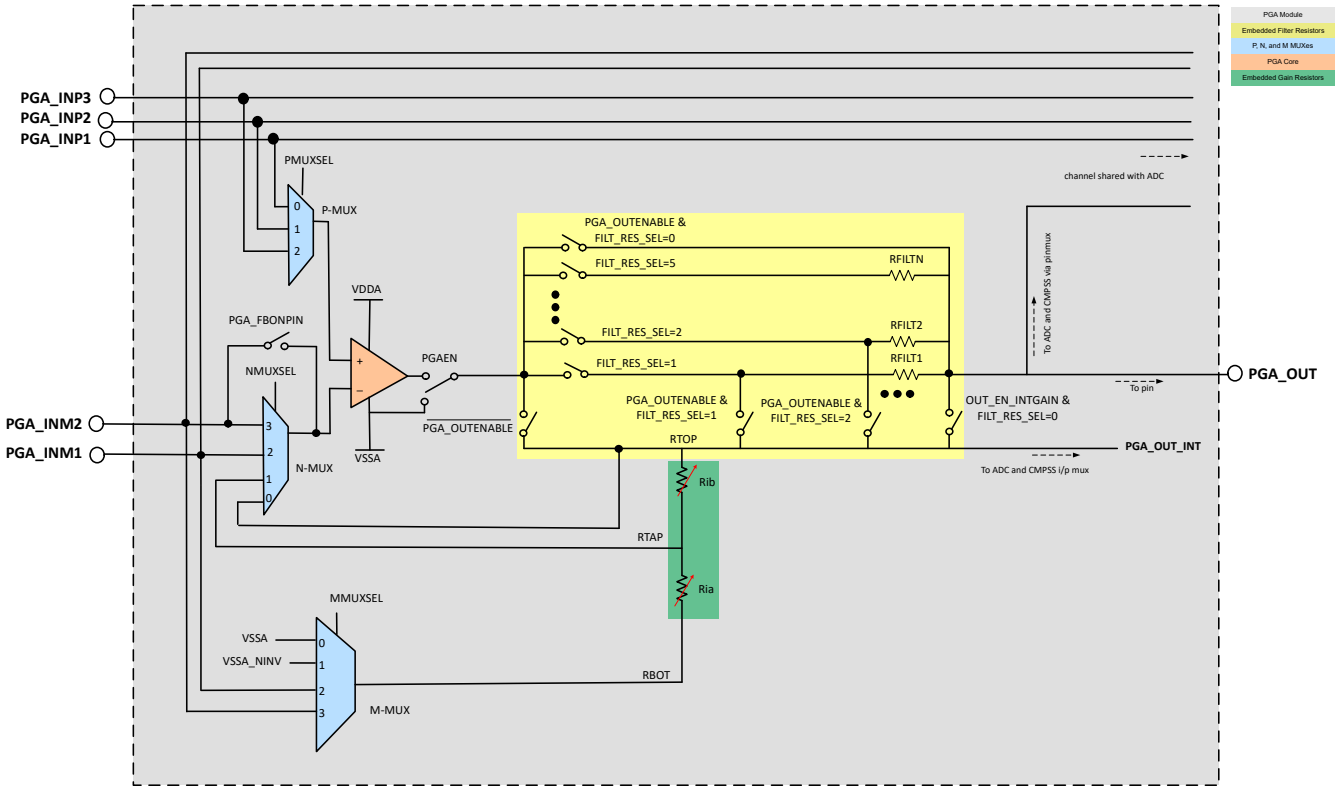


Figure 6-46. PGA Block Diagram

6.11.4.1 PGA Electrical Data and Timing

6.11.4.1.1 PGA Operating Conditions

over recommended operating s (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGA Output Range(1)		VSSA+0.025		VDDA–0.025	V
Cap Load on PGA Out			40		pF

(1) This is the linear output range of the PGA. The PGA can output voltages outside this range, but the voltages will not be linear.

6.11.4.1.2 PGA Characteristics

over recommended operating s (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General					
Min ADC S+H Settling within ±1 ADC LSB Accuracy (No Filter; All Gain Settings; Single ADC Driven) (4)	Gain = 1	125			ns
	Gain = 2/-1	146			
	Gain = 4/-3	125			
	Gain = 8/-7	154			
	Gain = 16/-15	227			
	Gain = 32/-31	322			
	Gain = 64/-63	420			
Gain Settings			1		
			2, 4, 8, 16, 32, 64		
			–1, –3, –7, –15, –31, –63		
Short Circuit Current (5)			41		mA
Full Scale Step Response (No Filter) Settling within 0.05% Accuracy(4)	G<64			420	ns
	G = 64/-63			500	ns
Settling Time: Gain Switching				10	µs
Slew Rate	Naked OPA Mode		12		V/µs
Slew Rate	Gain = 1		12		V/µs
	Gain = 2/-1		24		V/µs
	Gain = 4/-3		43		V/µs
	Gain = 8/-7		67		V/µs
	Gain = 16/-15		35		V/µs
	Gain = 32/-31		29		V/µs
	Gain = 64/-63		26		V/µs
R_{ia}	Gain = 1		256		kΩ
	Gain = 2/-1		14		kΩ
	Gain = 4/-3		7		kΩ
	Gain = 8/-7		8		kΩ
	Gain = 16/-15		8		kΩ
	Gain = 32/-31		8		kΩ
	Gain = 64/-63		4		kΩ

ADVANCE INFORMATION

6.11.4.1.2 PGA Characteristics (continued)

over recommended operating s (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ib}	Gain = 1		0		kΩ
	Gain = 2/-1		14		kΩ
	Gain = 4/-3		21		kΩ
	Gain = 8/-7		56		kΩ
	Gain = 16/-15		120		kΩ
	Gain = 32/-31		248		kΩ
	Gain = 64/-63		252		kΩ
Filter Resistor Targets	R_{FILT} = 800 Ω		800		Ω
	R_{FILT} = 400 Ω		400		Ω
	R_{FILT} = 200 Ω		200		Ω
	R_{FILT} = 100 Ω		100		Ω
	R_{FILT} = 50 Ω		50	62	Ω
Gain Bandwidth Product (Naked Op-Amp Mode)	Gain=1		7		MHz
Closed Loop -3bd BW	Gain=1		15		MHz
	Gain=2/-1		14		MHz
	Gain=4/-3		13.5		MHz
	Gain=8/-7		12		MHz
	Gain=16/-15		11		MHz
	Gain=32/-31		5.5		MHz
	Gain=64/-63		5.0		MHz
DC Characteristics					
Gain Error(1)	Gain = 1	–0.18		0.18	%
Gain Error(1)	Gain = 2, -1	–0.37		0.37	%
Gain Error(1)	Gain = 4, -3	–0.6		0.6	%
Gain Error(1)	Gain = 8, -7	–0.73		0.73	%
Gain Error(1)	Gain = 16, -15	–0.81		0.81	%
Gain Error(1)	Gain = 32, -31	–1.0		1.0	%
Gain Error(1)	Gain = 64, -63	–1.82		1.82	%
Offset Error(2)	Input Referred	–3.0	+/–1.0	3.0	mV
Offset Temp Coefficient	Input Referred	–7.0		7.0	µV/C
Offset Error - Chopped		–0.8		0.8	mV
Offset Temp Coefficient - Chopped			0.3		µV/C
DC Code Spread	G<64		2.5		12b LSB
	G = 64/-63		4		12b LSB
AC Characteristics					
Phase Margin Naked OPA	C_{load} = 40pF G=1		45		Deg
Aol (Open loop voltage gain) Naked OPA	R_L=7.5kΩ to GND 0.3V<V_O<VDDA-0.3V		94		dB
THD + Noise (THD+N) Naked OPA	f_{in}=1kHz G=1		82		dB

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6.11.4.1.2 PGA Characteristics (continued)

over recommended operating s (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR 10kHz (With ADC)	Gain = 1		68		dB
	Gain = 2, -1		68		
	Gain = 4, -3		66		
	Gain = 8, -7		62		
	Gain = 16, -15		58		
	Gain = 32, -31		55		
	Gain = 64, -63		51		
THD(3)	DC		–78		dB
THD(Up to 100kHz) (3)	Gain = 1		–58		dB
	Gain = 2, -1		–70		
	Gain = 4, -3		–70		
	Gain = 8, -7		–70		
	Gain = 16, -15		–70		
	Gain = 32, -31		–58		
	Gain = 64, -63		–58		
CMRR	DC: V_{IN} <=1.5V		–86		dB
	DC: Full Input Range		–77		dB
	Up to 100 kHz		–50		dB
PSRR(3)	DC		–75		dB
	Up to 10 kHz		–60		dB
	Up to 100 kHz		–40		dB
Noise PSD(3)	1 kHz		200		nV/sqrt(Hz)
	10 kHz		100		nV/sqrt(Hz)
Integrated Noise (Input Referred)(3)	3 Hz to 30 MHz		100		µV

(1) Includes ADC gain error.
(2) Includes ADC offset error.
(3) Performance of PGA alone.
(4) Step response time w filter = tS+H + 7.6*R_{filt}* C_{filt}
(5) Assumes no filter circuit

ADVANCE INFORMATION

6.11.5 Temperature Sensor

6.11.5.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in the *Temperature Sensor Characteristics* table.

6.11.5.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{acc}	Temperature Accuracy	Internal reference (-40°C to 30°C)	-15	±2	15	°C
		Internal reference (30°C to 85°C)	-9	±2	7	°C
		Internal reference (85°C to 125°C)	-5	±2	8	°C
		External reference (-40°C to 30°C)	-8	±2	10	°C
		External reference (30°C to 125°C)	-5	±2	8	°C
$t_{startup}$	Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor)			500		µs
t_{acq}	ADC acquisition time		450			ns

ADVANCE INFORMATION

6.12 Control Peripherals

6.12.1 Multichannel Pulse Width Modulator (MCPWM)

The MCPWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The MCPWM module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the MCPWM module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The MCPWM and eCAP synchronization scheme on the device provides flexibility in partitioning the MCPWM and eCAP modules and allows localized synchronization within the modules.

Figure 6-47 shows the MCPWM module.

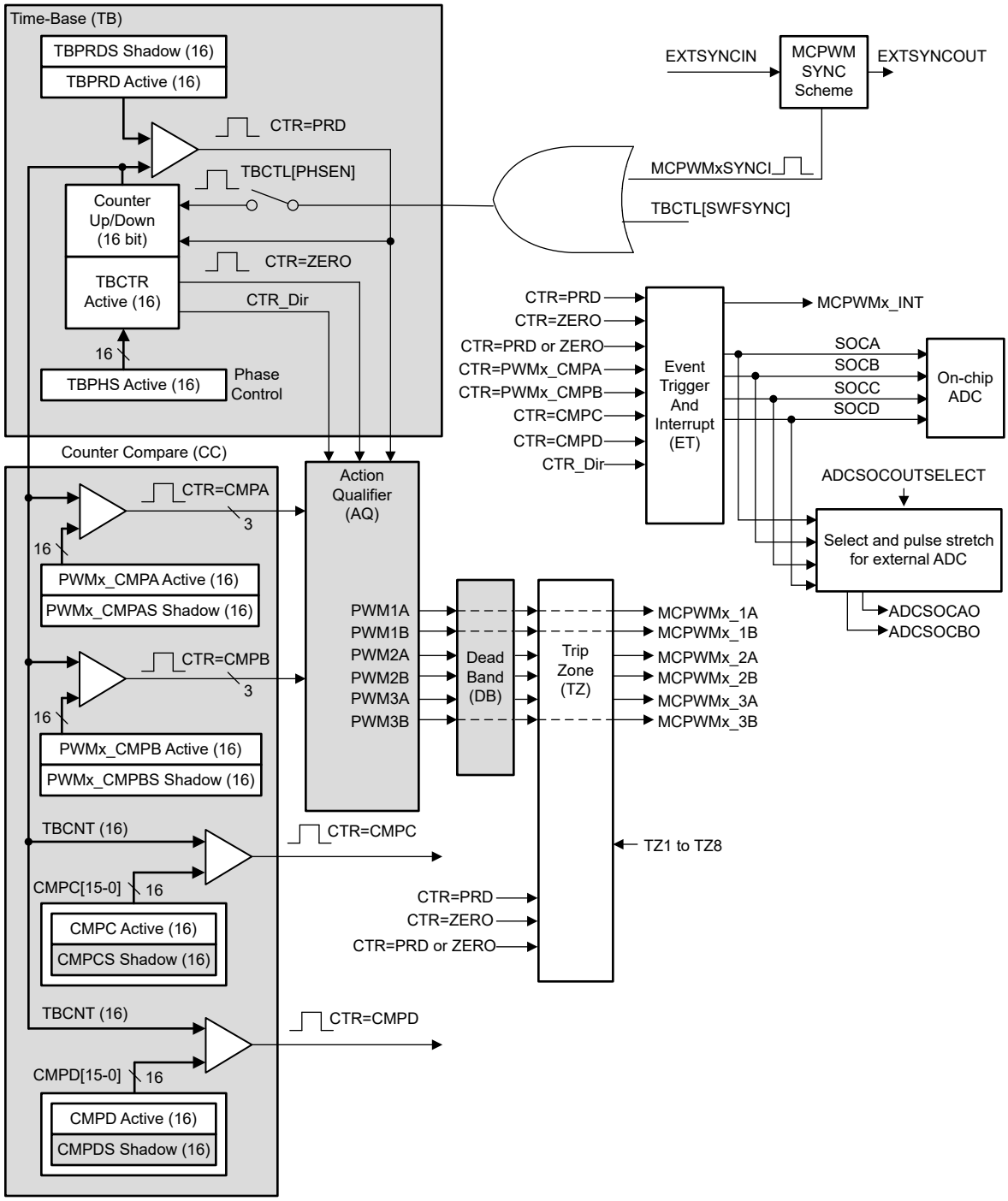

Figure 6-47. MCPWM Submodules and Critical Internal Signal Interconnects

6.12.1.1 Control Peripherals Synchronization

The MCPWM and eCAP synchronization scheme on the device provides flexibility in partitioning the MCPWM and eCAP modules and allows localized synchronization within the modules. Figure 6-48 shows the synchronization scheme.

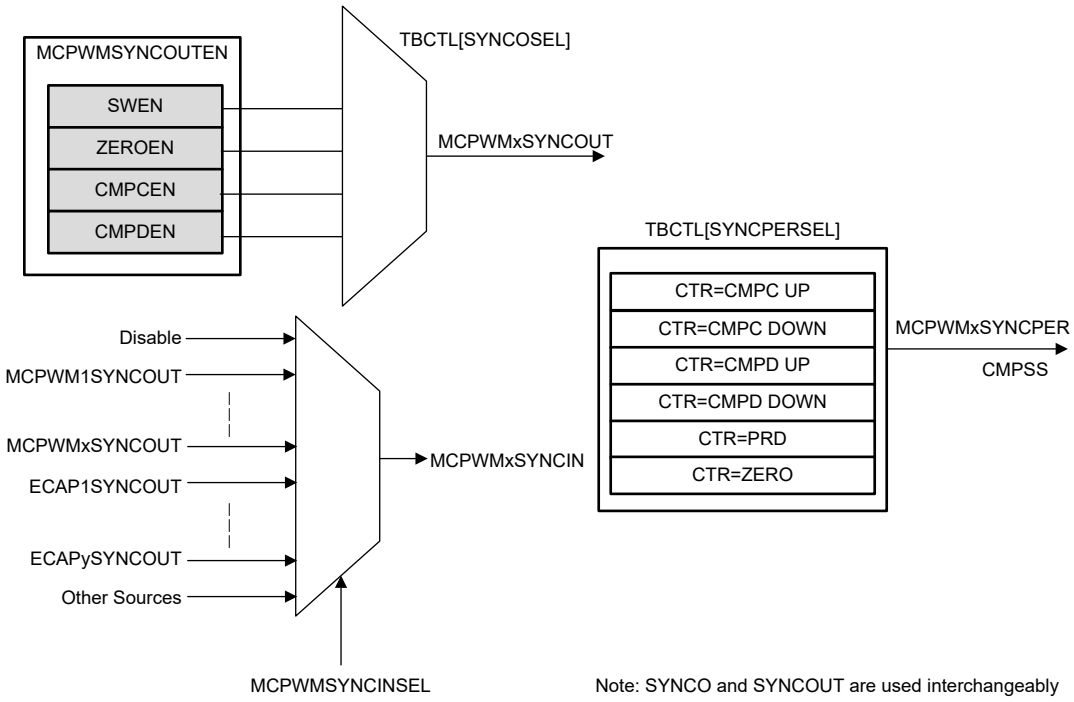

Figure 6-48. Synchronization Chain Architecture

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6.12.1.2 MCPWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.12.1.2.1 MCPWM Timing Requirements

			MIN	MAX	UNIT
$t_{w(SYNCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(MCPWMCLK)}$		cycles
		Synchronous	$2t_{c(MCPWMCLK)}$		
		With input qualifier	$1t_{c(MCPWMCLK)} + t_{w(IQSW)}$		

6.12.1.2.2 MCPWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

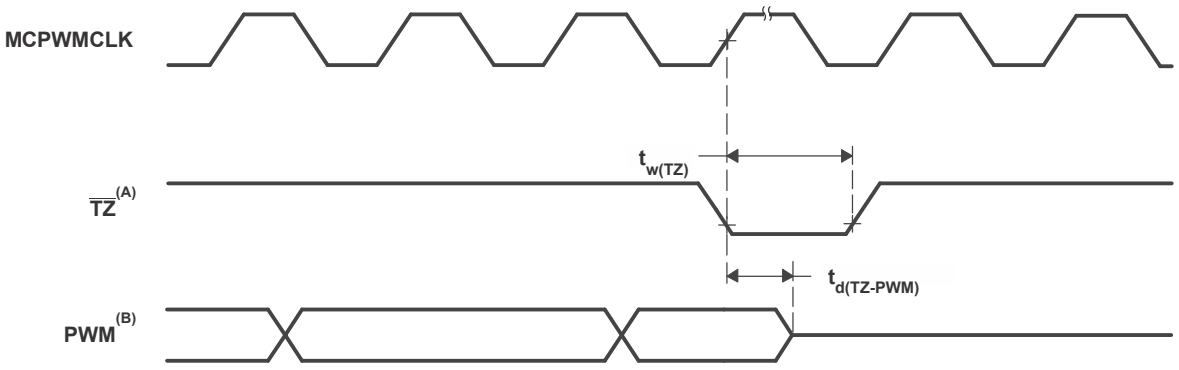
PARAMETER[1]		MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low	20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width	$8t_{c(SYSCLK)}$		cycles
$t_{d(TZ-PWM)}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low Delay time, trip input active to PWM Hi-Z		25	ns

(1) 20-pF load on pin.

6.12.1.2.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.12.1.2.3.1 PWM Hi-Z Characteristics Timing Diagram



A. $\overline{TZ}$: $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-49. PWM Hi-Z Characteristics

6.12.2 External ADC Start-of-Conversion Electrical Data and Timing

6.12.2.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(SYSCLK)}$		cycles

6.12.2.2 $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing Diagram

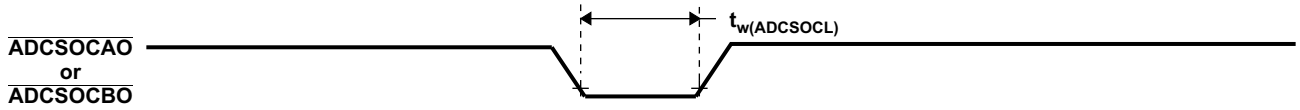


Figure 6-50. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

ADVANCE INFORMATION

6.12.3 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 6-51):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

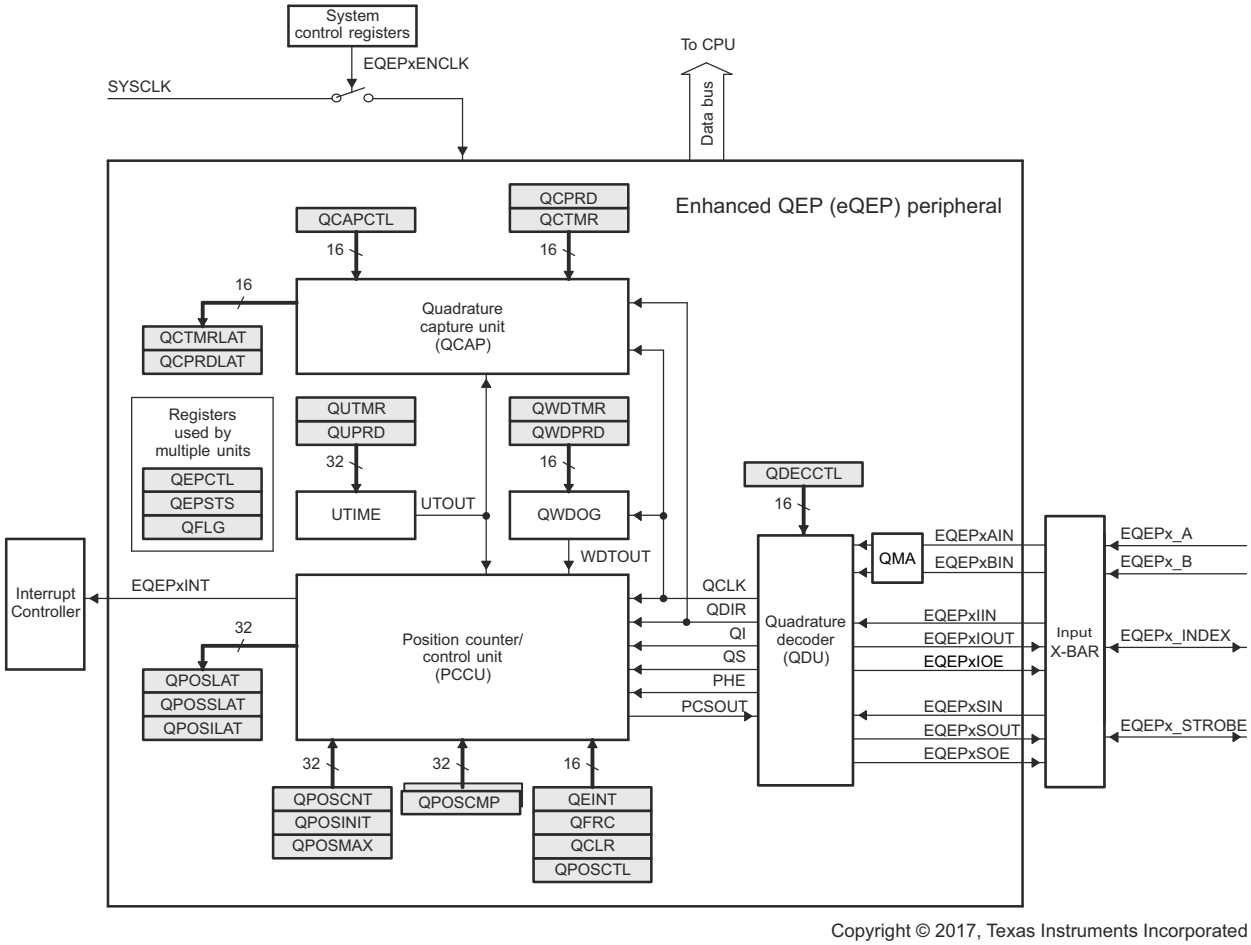


Figure 6-51. eQEP Block Diagram

6.12.3.1 eQEP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.12.3.1.1 eQEP Timing Requirements

			MIN	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$		
$t_{w(INDEXH)}$	QEP Index Input High time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(INDEXL)}$	QEP Index Input Low time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBH)}$	QEP Strobe High time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		
$t_{w(STROBL)}$	QEP Strobe Input Low time	Synchronous[1]	$2t_{c(SYSCLK)}$		cycles
		Synchronous with input qualifier	$2t_{c(SYSCLK)} + t_{w(IQSW)}$		

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.12.3.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$5t_{c(SYSCLK)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$7t_{c(SYSCLK)}$	cycles

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6.12.4 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this section include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
  - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
  - The modulo counter (ECCTL2 [MODCNTRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- DMA trigger source
  - eCAPxDMA was added as a DMA trigger. CEVT[1-4] can be configured as the source for eCAPxDMA.
- Input multiplexer
  - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the *Configuring Device Pins for the eCAP* section of the Enhanced Capture (eCAP) chapter in the *F28E12x Real-Time Microcontrollers Technical Reference Manual* .
- EALLOW protection
  - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
  - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

6.12.4.1 eCAP Block Diagram

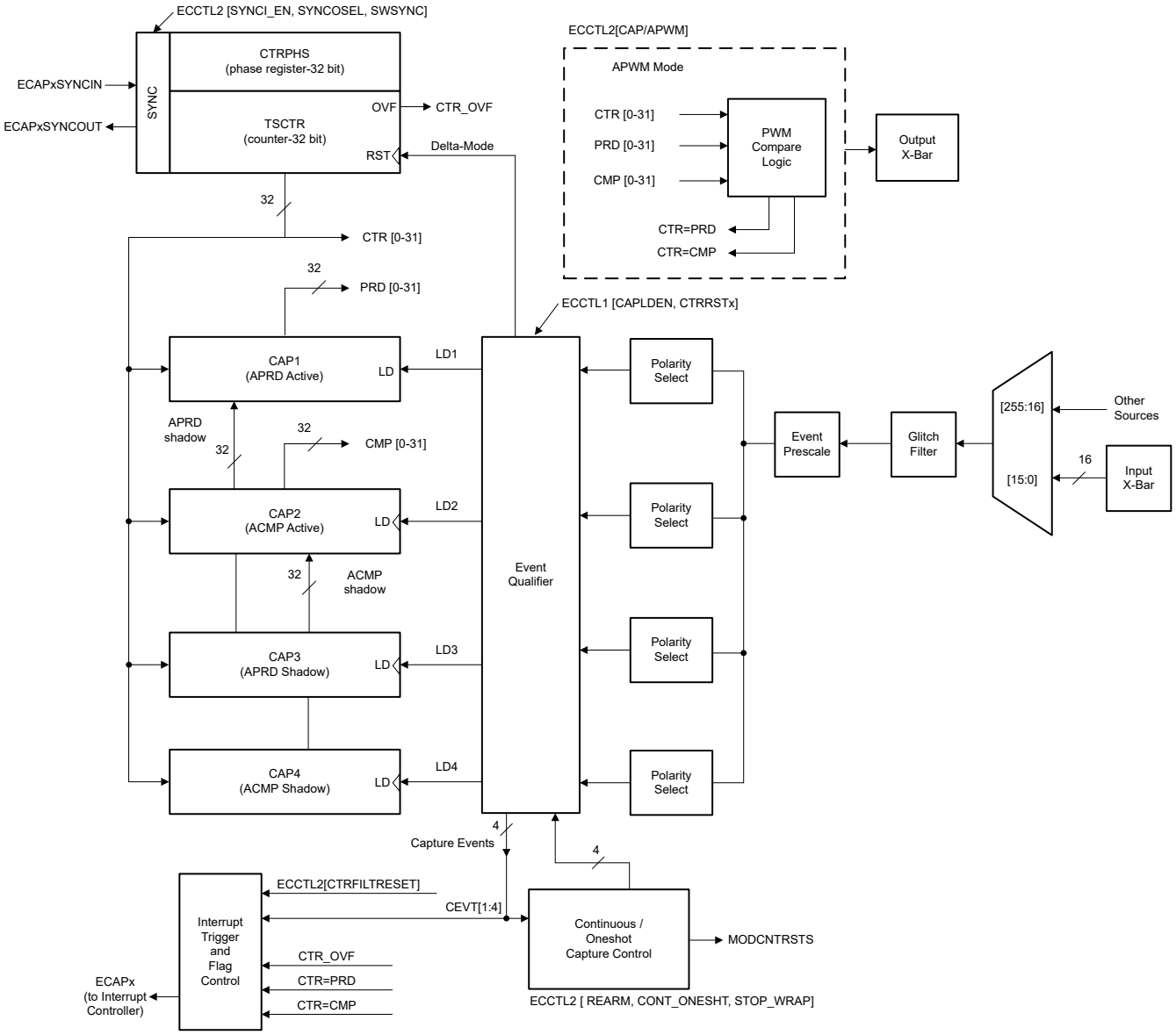

Figure 6-52. eCAP Block Diagram

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6.12.4.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from MCPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-53.

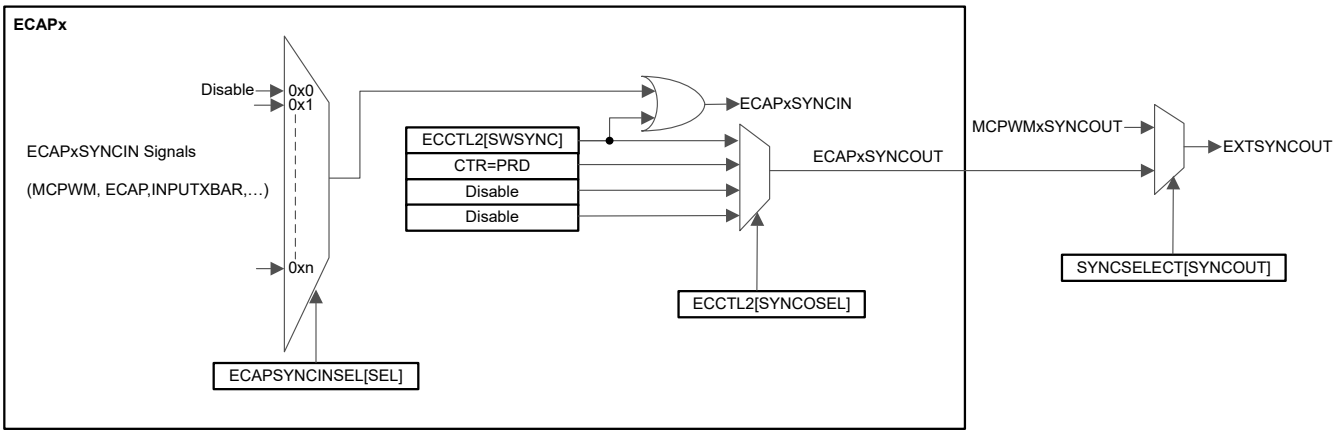

Figure 6-53. eCAP Synchronization Scheme

6.12.4.3 eCAP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.12.4.3.1 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20			ns

6.13 Communications Peripherals

6.13.1 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I^2C-bus specification (version 2.1):
  - Support for 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple controller-transmitters and target-receivers
  - Support for multiple target-transmitters and controller-receivers
  - Combined controller transmit/receive and receive/transmit mode
  - Data transfer rate from 10Kbps up to 400Kbps (Fast-mode)
- Supports voltage thresholds compatible to:
  - SMBus 3.0 and below
  - PMBus 1.3 and below
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two interrupts
  - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
    - Transmit Ready
    - Receive Ready
    - Register-Access Ready
    - No-Acknowledgment
    - Arbitration-Lost
    - Stop Condition Detected
    - Addressed-as-Target
  - I2Cx_FIFO interrupts:
    - Transmit FIFO interrupt
    - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-54 shows how the I2C peripheral module interfaces within the device.

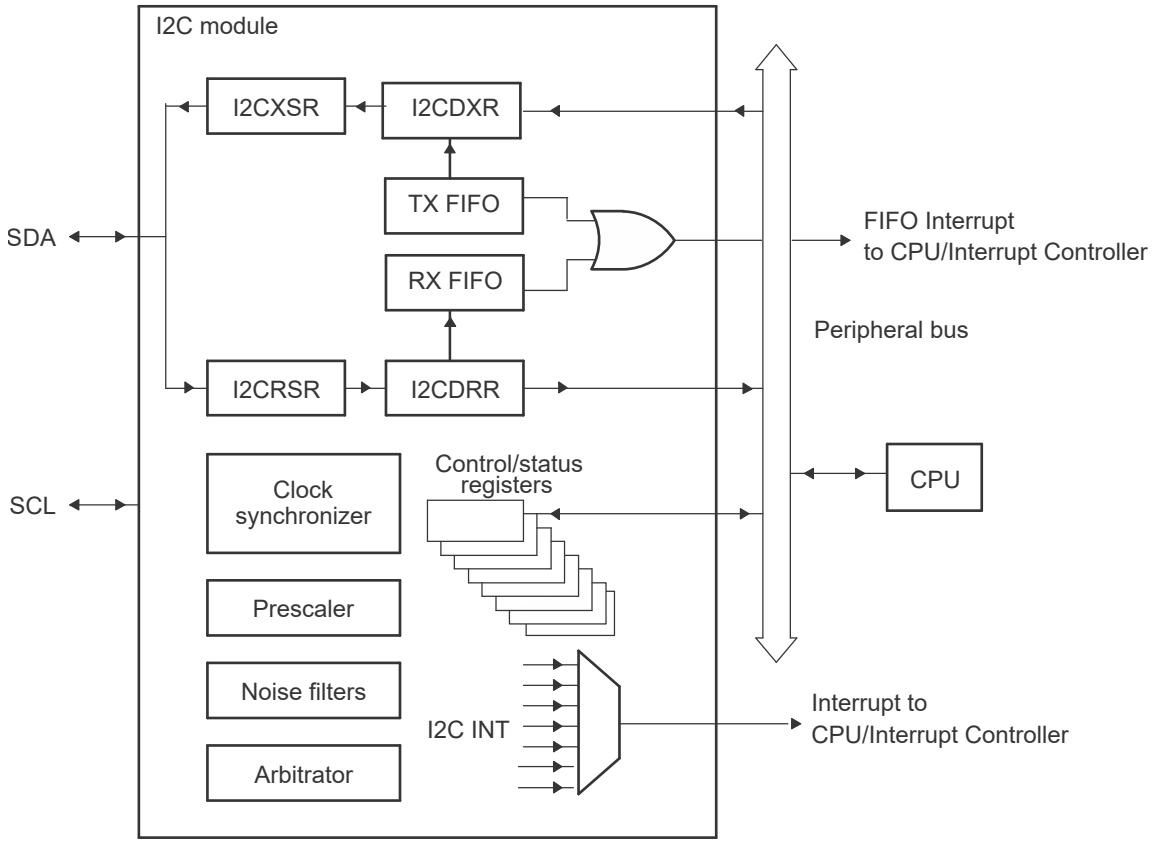

Figure 6-54. I2C Peripheral Module Interfaces

6.13.1.1 I2C Electrical Data and Timing

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the *I2C Bus Pullup Resistor Calculation* Application Note.

6.13.1.1.1 I2C Timing Requirements

NO.			MIN	MAX	UNIT
Standard mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	4.0		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	4.0		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	250		ns
T5	$t_{r(SDA)}$	Rise time, SDA		1000	ns
T6	$t_{r(SCL)}$	Rise time, SCL		1000	ns
T7	$t_{f(SDA)}$	Fall time, SDA		300	ns
T8	$t_{f(SCL)}$	Fall time, SCL		300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	4.0		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF
Fast mode					
T0	f_{mod}	I2C module frequency	7	12	MHz
T1	$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall	0.6		µs
T2	$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay	0.6		µs
T3	$t_{h(SCL-DAT)}$	Hold time, data after SCL fall	0		µs
T4	$t_{su(DAT-SCL)}$	Setup time, data before SCL rise	100		ns
T5	$t_{r(SDA)}$	Rise time, SDA	20	300	ns
T6	$t_{r(SCL)}$	Rise time, SCL	20	300	ns
T7	$t_{f(SDA)}$	Fall time, SDA	11.4	300	ns
T8	$t_{f(SCL)}$	Fall time, SCL	11.4	300	ns
T9	$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay	0.6		µs
T10	$t_{w(SP)}$	Pulse duration of spikes that will be suppressed by filter	0	50	ns
T11	C_b	capacitance load on each bus line		400	pF

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6.13.1.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
Standard mode						
S1	f_{SCL}	SCL clock frequency		0	100	kHz
S2	T_{SCL}	SCL clock period		10		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		4.7		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		4.0		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		4.7		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			3.45	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			3.45	µs
	V_{IL}	Valid low-level input voltage		–0.3	0.3 * V_{DDIO}	V
	V_{IH}	Valid high-level input voltage		0.7 * V_{DDIO}	V_{DDIO} + 0.3	V
	V_{OL}	Low-level output voltage	Sinking 3 mA	0	0.4	V
S8	I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA
Fast mode						
S1	f_{SCL}	SCL clock frequency		0	400	kHz
S2	T_{SCL}	SCL clock period		2.5		µs
S3	$t_{w(SCLL)}$	Pulse duration, SCL clock low		1.3		µs
S4	$t_{w(SCLH)}$	Pulse duration, SCL clock high		0.6		µs
S5	t_{BUF}	Bus free time between STOP and START conditions		1.3		µs
S6	$t_{v(SCL-DAT)}$	Valid time, data after SCL fall			0.9	µs
S7	$t_{v(SCL-ACK)}$	Valid time, Acknowledge after SCL fall			0.9	µs
	V_{IL}	Valid low-level input voltage		–0.3	0.3 * V_{DDIO}	V
	V_{IH}	Valid high-level input voltage		0.7 * V_{DDIO}	V_{DDIO} + 0.3	V
	V_{OL}	Low-level output voltage	Sinking 3 mA	0	0.4	V
S8	I_I	Input current on pins	0.1 V_{bus} < V_i < 0.9 V_{bus}	–10	10	µA

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6.13.1.1.3 I2C Timing Diagram

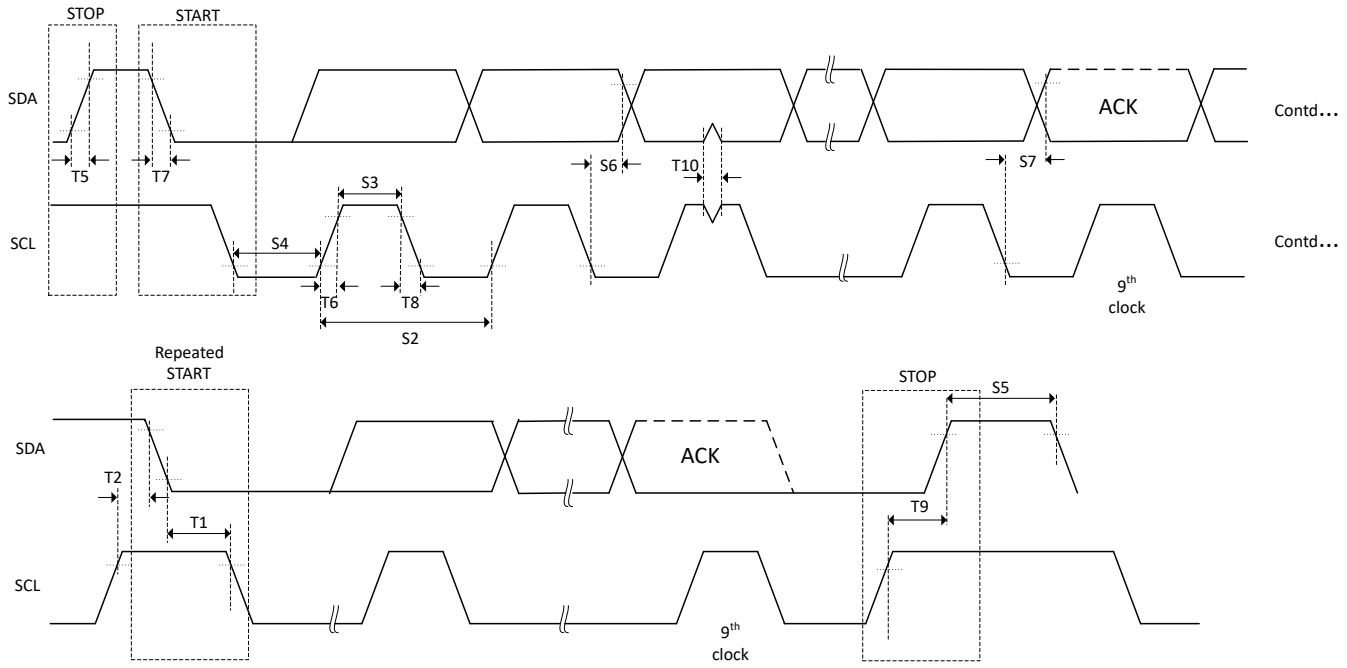

Figure 6-55. I2C Timing Diagram

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6.13.2 Universal Asynchronous Receiver-Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter (UART) module in this device contains the following features:

- Programmable baud-rate generator allowing speeds of up to 10Mbps for regular speed (divide by 16) and 20Mbps for high speed (divide by 8)
- Separate 16-level-deep and 8-bit-wide transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
- Programmable FIFO length, including 1-byte-deep operation providing conventional double-buffered interface (non-FIFO mode)
- FIFO trigger levels of 1/16, ⅛, 3/16, ½, 5/16, 3/8, 7/16, ½, 9/16, 5/8, 11/16, 3/4, 13/16, ⅞ and 15/16
- Standard asynchronous communication bits for start, stop, and parity
- Line-break generation and detection
- Fully programmable serial interface characteristics
  - 5, 6, 7, or 8 data bits
  - Even, odd, stick, or no parity-bit generation and detection
  - 1 or 2 stop-bit generation
- IrDA serial-IR (SIR) encoder and decoder providing:
  - Programmable use of IrDA SIR or UART input/output
  - Support of IrDA SIR encoder and decoder functions for data rates of up to 115.2Kbps half-duplex
  - Support of normal 3/16 and low-power (1.41 to 2.23 µs) bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power-mode bit duration
- EIA-485 9-bit support
- Standard FIFO-level and End-of-Transmission (EOT) interrupts
- Efficient transfers using Direct Memory Access (DMA) Controller
  - Separate channels for transmit and receive
  - Receive burst request asserted at programmed FIFO level
  - Transmit burst request asserted at programmed FIFO level

Figure 6-56 shows the UART module block diagram.

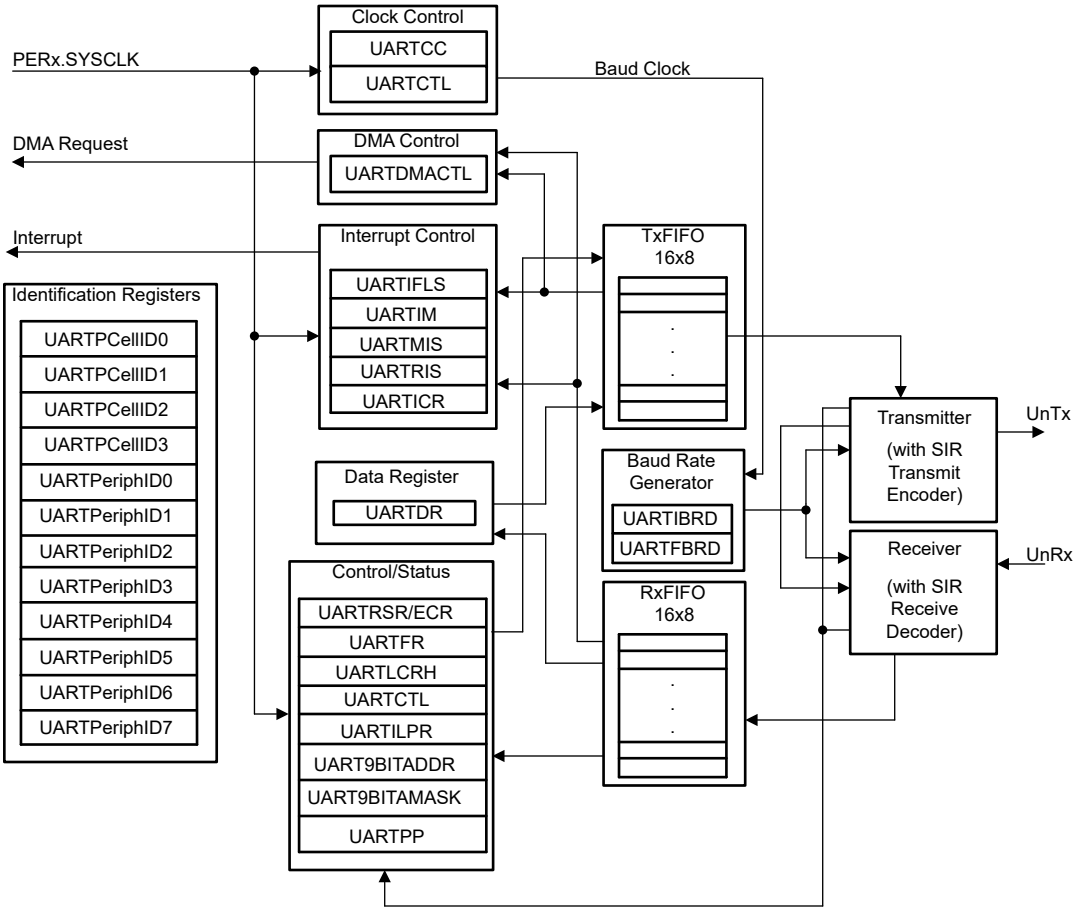

Figure 6-56. UART Module Block Diagram

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6.13.3 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the controller or peripheral operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPIPOCI: SPI peripheral-output/controller-input pin
- SPIPICO: SPI peripheral-input/controller-output pin
- $\overline{\text{SPIPTE}}$: SPI peripheral transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Controller and Peripheral
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- DMA support
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- $\overline{\text{SPIPTE}}$ inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-57 shows the SPI CPU interfaces.

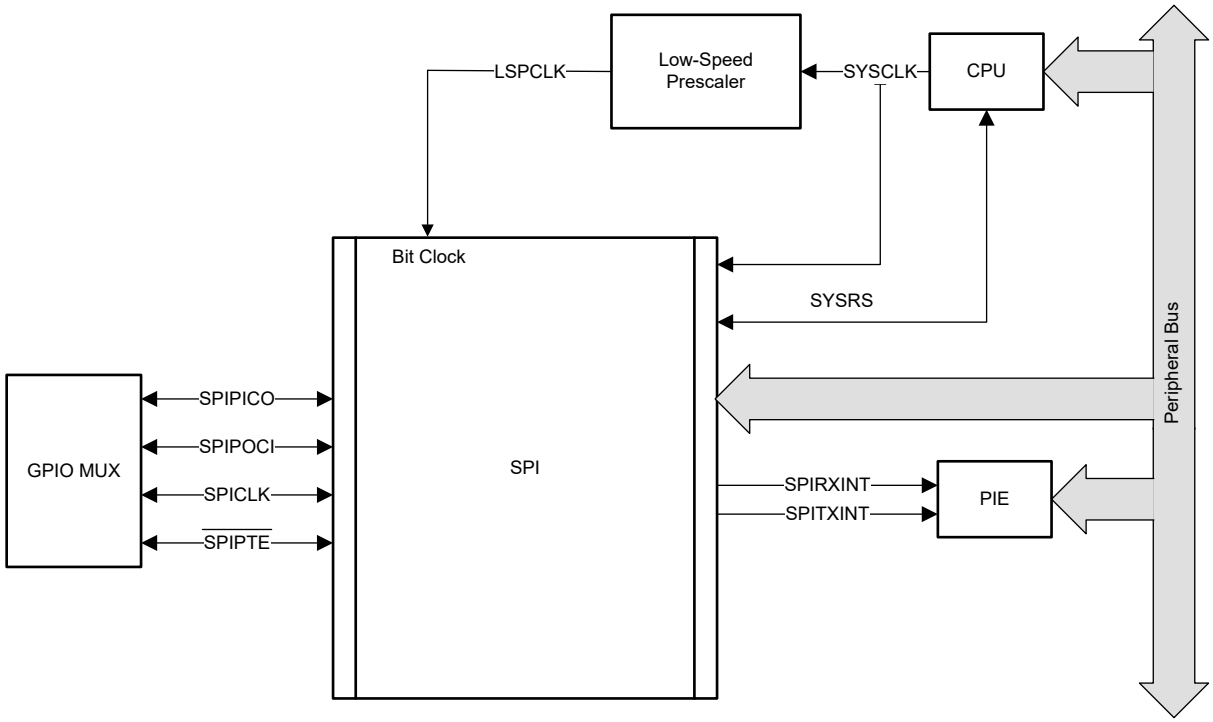

Figure 6-57. SPI CPU Interface

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6.13.3.1 SPI Controller Mode Timings

The following sections contain the SPI Controller Mode timings.

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5pF on SPICLK, SPIPICO, and SPIPOCI. In HS_MODE, a maximum clock of 50MHz is supported.

6.13.3.1.1 SPI Controller Mode Timing Requirements

NO.			(BRR + 1) (1)	MIN	MAX	UNIT
High-Speed Mode						
8	$t_{su(POCI)M}$	Setup time, SPIPOCI valid before SPICLK	Even, Odd	1		ns
9	$t_{h(POCI)M}$	Hold time, SPIPOCI valid after SPICLK	Even, Odd	6.5		ns
Normal Mode						
8	$t_{su(POCI)M}$	Setup time, SPIPOCI valid before SPICLK	Even, Odd	15		ns
9	$t_{h(POCI)M}$	Hold time, SPIPOCI valid after SPICLK	Even, Odd	0		ns

(1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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6.13.3.1.2 SPI Controller Mode Switching Characteristics - Clock Phase 0

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER(1) (2)		(BRR + 1)(3)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPISTE}$ active to SPICLK	Even	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
			Odd	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$	$1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$	
24	$t_{v(STE)M}$	Valid time, SPICLK to $\overline{SPISTE}$ inactive	Even	$0.5t_{c(SPC)M} - 3$	$0.5t_{c(SPC)M} + 3$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$	
High-Speed Mode						
4	$t_{d(PICO)M}$	Delay time, SPICLK to SPIPICO valid	Even, Odd		1	ns
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
Normal Mode						
4	$t_{d(PICO)M}$	Delay time, SPICLK to SPIPICO valid	Even, Odd		2	ns
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	0.5tc(SPC)M – 0.5tc(LSPCLK) – 3		

(1) 10-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.
(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

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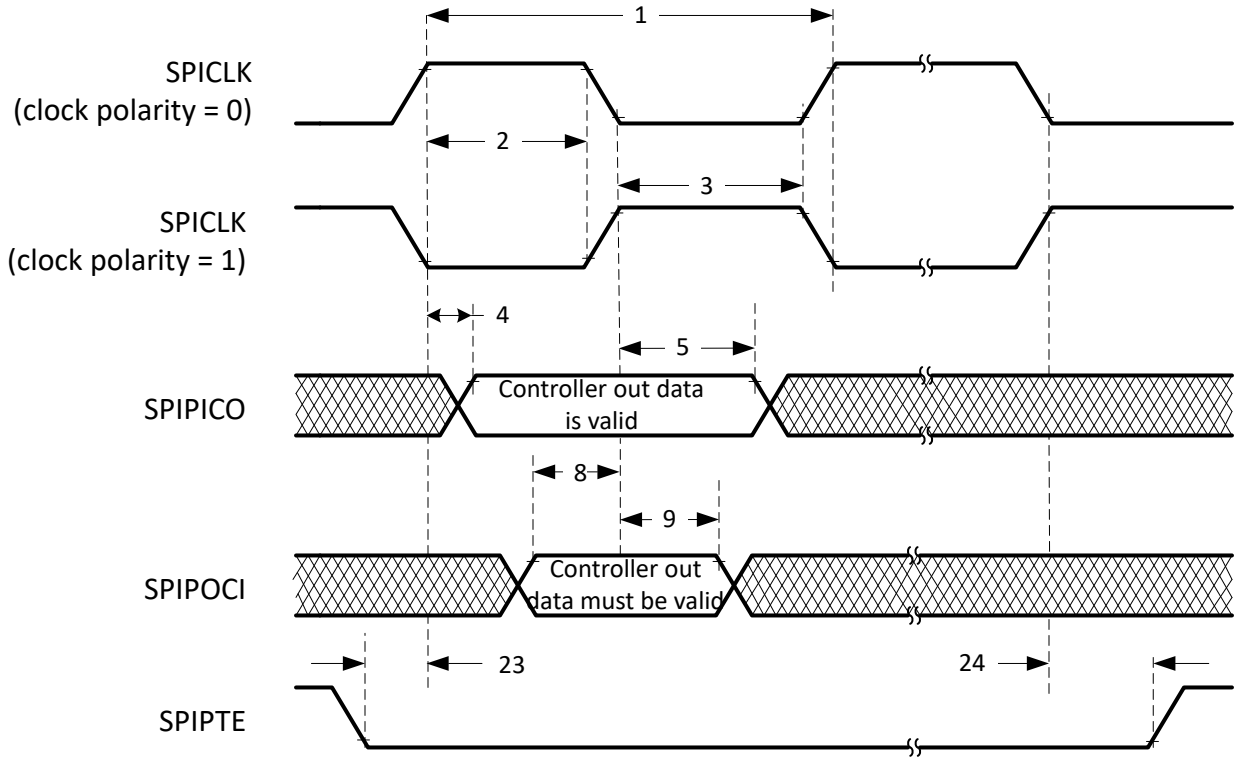
6.13.3.1.3 SPI Controller Mode Switching Characteristics - Clock Phase 1

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[1] [2]		(BRR + 1)	MIN	MAX	UNIT
General						
1	$t_{c(SPC)M}$	Cycle time, SPICLK	Even	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	ns
			Odd	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK, first pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$	
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK, second pulse	Even	$0.5t_{c(SPC)M} - 1$	$0.5t_{c(SPC)M} + 1$	ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$	
23	$t_{d(SPC)M}$	Delay time, $\overline{SPISTE}$ valid to SPICLK	Even, Odd	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$	ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{SPISTE}$ invalid	Even	–3	3	ns
			Odd	–3	3	
High-Speed Mode						
4	$t_{d(PICO)M}$	Delay time, SPIPICO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$		
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		
Normal Mode						
4	$t_{d(PICO)M}$	Delay time, SPIPICO valid to SPICLK	Even	$0.5t_{c(SPC)M} - 2$		ns
			Odd	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$		
5	$t_{v(PICO)M}$	Valid time, SPIPICO valid after SPICLK	Even	$0.5t_{c(SPC)M} - 3$		ns
			Odd	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$		

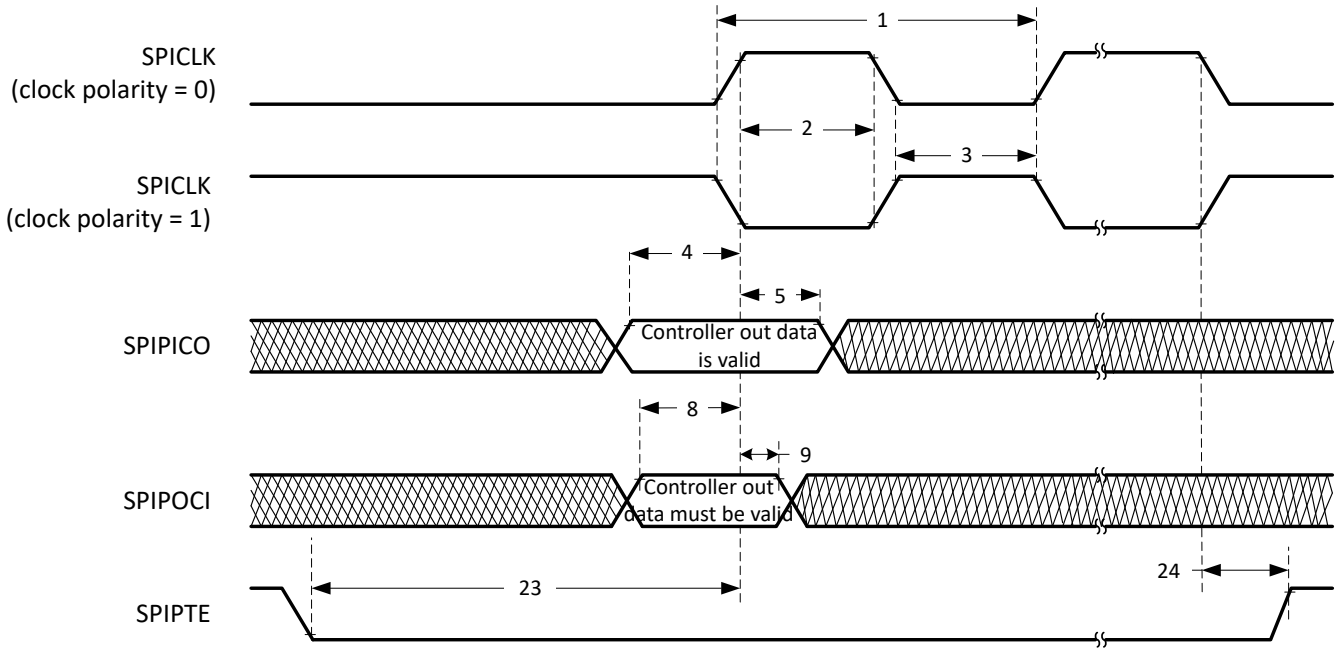
(1) 10-pF load on pin for High-Speed Mode.
(2) 20-pF load on pin for Normal Mode.

6.13.3.1.4 SPI Controller Mode Timing Diagrams



A. On the trailing end of the word, SPIPTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-58. SPI Controller Mode External Timing (Clock Phase = 0)



A. On the trailing end of the word, SPIPTE will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-59. SPI Controller Mode External Timing (Clock Phase = 1)

ADVANCE INFORMATION

6.13.3.2 SPI Peripheral Mode Timings

The following sections contain the SPI Peripheral Mode timings.

6.13.3.2.1 SPI Peripheral Mode Timing Requirements

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK, first pulse	$2t_{c(SYSCLK)} – 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK, second pulse	$2t_{c(SYSCLK)} – 1$		ns
19	$t_{su(PICO)S}$	Setup time, SPIPICO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(PICO)S}$	Hold time, SPIPICO valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 0)	$2t_{c(SYSCLK)} + 15$		ns
		Setup time, $\overline{\text{SPISTE}}$ valid before SPICLK (Clock Phase = 1)	$2t_{c(SYSCLK)} + 15$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ invalid after SPICLK	$1.5t_{c(SYSCLK)}$		ns

6.13.3.2.2 SPI Peripheral Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER(1)		MIN	MAX	UNIT
Normal Mode					
15	$t_{d(POCI)S}$	Delay time, SPICLK to SPIPOCI valid		12.5	ns
16	$t_{v(POCI)S}$	Valid time, SPIPOCI valid after SPICLK	0		ns
High-Speed Mode					
15	$t_{d(POCI)S}$	Delay time, SPICLK to SPIPOCI valid		12.5	ns
16	$t_{v(POCI)S}$	Valid time, SPIPOCI valid after SPICLK	0		ns

(1) 20-pF load on pin.

6.13.3.2.3 SPI Peripheral Mode Timing Diagrams

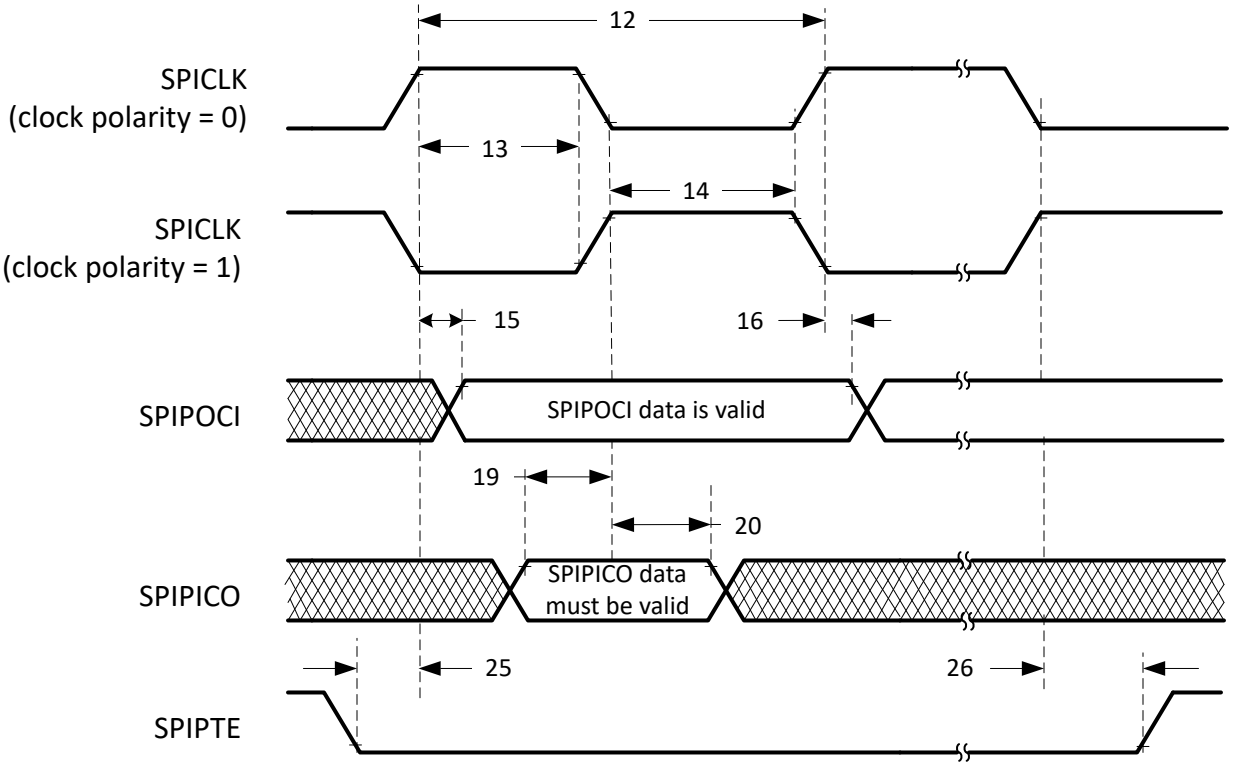


Figure 6-60. SPI Peripheral Mode External Timing (Clock Phase = 0)

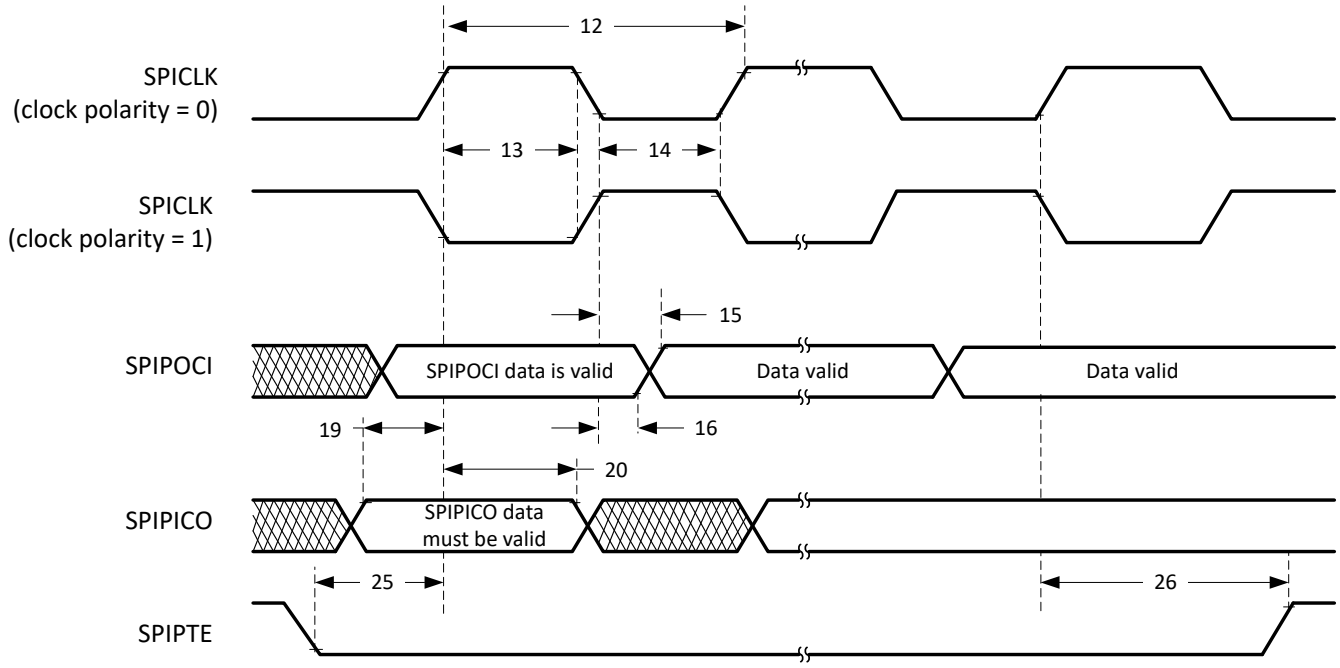


Figure 6-61. SPI Peripheral Mode External Timing (Clock Phase = 1)

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6.13.4 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
  - Baud rate programmable to 64K different rates
- Data-word format
  - 1 start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half-duplex or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Figure 6-62 shows the SCI block diagram.

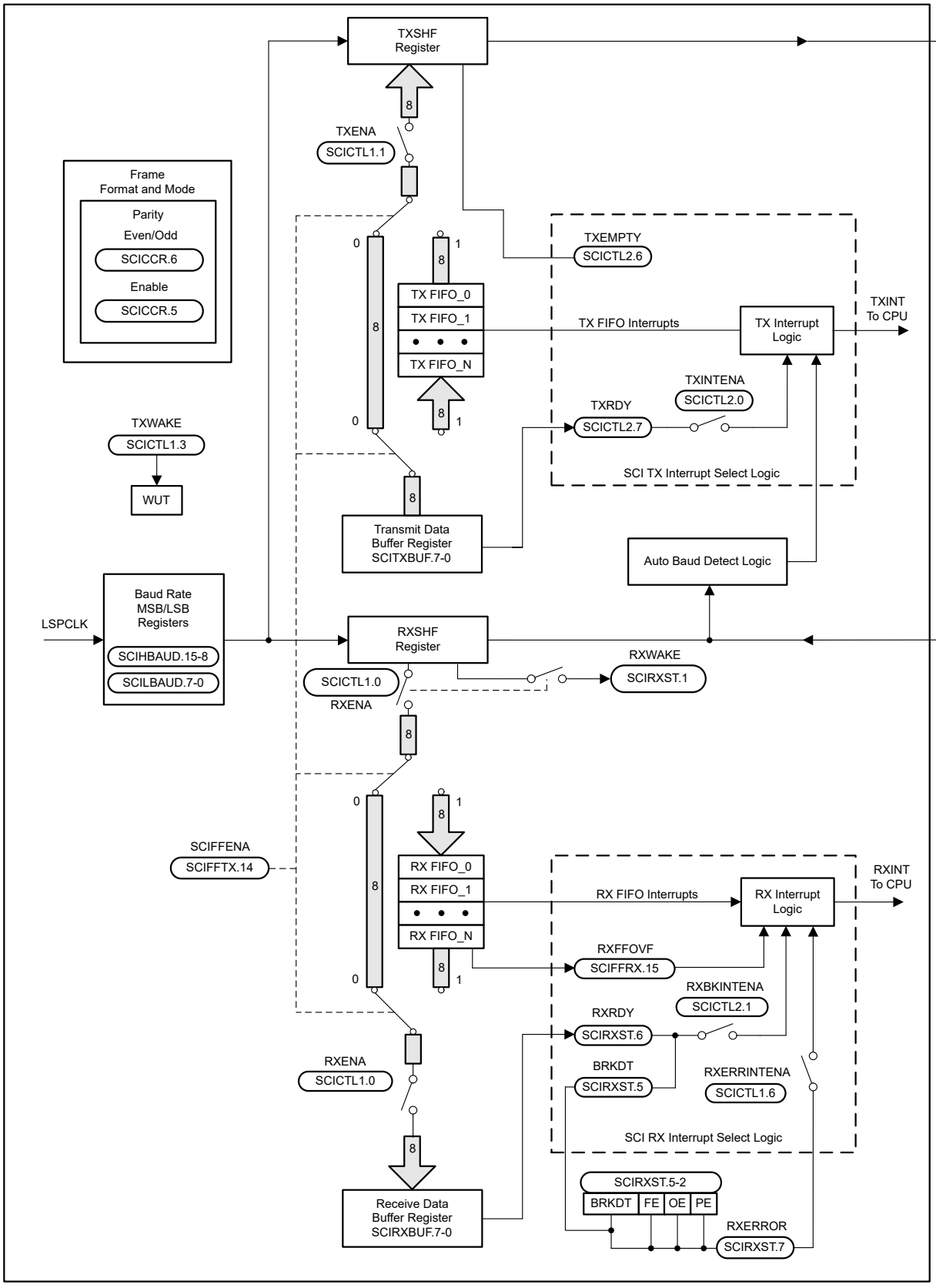

Figure 6-62. SCI Block Diagram

ADVANCE INFORMATION

7 Detailed Description

7.1 Memory

7.1.1 C28x Memory Map

Table 7-1. Memory Map

MEMORY	SIZE (x16)	START ADDRESS	END ADDRESS	CPU1.DMA ACCESS	ECC/ Parity	SECURITY	PART NUMBER
M0 RAM	1024	0x0000_0000	0x0000_03FF	-	Parity	-	-
M1 RAM	1024	0x0000_0400	0x0000_07FF	-	Parity	-	-
PIE Vector Table	160	0x0000_0D00	0x0000_0D9F	-	Parity	-	-
GS0_1 RAM (with Parity)	1024	0x0000_C000	0x0000_C3FF	YES	Parity	-	-
GS0_2 RAM (with Parity)	1024	0x0000_C400	0x0000_C7FF	YES	Parity	-	-
GS0_3 RAM (with Parity)	1024	0x0000_C800	0x0000_CBFF	YES	Parity	-	-
GS0_4 RAM (with Parity)	1024	0x0000_CC00	0x0000_CFFF	YES	Parity	-	-
GS0_5 RAM (with Parity)	1024	0x0000_D000	0x0000_D3FF	YES	Parity	-	-
GS0_6 RAM (with Parity)	1024	0x0000_D400	0x0000_D7FF	YES	Parity	-	-
TI OTP Bank 0	1536	0x0007_2000	0x0007_25FF	-	ECC	-	-
UID_REGS	6	0x0007_2172	0x0007_2177	-	ECC	-	-
DCSM BANK0 Z1 OTP	512	0x0007_8000	0x0007_81FF	-	ECC	YES	-
DCSM BANK0 Z2 OTP	512	0x0007_8200	0x0007_83FF	-	ECC	YES	-
BANK0 MAIN Sector (first 128 KB)	65536	0x0008_0000	0x0008_FFFF	-	ECC	YES	-
Z1 Secure functions (Secure Boot, Secure Code Copy, Secure CRC Calc)	4096	0x003F_8000	0x003F_8FFF	-	Parity	YES	-
BootROM functions Flash API Math Tables (IQ) FPU32 Tables FFT Twiddle Factor Tables	28672	0x003F_9000	0x003F_FFFF	-	Parity	-	-
TI OTP Bank 0 ECC	192	0x0107_0400	0x0107_04BF	-	-	-	-

7.1.1.1 Dedicated RAM (Mx RAM)

The CPU subsystem has two dedicated ECC-capable RAM blocks: M0 and M1. These memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them).

7.1.2 Flash Memory Map

On the F28E12x devices, one flash bank is available. Code to program the flash should be executed out of RAM, there should not be any kind of access to the flash bank when an erase or program operation is in progress.

Table 7-2. Flash Memory Map

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
OTP Sectors							
ALL	TI OTP Bank 0 (Unsecure)	1536 x 16	0x0007 2000	0x0007 25EF	128 x 16	0x0107 0200	0x0107 02BD
	TI OTP Bank 0 (Secure)	16 x 16	0x0007 25F0	0x0007 25FF	128 x 16	0x0107 02BE	0x0107 02BF
	User configurable DCSM OTP Bank 0	1K x 16	0x0007 8000	0x0007 83FF	128 x 16	0x0107 1000	0x0107 107F
Bank 0 Sectors							
ALL	Sector 0	1K x 16	0x0008 0000	0x0008 03FF	128 x 16	0x0108 0000	0x0108 007F
	Sector 1	1K x 16	0x0008 0400	0x0008 07FF	128 x 16	0x0108 0080	0x0108 00FF
	Sector 2	1K x 16	0x0008 0800	0x0008 0BFF	128 x 16	0x0108 0100	0x0108 017F
	Sector 3	1K x 16	0x0008 0C00	0x0008 0FFF	128 x 16	0x0108 0180	0x0108 01FF
	Sector 4	1K x 16	0x0008 1000	0x0008 13FF	128 x 16	0x0108 0200	0x0108 027F
	Sector 5	1K x 16	0x0008 1400	0x0008 17FF	128 x 16	0x0108 0280	0x0108 02FF
	Sector 6	1K x 16	0x0008 1800	0x0008 1BFF	128 x 16	0x0108 0300	0x0108 037F
	Sector 7	1K x 16	0x0008 1C00	0x0008 1FFF	128 x 16	0x0108 0380	0x0108 03FF
	Sector 8	1K x 16	0x0008 2000	0x0008 23FF	128 x 16	0x0108 0400	0x0108 047F
	Sector 9	1K x 16	0x0008 2400	0x0008 27FF	128 x 16	0x0108 0480	0x0108 04FF
	Sector 10	1K x 16	0x0008 2800	0x0008 2BFF	128 x 16	0x0108 0500	0x0108 057F
	Sector 11	1K x 16	0x0008 2C00	0x0008 2FFF	128 x 16	0x0108 0580	0x0108 05FF
	Sector 12	1K x 16	0x0008 3000	0x0008 33FF	128 x 16	0x0108 0600	0x0108 067F
	Sector 13	1K x 16	0x0008 3400	0x0008 37FF	128 x 16	0x0108 0680	0x0108 06FF
	Sector 14	1K x 16	0x0008 3800	0x0008 3BFF	128 x 16	0x0108 0700	0x0108 077F
	Sector 15	1K x 16	0x0008 3C00	0x0008 3FFF	128 x 16	0x0108 0780	0x0108 07FF
	Sector 16	1K x 16	0x0008 4000	0x0008 43FF	128 x 16	0x0108 0800	0x0108 087F
	Sector 17	1K x 16	0x0008 4400	0x0008 47FF	128 x 16	0x0108 0880	0x0108 08FF
	Sector 18	1K x 16	0x0008 4800	0x0008 4BFF	128 x 16	0x0108 0900	0x0108 097F
	Sector 19	1K x 16	0x0008 4C00	0x0008 4FFF	128 x 16	0x0108 0980	0x0108 09FF
	Sector 20	1K x 16	0x0008 5000	0x0008 53FF	128 x 16	0x0108 0A00	0x0108 0A7F
	Sector 21	1K x 16	0x0008 5400	0x0008 57FF	128 x 16	0x0108 0A80	0x0108 0AFF
	Sector 22	1K x 16	0x0008 5800	0x0008 5BFF	128 x 16	0x0108 0B00	0x0108 0B7F
	Sector 23	1K x 16	0x0008 5C00	0x0008 5FFF	128 x 16	0x0108 0B80	0x0108 0BFF
	Sector 24	1K x 16	0x0008 6000	0x0008 63FF	128 x 16	0x0108 0C00	0x0108 0C7F
	Sector 25	1K x 16	0x0008 6400	0x0008 67FF	128 x 16	0x0108 0C80	0x0108 0CFF
	Sector 26	1K x 16	0x0008 6800	0x0008 6BFF	128 x 16	0x0108 0D00	0x0108 0D7F
	Sector 27	1K x 16	0x0008 6C00	0x0008 6FFF	128 x 16	0x0108 0D80	0x0108 0DFF
	Sector 28	1K x 16	0x0008 7000	0x0008 73FF	128 x 16	0x0108 0E00	0x0108 0E7F
	Sector 29	1K x 16	0x0008 7400	0x0008 77FF	128 x 16	0x0108 0E80	0x0108 0EFF
	Sector 30	1K x 16	0x0008 7800	0x0008 7BFF	128 x 16	0x0108 0F00	0x0108 0F7F
	Sector 31	1K x 16	0x0008 7C00	0x0008 7FFF	128 x 16	0x0108 0F80	0x0108 0FFF

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Table 7-2. Flash Memory Map (continued)

PART NUMBER	SECTOR	ADDRESS			ECC ADDRESS		
		SIZE	START	END	SIZE	START	END
F28E120SC	Sector 32	1K x 16	0x0008 8000	0x0008 83FF	128 x 16	0x0108 1000	0x0108 107F
	Sector 33	1K x 16	0x0008 8400	0x0008 87FF	128 x 16	0x0108 1080	0x0108 10FF
	Sector 34	1K x 16	0x0008 8800	0x0008 8BFF	128 x 16	0x0108 1100	0x0108 117F
	Sector 35	1K x 16	0x0008 8C00	0x0008 8FFF	128 x 16	0x0108 1180	0x0108 11FF
	Sector 36	1K x 16	0x0008 9000	0x0008 93FF	128 x 16	0x0108 1200	0x0108 127F
	Sector 37	1K x 16	0x0008 9400	0x0008 97FF	128 x 16	0x0108 1280	0x0108 12FF
	Sector 38	1K x 16	0x0008 9800	0x0008 9BFF	128 x 16	0x0108 1300	0x0108 137F
	Sector 39	1K x 16	0x0008 9C00	0x0008 9FFF	128 x 16	0x0108 1380	0x0108 13FF
	Sector 40	1K x 16	0x0008 A000	0x0008 A3FF	128 x 16	0x0108 1400	0x0108 147F
	Sector 41	1K x 16	0x0008 A400	0x0008 A7FF	128 x 16	0x0108 1480	0x0108 14FF
	Sector 42	1K x 16	0x0008 A800	0x0008 ABFF	128 x 16	0x0108 1500	0x0108 157F
	Sector 43	1K x 16	0x0008 AC00	0x0008 AFFF	128 x 16	0x0108 1580	0x0108 15FF
	Sector 44	1K x 16	0x0008 B000	0x0008 B3FF	128 x 16	0x0108 1600	0x0108 167F
	Sector 45	1K x 16	0x0008 B400	0x0008 B7FF	128 x 16	0x0108 1680	0x0108 16FF
	Sector 46	1K x 16	0x0008 B800	0x0008 BBFF	128 x 16	0x0108 1700	0x0108 177F
	Sector 47	1K x 16	0x0008 BC00	0x0008 BFFF	128 x 16	0x0108 1780	0x0108 17FF
	Sector 48	1K x 16	0x0008 C000	0x0008 C3FF	128 x 16	0x0108 1800	0x0108 187F
	Sector 49	1K x 16	0x0008 C400	0x0008 C7FF	128 x 16	0x0108 1880	0x0108 18FF
	Sector 50	1K x 16	0x0008 C800	0x0008 CBFF	128 x 16	0x0108 1900	0x0108 197F
	Sector 51	1K x 16	0x0008 CC00	0x0008 CFFF	128 x 16	0x0108 1980	0x0108 19FF
	Sector 52	1K x 16	0x0008 D000	0x0008 D3FF	128 x 16	0x0108 1A00	0x0108 1A7F
	Sector 53	1K x 16	0x0008 D400	0x0008 D7FF	128 x 16	0x0108 1A80	0x0108 1AFF
	Sector 54	1K x 16	0x0008 D800	0x0008 DBFF	128 x 16	0x0108 1B00	0x0108 1B7F
	Sector 55	1K x 16	0x0008 DC00	0x0008 DFFF	128 x 16	0x0108 1B80	0x0108 1BFF
	Sector 56	1K x 16	0x0008 E000	0x0008 E3FF	128 x 16	0x0108 1C00	0x0108 1C7F
	Sector 57	1K x 16	0x0008 E400	0x0008 E7FF	128 x 16	0x0108 1C80	0x0108 1CFF
	Sector 58	1K x 16	0x0008 E800	0x0008 EBFF	128 x 16	0x0108 1D00	0x0108 1D7F
	Sector 59	1K x 16	0x0008 EC00	0x0008 EFFF	128 x 16	0x0108 1D80	0x0108 1DFF
	Sector 60	1K x 16	0x0008 F000	0x0008 F3FF	128 x 16	0x0108 1E00	0x0108 1E7F
	Sector 61	1K x 16	0x0008 F400	0x0008 F7FF	128 x 16	0x0108 1E80	0x0108 1EFF
	Sector 62	1K x 16	0x0008 F800	0x0008 FBFF	128 x 16	0x0108 1F00	0x0108 1F7F
	Sector 63	1K x 16	0x0008 FC00	0x0008 FFFF	128 x 16	0x0108 1F80	0x0108 1FFF

ADVANCE INFORMATION

7.1.3 Peripheral Registers Memory Map

Table 7-3. Peripheral Registers Memory Map

Structure	DriverLib Name	Base Address	CPU1.DMA	Pipeline Protected
Peripheral Frame 0 (PF0)				
CPUTIMER_REGS	CPUTIMER0_BASE	0x0000_0C00	-	-
CPUTIMER_REGS	CPUTIMER1_BASE	0x0000_0C08	-	-
CPUTIMER_REGS	CPUTIMER2_BASE	0x0000_0C10	-	-
PIE_CTRL_REGS	PIECTRL_BASE	0x0000_0CE0	-	-
PIE_VECT_TABLE	PIEVECTTABLE_BASE	0x0000_0D00	-	-
DMA_REGS	DMA_BASE	0x0000_1000	-	-
DMA_CH_REGS	DMA_CH1_BASE	0x0000_1020	-	-
DMA_CH_REGS	DMA_CH2_BASE	0x0000_1040	-	-
ADC_LITE_RESULT_REGS	ADCARESULT_BASE	0x0000_1800	YES	-
UID_REGS	UID_BASE	0x0007_2172	-	-
DCSM_Z1_OTP	DCSM_Z1OTP_BASE	0x0007_8000	-	-
DCSM_Z2_OTP	DCSM_Z2OTP_BASE	0x0007_8200	-	-
Peripheral Frame 1 (PF1)				
MCPWM_6CH_REGS	PWM1_BASE	0x0000_4000	YES	YES
MCPWM_2CH_REGS	PWM3_BASE	0x0000_4800	YES	YES
EQEP_REGS	EQEP1_BASE	0x0000_5100	YES	YES
ECAP_REGS	ECAP1_BASE	0x0000_5200	YES	YES
CMPSS_LITE_REGS	CMPSSLITE1_BASE	0x0000_5500	YES	YES
CMPSS_LITE_REGS	CMPSSLITE2_BASE	0x0000_5540	YES	YES
CMPSS_LITE_REGS	CMPSSLITE3_BASE	0x0000_5580	YES	YES
PGA_REGS	PGA1_BASE	0x0000_5B00	YES	YES
Peripheral Frame 2 (PF2)				
SPI_REGS	SPIA_BASE	0x0000_6100	YES	YES
Peripheral Frame 3 (PF3)				
ADC_LITE_REGS	ADCA_BASE	0x0000_7400	-	YES
Peripheral Frame 4 (PF4)				
INPUT_XBAR_REGS	INPUTXBAR_BASE	0x0000_7900	-	YES
XBAR_REGS	XBAR_BASE	0x0000_7920	-	YES
SYNC_SOC_REGS	SYNCSOC_BASE	0x0000_7940	-	YES
DMA_CLA_SRC_SEL_REGS	DMACLASRCSEL_BASE	0x0000_7980	-	YES
PWM_XBAR_REGS	PWMXBAR_BASE	0x0000_7A00	-	YES
OUTPUT_XBAR_REGS	OUTPUTXBAR_BASE	0x0000_7A80	-	YES
GPIO_CTRL_REGS	GPIOCTRL_BASE	0x0000_7C00	-	YES
GPIO_DATA_REGS	GPIODATA_BASE	0x0000_7F00	-	YES
GPIO_DATA_READ_REGS	GPIODATAREAD_BASE	0x0000_7F80	-	YES
DEV_CFG_REGS	DEVCFG_BASE	0x0005_D000	-	YES
CLK_CFG_REGS	CLKCFG_BASE	0x0005_D200	-	YES
CPU_SYS_REGS	CPUSYS_BASE	0x0005_D300	-	YES
SYS_STATUS_REGS	SYSSTAT_BASE	0x0005_D400	-	YES
ANALOG_SUBSYS_REGS	ANALOGSUBSYS_BASE	0x0005_D700	-	YES
Peripheral Frame 6 (PF6)				
DCSM_Z1_REGS	DCSM_Z1_BASE	0x0005_F000	-	YES
DCSM_Z2_REGS	DCSM_Z2_BASE	0x0005_F080	-	YES
DCSM_COMMON_REGS	DCSMCOMMON_BASE	0x0005_F0C0	-	YES
MEM_CFG_REGS	MEMCFG_BASE	0x0005_F400	-	YES
MEMORY_ERROR_REGS	MEMORYERROR_BASE	0x0005_F540	-	YES
ROM_WAIT_STATE_REGS	ROMWAITSTATE_BASE	0x0005_F580	-	YES

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Table 7-3. Peripheral Registers Memory Map (continued)

Structure	DriverLib Name	Base Address	CPU1.DMA	Pipeline Protected
TEST_ERROR_REGS	TESTERROR_BASE	0x0005_F590	-	YES
FLASH_CTRL_REGS	FLASH0CTRL_BASE	0x0005_F800	-	YES
FLASH_ECC_REGS	FLASH0ECC_BASE	0x0005_FB00	-	YES
Peripheral Frame 7 (PF7)				
DCC_REGS	DCC0_BASE	0x0005_E700	-	YES
Peripheral Frame 9 (PF9)				
WD_REGS	WD_BASE	0x0000_7000	-	YES
NMI_INTRUPT_REGS	NMI_BASE	0x0000_7060	-	YES
XINT_REGS	XINT_BASE	0x0000_7070	-	YES
SCI_REGS	SCIA_BASE	0x0000_7200	-	YES
SCI_REGS	SCIB_BASE	0x0000_7210	-	YES
I2C_REGS	I2CA_BASE	0x0000_7300	-	YES
Peripheral Frame 11 (PF11)				
UART_REGS, UART_REGS_WRITE	UARTA_BASE, UARTAWRITE_BASE	0x0006_A000	YES	YES

7.2 Identification

Table 7-4 lists the Device Identification Registers. Additional information on these device identification registers can be found in the *F28E12x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-4. Device Identification Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION	
PARTIDL	0x0007 21CA	2	*Bits*	*Options*
			23-16 FLASH_SIZE	0x2 - 64KB
				0x4 - 128KB
			7-6 QUAL	0 = Engineering sample (TMX)
				1 = Pilot production (TMP)
				2 = Fully qualified (TMS)
PARTIDH	0x0007 21CC	2	Device part identification number	
			F28E120SC	0x10FF 0500
			F28E120SB	0x10FE 0500
REVID	0x0005 D006	2	Silicon revision number	
			Revision 0	0x0000 0001
UID_UNIQUE0	0x0007 214A	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices.	
UID_UNIQUE1	0x0007 214C	2	Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices.	

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7.3 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the *TMS320C28x CPU and Instruction Set Reference Guide*.

7.3.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information on the C28x Floating Point Unit (FPU), see the *TMS320C28x Extended Instruction Sets Technical Reference Manual*.

7.4 Direct Memory Access (DMA)

The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing. Figure 7-1 shows a device-level block diagram of the DMA.

DMA features include:

- Two channels with independent ePIE interrupts
- Peripheral interrupt trigger sources
  - ADC interrupts and EVT signals
  - External Interrupts
  - MCPWM SOC signals
  - CPU timers
  - SPI transmit and receive
  - UART transmit and receive
    - Regular FIFO level triggers (UARTx_TX and UARTx_RX) and single request triggers (UARTx_TX_SREQ and UARTx_RX_SREQ)
- Data sources and destinations:
  - GSx RAM
  - ADC result registers
  - Control peripheral registers (MCPWM, eQEP
  - Communication peripheral registers (SPI, UART)
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: Three cycles per word without arbitration

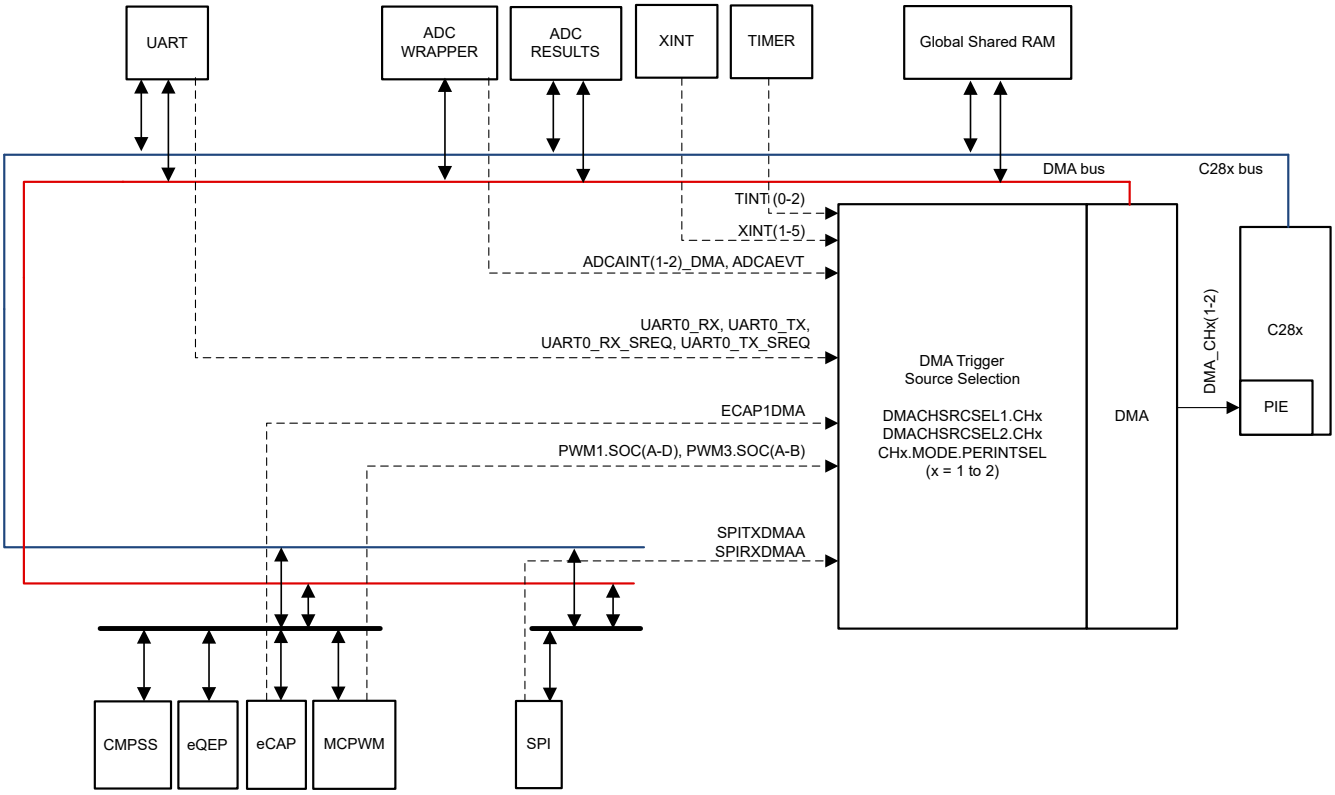

Figure 7-1. DMA Block Diagram

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7.5 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes supported on this device. The boot ROM uses the boot mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration.

Table 7-5 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used.

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

See the Reset (XRSn) Switching Characteristics table and the Reset Timing Diagrams section for $t_{boot\text{-}flash}$, the boot ROM execution time to first instruction fetch in flash.

Table 7-5. Device Default Boot Modes

BOOT MODE	GPIO24 (DEFAULT BOOT MODE SELECT PIN 1)	GPIO32 (DEFAULT BOOT MODE SELECT PIN 0)
Parallel IO	0	0
SCI / Wait Boot(1)	0	1
Flash	1	1

(1) SCI boot mode can be used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.

Table 7-6 lists the possible boot modes supported on the device. The default boot mode pins are GPIO24 (boot mode pin 1) and GPIO32 (boot mode pin 0). Users may choose to have weak pullups for boot mode pins if they use a peripheral on these pins as well, so the pullups can be overdriven. On this device, customers can change the factory default boot mode pins by programming user-configurable Dual Code Security Module (DCSM) OTP locations.

Table 7-6. All Available Boot Modes

BOOT MODE NUMBER	BOOT MODE
0	Parallel
1	SCI / Wait
3	Flash
4	Wait
5	RAM
6	SPI
7	I2C
10	Secure Flash

Note

All the peripheral boot modes supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, and so forth). Whenever these boot modes are referred to in this section, such as SCI boot, it is actually referring to the first module instance, meaning SCI boot on the SCIA port. The same applies to the other peripheral boots.

7.5.1 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from zero boot mode select pins up to three boot mode select pins and from one configured boot mode up to eight configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of SPI for firmware updates, tertiary boot option of SCI boot for debugging, and so forth.)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: Two BMSPs are required to select between three boot mode options)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default which is disabled). Refer to Section 7.5.1.1 for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0=Boot to Flash, BOOTDEF1=SPI Boot, BOOTDEF2=SCI Boot; all other BOOTDEFx are left as default/nothing). Refer to the *Configuring Boot Mode Pins* section for all the details on setting up and configuring the custom boot mode table.

Additionally, the *Boot Mode Example Use Cases* section of the *F28E12x Real-Time Microcontrollers Technical Reference Manual* provides some example use cases on how to configure the BMSPs and custom boot tables.

7.5.1.1 Configuring Boot Mode Pins

This section explains how the boot mode select pins are customized by the user, by programming the BOOTPIN-CONFIG location (refer to Table 7-7), in the user-configurable dual-zone security module (DCSM) OTP. The location in the DCSM OTP is Z1-OTP-BOOTPIN-CONFIG or Z2-OTP-BOOTPIN-CONFIG. When debugging, EMU-BOOTPIN-CONFIG is the emulation equivalent of Z1-OTP-BOOTPIN-CONFIG/Z2-OTP-BOOTPIN-CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use **zero**, **one**, **two**, or **three** boot mode select pins as needed.

Note

When using Z2-OTP-BOOTPIN-CONFIG, the configurations programmed in this location take priority over the configurations in Z1-OTP-BOOTPIN-CONFIG. It is recommended to use Z1-OTP-BOOTPIN-CONFIG first and then, if OTP configurations need to be altered, switch to using Z2-OTP-BOOTPIN-CONFIG.

Table 7-7. BOOTPIN-CONFIG Bit Fields

Bit	Name	Description
31:24	Key	Write 0x5A to these 8-bits to tell the boot ROM code that the bits in this register are valid.
23:16	Boot Mode Select Pin 2 (BMSP2)	Refer to BMSP0 description.
15:8	Boot Mode Select Pin 1 (BMSP1)	Refer to BMSP0 description.
7:0	Boot Mode Select Pin 0 (BMSP0)	Set to the GPIO pin to be used during boot (up to 255). 0x0 = GPIO0, 0x01 = GPIO1, and so on. Writing 0xFF disables this BMSP and this pin is no longer used to select the boot mode.

Note

GPIO 12, 13, 20, 21, 28, 224, 226-228, 230, 242-243 are analog pins, but digital inputs are possible on these pins provided the software writes to the GPIOHAMSEL register bits.

The following GPIOs cannot be used as a BMSP. If selected for a particular BMSP, the boot ROM automatically selects the factory default GPIOs for BMSP0 and BMSP1. Factory default for BMSP2 is 0xFF, which disables the BMSP.

- GPIO 8, GPIO 14, and GPIO 15 (Not available on any package)
- GPIO 17 to GPIO 22 (Not available on any package)
- GPIO 25 to GPIO 27 (Not available on any package)
- GPIO 31, GPIO 34 to GPIO 38 (Not available on any package)
- GPIO 42, GPIO 44, and GPIO 46 to GPIO 49 (Not available on any package)
- GPIO 225 and GPIO 229 (Not available on any package)
- GPIO 231 to GPIO 241 (Not available on any package)
- GPIO 244 and GPIO 245 (Not available on any package)

Table 7-8. Standalone Boot Mode Select Pin Decoding

BOOTPIN_CONFIG Key	BMSP0	BMSP1	BMSP2	Realized Boot Mode
!= 0x5A	Don't Care	Don't Care	Don't Care	Boot as defined by the factory default BMSPs.
= 0x5A	0xFF	0xFF	0xFF	Boot as defined in the boot table for boot mode 0 (All BMSPs disabled).
	Valid GPIO	0xFF	0xFF	Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled).
	0xFF	Valid GPIO	0xFF	Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled).
	0xFF	0xFF	Valid GPIO	Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled)
	Valid GPIO	Valid GPIO	0xFF	Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled).
	Valid GPIO	0xFF	Valid GPIO	Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled).
	0xFF	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled).
	Valid GPIO	Valid GPIO	Valid GPIO	Boot as defined by the values of BMSP0, BMSP1, and BMSP2.
	Invalid GPIO	Valid GPIO	Valid GPIO	BMSP0 is reset to the factory default BMSP0 GPIO. Boot as defined by the values of BMSP0, BMSP1, and BMSP2.
	Valid GPIO	Invalid GPIO	Valid GPIO	BMSP1 is reset to the factory default BMSP1 GPIO. Boot as defined by the values of BMSP0, BMSP1, and BMSP2.
	Valid GPIO	Valid GPIO	Invalid GPIO	BMSP2 is reset to the factory default state, which is disabled. Boot as defined by the values of BMSP0 and BMSP1.

Note

When decoding the boot mode, BMSP0 is the least-significant bit and BMSP2 is the most-significant bit of the boot table index value. It is recommended when disabling BMSPs to start with disabling BMSP2. For example, in an instance when only using BMSP2 (BMSP1 and BMSP0 are disabled), then only the boot table indexes of 0 and 4 are selectable. In the instance when using only BMSP0, then the selectable boot table indexes are 0 and 1.

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7.5.1.2 Configuring Boot Mode Table Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options. The 64-bit location is located in user-configurable DCSM OTP in the Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations. When debugging, EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH are the emulation equivalents of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH, and can be programmed to experiment with different boot mode options without writing to OTP. The range of customization to the boot definition table depends on how many boot mode select pins (BMSP) are being used. For example, 0 BMSPs equals to 1 table entry, 1 BMSP equals to 2 table entries, 2 BMSPs equals to 4 table entries, and 3 BMSPs equals to 8 table entries. Refer to the *F28E12x Real-Time Microcontrollers Technical Reference Manual* for examples on how to setup the BOOTPIN_CONFIG and BOOTDEF values.

Note

The locations Z2-OTP-BOOTDEF-LOW and Z2-OTP-BOOTDEF-HIGH are used instead of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations when Z2-OTP-BOOTPIN-CONFIG is configured. Refer to Section 7.5.1.1 for more details on BOOTPIN_CONFIG usage.

Table 7-9. BOOTDEF Bit Fields

BOOTDEF Name	Byte Position	Name	Description
BOOT_DEF0	7:0	[3:0] BOOT_DEF0 Mode	Set the boot mode number from Table 7-6. Any unsupported boot mode causes the device to either go to Wait boot (debugger connected) or boot to Flash (standalone).
		[7:4] BOOT_DEF0 Options	Set alternate/additional boot options. This can include changing the GPIOs for a particular boot peripheral or specifying a different Flash entry point. Refer to the *GPIO Assignments* section for valid BOOTDEF values to set in the table.
BOOT_DEF1	15:8	BOOT_DEF1 Mode/ Options	Refer to BOOT_DEF0 description.
BOOT_DEF2	23:16	BOOT_DEF2 Mode/ Options	
BOOT_DEF3	31:24	BOOT_DEF3 Mode/ Options	
BOOT_DEF4	39:32	BOOT_DEF4 Mode/ Options	
BOOT_DEF5	47:40	BOOT_DEF5 Mode/ Options	
BOOT_DEF6	55:48	BOOT_DEF6 Mode/ Options	
BOOT_DEF7	63:56	BOOT_DEF7 Mode/ Options	

7.5.2 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. Refer to Section 7.5.1.2 on how to configure BOOT_DEFx. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Default boot mode GPIO pins:

- Boot mode pin 0 - GPIO32
- Boot mode pin 1 - GPIO24

Guidelines on boot pin selection:

- Avoid pins that have PWM functionality.
- Cannot be analog or USB pins.
- Boot mode select pins and default boot peripheral pins can be available on all packages.
- Avoid JTAG emulation pins and crystal pins.
- Boot mode select pins can be inputs.
- Pins cannot have PHY bootstrap functionality.

Table 7-10. SCI Boot Options

Option	BOOTDEFx Value	SCITXDA GPIO	SCIRXDA GPIO	Package Supported
0 (default)	0x01	GPIO29	GPIO28	All
1	0x21	GPIO1	GPIO0	All
3	0x61	GPIO7	GPIO3	48-PT, 32-RHB, 32-VFC
4	0x81	GPIO16	GPIO3	48-PT

Table 7-11. I2C Boot Options

Option	BOOTDEFx Value	SDAA GPIO	SCLA GPIO	Package Supported
0	0x07	GPIO0	GPIO1	All
1	0x27	GPIO32	GPIO33	48-PT
2	0x47	GPIO5	GPIO4	All

Table 7-12. SPI Boot Options

Option	BOOTDEFx Value	SPIPICOA	SPIPOCIA	SPICLKA	SPIPTEA	Package Supported
0	0x06	GPIO24	GPIO1	GPIO3	GPIO5	All
1	0x26	GPIO16	GPIO1	GPIO3	GPIO0	48-PT
3	0x66	GPIO16	GPIO13	GPIO12	GPIO24	48-PT

Table 7-13. Wait Boot Options

Option	BOOTDEFx Value	Watchdog Status	Package Supported
0	0x04	Enabled	All
1	0x24	Disabled	All

Table 7-14. Flash Boot Options

Option	BOOTDEFx Value	Flash Entry Address	Flash Sector	Package Supported
0 (default)	0x03	0x0008 0000	CPU1 Bank 0 Sector 0	All
1	0x23	0x0008 8000	CPU1 Bank 0 Sector 32	All

Table 7-15. Secure Flash Boot Options

Option	BOOTDEFx Value	Flash Entry Address	Flash Sector	Package Supported
0 (default)	0x0A	0x0008 0000	CPU1 Bank 0 Sector 0	All

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Table 7-15. Secure Flash Boot Options (continued)

Option	BOOTDEFx Value	Flash Entry Address	Flash Sector	Package Supported
1	0x2A	0x0008 8000	CPU1 Bank 0 Sector 32	All

Table 7-16. Parallel Boot Options

Option	BOOTDEFx Value	D0-D7 GPIO	DSP Control GPIO	Host Control GPIO	Package Supported
0 (default)	0x00	D0-D7 (GPIO 0,1,3,4,5,24,28,29)	GPIO224	GPIO242	All
1	0x20	D0-D7 (GPIO 0-7)	GPIO12	GPIO13	48-PT

7.6 Security

Security features are enforced by the Dual Code Security Module (DCSM). The primary layer of defense is securing the boundary of the chip, which should always be enabled. Additionally, the Dual Zone Security feature is available to support code partitioning.

7.6.1 Securing the Boundary of the Chip

The following two features, along with authentication in the firmware update code, should be used to help to prevent unauthorized code from running on the device.

7.6.1.1 JTAGLOCK

Enabling the JTAGLOCK feature in the USER OTP disables JTAG access (for example, debug probe) to resources on the device.

7.6.1.2 Zero-pin Boot

Enabling the Zero-pin Boot option along with Flash Boot in the USER OTP blocks all pin-based external bootloader options (for example, SCI, Parallel).

7.6.2 Dual-Zone Security

The dual-zone security mechanism offers protection for two zones: Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (LSx RAM and flash sectors).

7.6.3 Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

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7.7 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ microcontrollers, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-2 shows the various functional blocks within the watchdog module.

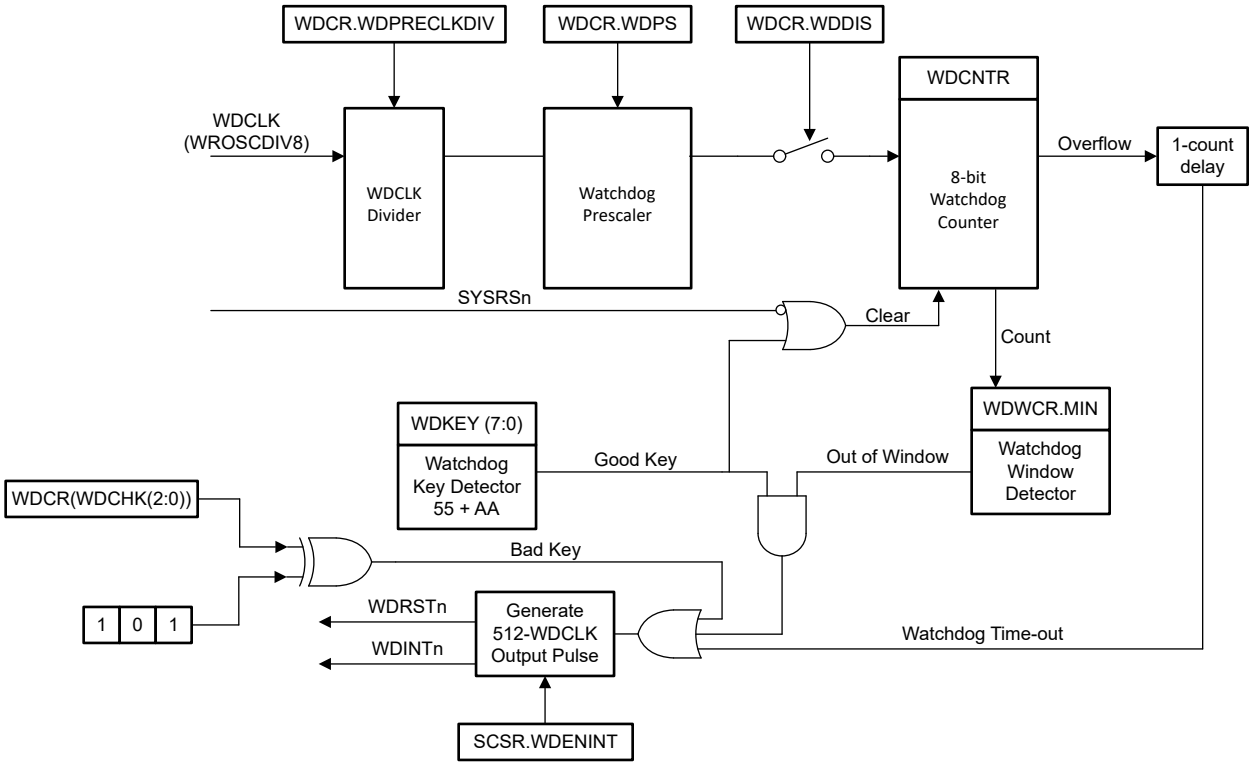


Figure 7-2. Windowed Watchdog

7.8 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- WROSCDIV8
- SYSOSCDIV4
- X1 (XTAL)

7.9 Dual-Clock Comparator (DCC)

The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.9.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.9.2 Mapping of DCCx Clock Source Inputs

Table 7-17. DCCx Clock Source0 Table

DCCxCLKSRC0[3:0]	CLOCK NAME
0x0	XTAL/X1
0x1	WROSCDIV8
0x2	SYSOSCDIV4
0x4	TCK
0x5	CPU1.SYSCLK
0xC	INPUT XBAR (Output16 of input-xbar)
others	Reserved

Table 7-18. DCCx Clock Source1 Table

DCCxCLKSRC1[4:0]	CLOCK NAME
0x0	PLLRAWCLK
0x2	WROSCDIV8
0x3	SYSOSCDIV4
0x6	CPU1.SYSCLK
0x9	Input XBAR (Output15 of the input-xbar)
0xB	MCPWMCLK
0xC	LSPCLK
0xD	ADCCLK
0xE	WDCLK
0xF	Reserved
others	Reserved

8 Reference Design

The TI Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all reference designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at the Select TI reference designs page.

Below is a partial list of applicable reference designs. A full listing of supported reference designs for this device, as well as other C2000 MCUs, is maintained inside TI resource explorer.

3-kW, 180-W/in3 single-phase totem-pole bridgeless PFC reference design with 16-A max input
This reference design demonstrates a method to control a continuous conduction mode Totem pole power factor correction converter (PFC) using C2000™ microcontrollers. The PFC also works as inverter in grid connected (current controlled) mode. The converter is designed to support a maximum input current of 16-ARMS and peak power of 3.6 kW.

GaN-based, 6.6-kW, bidirectional, onboard charger reference design
The PMP22650 reference design is a 6.6-kW, bidirectional, onboard charger. The design employs a two-phase totem pole PFC and a full-bridge CLLLC converter with synchronous rectification. The CLLLC utilizes both frequency and phase modulation to regulate the output across the required regulation range.

Bidirectional CLLLC resonant dual active bridge (DAB) reference design for HEV/EV onboard charger
CLLLC resonant DAB with bidirectional power flow capability and soft switching characteristics is an ideal candidate for Hybrid Electric Vehicle/Electric Vehicle (HEV/EV) on-board chargers and energy storage applications. This design illustrates control of this power topology using a C2000™ MCU in closed voltage and closed current-loop mode.

48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Evaluation Module
The BOOSTXL-3PHGANINV evaluation module features a 48-V/10-A three-phase GaN inverter with precision in-line shunt-based phase current sensing for accurate control of precision drives such as servo drives.

C2000 DesignDRIVE position manager BoosterPack™ plug-in module
The PositionManager BoosterPack is a flexible low voltage platform intended for evaluating interfaces to absolute encoders and analog sensors like resolvers and SinCos transducers. When combined with the DesignDRIVE Position Manager software solutions this low-cost evaluation module becomes a powerful tool for interfacing many popular position encoder types such as EnDat, BiSS and T-format with C2000 Real-Time Control devices. C2000 Position Manager technology integrates interfaces to the most popular digital and analog position sensors onto C2000 Real-Time Controller, thus eliminating the need for external FPGAs for these functions.

C2000™ MCU evaluation module for high-voltage three-phase inverter motor control
The TIEVM-MTR-HVINV is a 750W development board for high-voltage motor drive applications. This EVM implements sensorless FOC control for a three-phase permanent-magnet synchronous motor (PMSM) with the InstaSPIN-FOC FAST and eSMO sensorless observers. The modular design allows for plug-and-play support of different daughterboard attachments to the same motherboard. The hardware and firmware of this EVM are tested and ready-to-use to help accelerate development time, with design details and test results available in this user's guide.

250W motor inverter reference design
This reference design is a 250W motor drive for a major appliances or similar applications, which illustrates a GaN IPM DRV7308 based high efficiency motor inverter without heat sink, also demo a low standby power design with UCC28911. This reference design shows a method to implement sensorless FOC control for a 3-phase PMSM with a FAST™ software encoder or eSMO. With a modular design, this reference design supports both the C2000™ MCU and MSPM0 series microcontroller daughter-board on the same motherboard. The hardware and software available with this reference design are tested and ready-to-use to help accelerate development time to market. The design details and test results are found in this design guide.

ADVANCE INFORMATION

DRV8323RS three-phase smart gate driver with buck, shunt amps (SPI interface) evaluation module

The BOOSTXL-DRV8323RS is a 15A, 3-phase brushless DC drive stage based on the DRV8323RH gate driver and CSD88599Q5DC NexFETTM power blocks. The module has individual DC bus and phase voltage sense as well as individual low-side current shunt amplifiers, making this evaluation module ideal for sensorless BLDC algorithms. The module supplies MCU 3.3V power with an integrated 0.6A step down buck regulator. The drive stage is fully protected with short circuit, thermal, shoot-through, and under voltage protection and easily configurable via the devices SPI registers.

DRV8323RH Three-Phase Smart Gate Driver With Buck, Shunt Amps (Hardware Interface) Evaluation Module

The BOOSTXL-DRV8323RH is a 15A, 3-phase brushless DC drive stage based on the DRV8323RH gate driver and CSD88599Q5DC NexFETTM power blocks. The module has individual DC bus and phase voltage sense as well as individual low-side current shunt amplifiers, making this EVM ideal for sensorless BLDC algorithms. The module supplies MCU 3.3V power with an integrated 0.6A step down buck regulator. The drive stage is fully protected with short circuit, thermal, shoot-through, and under voltage protection and easily configurable via different hardware configuration pins.

DRV8329A evaluation module for three-phase BLDC gate driver

The DRV8329AEVM is a 30-A, 3-phase brushless DC drive stage based on the DRV8329A gate driver for BLDC motors. The DRV8329 incorporates three diodes for bootstrap operation without the need for external diodes. The device includes a current shunt amplifier for low-side current measurement, 80-mA LDO, dead time control pin, VDS overcurrent level pin, and gaet driver shutoff pin. The EVM includes switches, potentiometers, and resistors to evaluate these settings as well as configurability for the A variant (6x PWM) and B variant (3x PWM) of the DRV8329 device.

DRV8316R three-phase PWM motor driver evaluation module

The DRV8316REVM provides three half-H-bridge integrated MOSFET drivers for driving a three-phase brushless DC (BLDC) motor with 8-A Peak current drive, for 12-V/24-V DC rails or battery powered applications.

DRV8353RS evaluation module, three-phase brushless DC smart gate driver

The DRV8353RS-EVM is a 15A, 3-phase brushless DC drive stage based on the DRV8353RS gate driver and CSD19532Q5B NexFET™ MOSFETs.

1.3kW GaN totem pole PFC and motor inverter reference design

The TIDA-010282 reference design is a 1.3-kW totem pole power factor correction and motor inverter for major appliances and similar products. The design illustrates a method to implement digital Totem Pole PFC and sensorless vector control of 3-phase permanent magnet synchronous motor (PMSM) to meet higher efficiency and low profile requirements with a single C2000™ microcontroller. The hardware and software available with this reference design are tested and ready-to-use to help accelerate development time to market. The design details and test results can be found in this design guide.

ADVANCE INFORMATION

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MCU devices. Each MCU commercial family member has one of three prefixes: X, P, or no prefix (for example, XF28E120SCPT).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

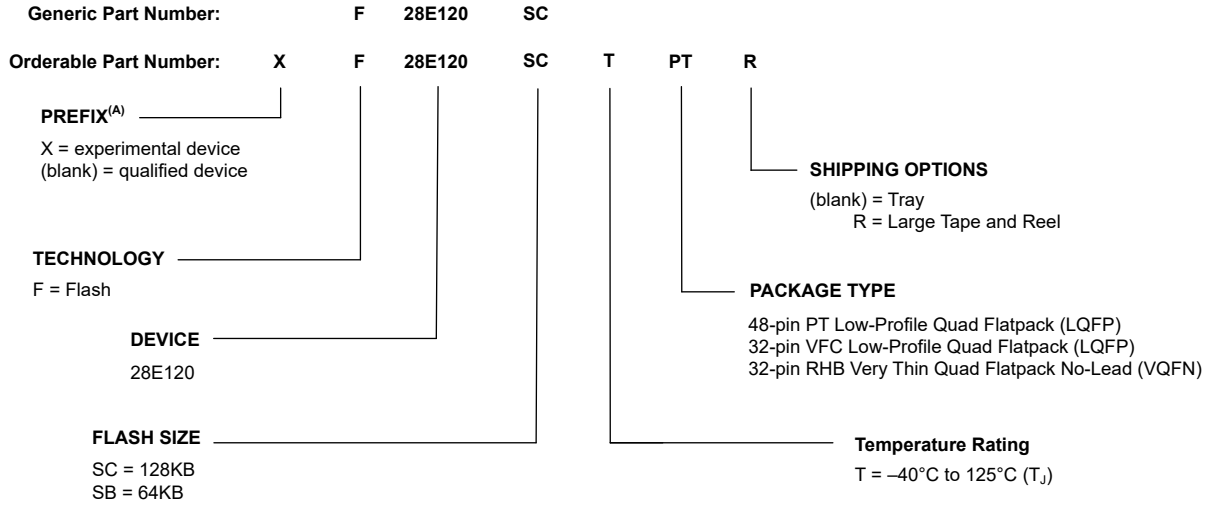
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PT).

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.



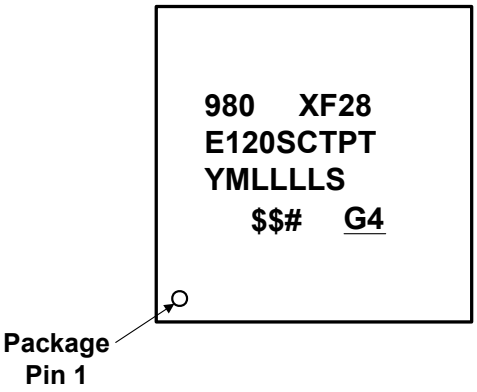
A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

ADVANCE INFORMATION

9.2 Markings

Figure 9-2, Figure 9-3, and Figure 9-4 show the package symbolization. Table 9-1 lists the silicon revision codes.

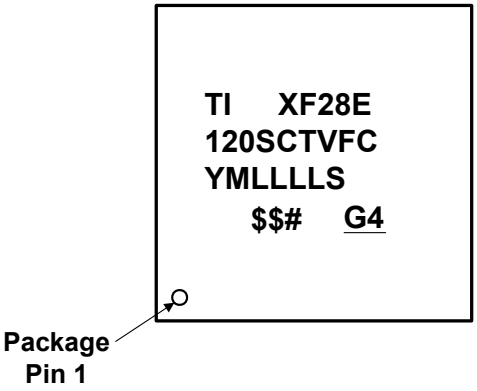


YMLLLLS = Lot Trace Code

980 = TI EIA Code
YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-2. Package Symbolization for PT Package

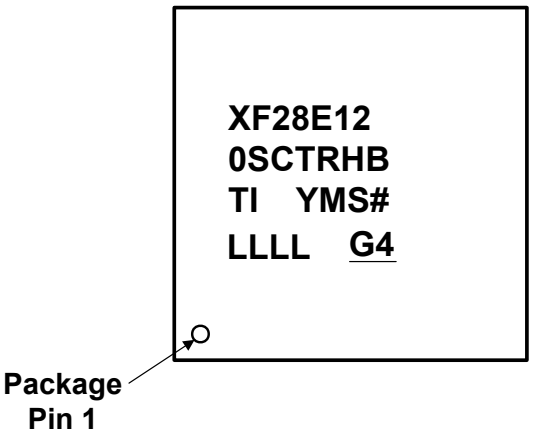


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
$$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-3. Package Symbolization for VFC Package



YM = 2-digit Year/Month Code
S = Assembly Site Code
# = Silicon Revision Code
LLLL = Assembly Lot Code

G4 = Green (Low Halogen and RoHS-compliant)

Figure 9-4. Package Symbolization for RHB Package

Table 9-1. Revision Identification

SILICON REVISION CODE	SILICON REVISION	REVID(1) ADDRESS: 0x5D006	COMMENTS
Blank	0	0x0000 0001	This silicon revision is available as TMX.

(1) Silicon Revision ID

9.3 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time microcontrollers page.

Development Tools

TI Resource Explorer
To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

Software Tools

C2000Ware for C2000 MCUs
C2000Ware for C2000™ MCUs is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

DigitalPower SDK
DigitalPower SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs), which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

MotorControl SDK
MotorControl SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs), which are targeted for industrial drive and other motor control, MotorControl SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

Code Composer Studio™ integrated development environment (IDE)
Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. Code Composer Studio is available for download across Windows®, Linux® and macOS® desktops. It can also be used in the cloud by visiting https://dev.ti.com. Code Composer Studio includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler and many other features. The intuitive IDE takes you through each step of the application development flow. Familiar tools and interfaces make getting started faster than ever before. The desktop version of Code Composer Studio combines the advantages of the Eclipse software framework with advanced capabilities from TI resulting in a compelling feature-rich environment. The cloud-based Code Composer Studio leverages the Theia application framework enabling development in the cloud without needing to download and install large amounts of software.

SysConfig System configuration tool
SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a standalone installer, or can be used via the dev.ti.com cloud tools portal. For more information about the SysConfig system configuration tool, visit the System configuration tool page.

C2000 Third-party search tool
TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

ADVANCE INFORMATION

UniFlash Standalone Flash Tool
UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the *Design tools & simulation* section of the *Design & development* page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000 real-time microcontrollers page.

9.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Errata

F28E12x Real-Time MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

Technical Reference Manual

F28E12x Real-Time Microcontrollers Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F28E12x real-time microcontrollers.

CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

TMS320C28x Extended Instruction Sets Technical Reference Manual describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

C2000 Real-Time Microcontrollers Peripherals Reference Guide describes all the peripherals available for TMS320x28x and F29x devices. This reference guide shows the peripherals used by each device and provides descriptions of the peripherals.

Tools Guides

TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Notes

The SMT & packaging application notes website lists documentation on TI's surface mount technology (SMT) and application notes on a variety of packaging-related topics.

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

The Essential Guide for Developing With C2000™ Real-Time Microcontrollers provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

Migrating Software From 8-Bit (Byte) Addressable CPUs to C28x CPU discusses common scenarios of migrating software from 8-bit (byte) addressable CPUs to C28x CPU, and provides a guide on how to develop application irrespective of the addressability.

The *Hardware Design Guide for F2800x C2000™ Real-Time MCU Series Application Note* is an essential guide for hardware developers using C2000 devices, and helps to streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging among many others.

9.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.6 Trademarks

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macOS® is a registered trademark of Apple Inc.
All trademarks are the property of their respective owners.

ADVANCE INFORMATION

9.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Trademarks

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Linux® is a registered trademark of Linus Torvalds.
macOS® is a registered trademark of Apple Inc.
All trademarks are the property of their respective owners.

11 Revision History

Changes from July 27, 2025 to September 8, 2025	Page
• **This Revision History lists the changes from SPRSPB9 to SPRSPB9A.**	1
• *TAPE AND REEL INFORMATION* section: Added XF28E120SBTRHBR	177

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

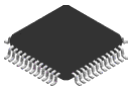
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

To learn more about TI packaging, visit the Packaging website.

ADVANCE INFORMATION

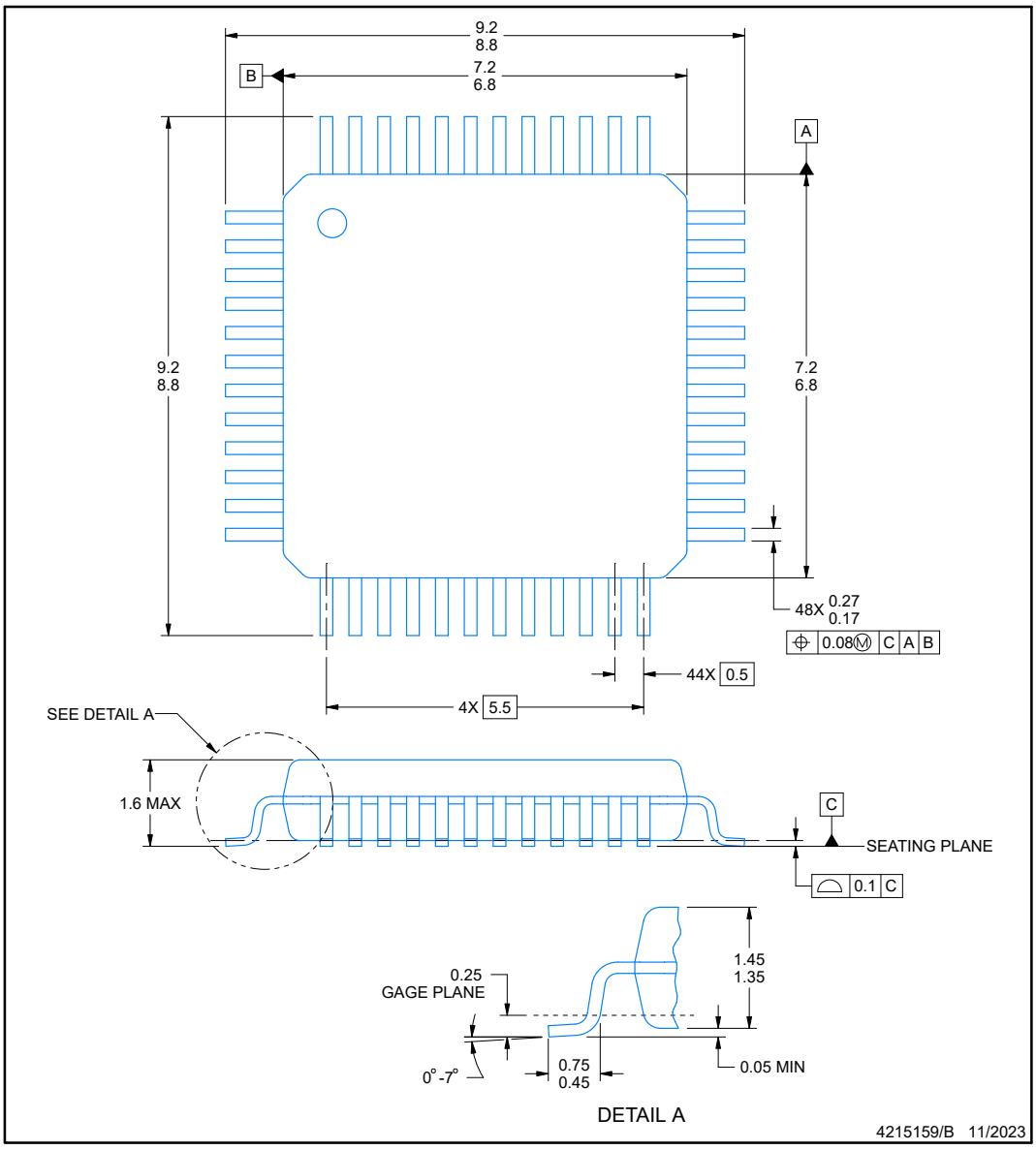
PACKAGE OUTLINE

PT0048A



LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES:

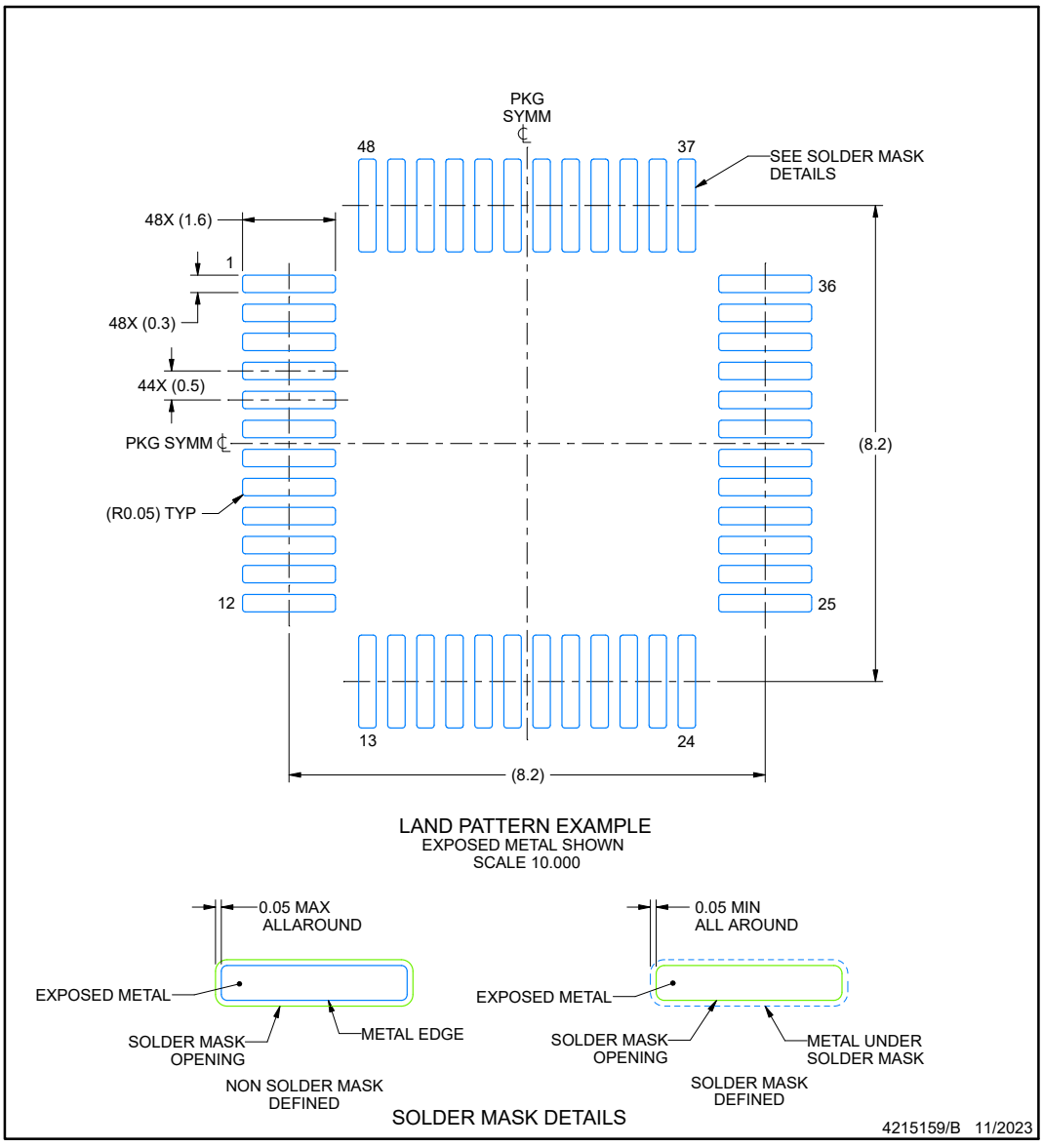
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.

Texas Instruments
www.ti.com

EXAMPLE BOARD LAYOUT

PT0048A — **LQFP - 1.6 mm max height**

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

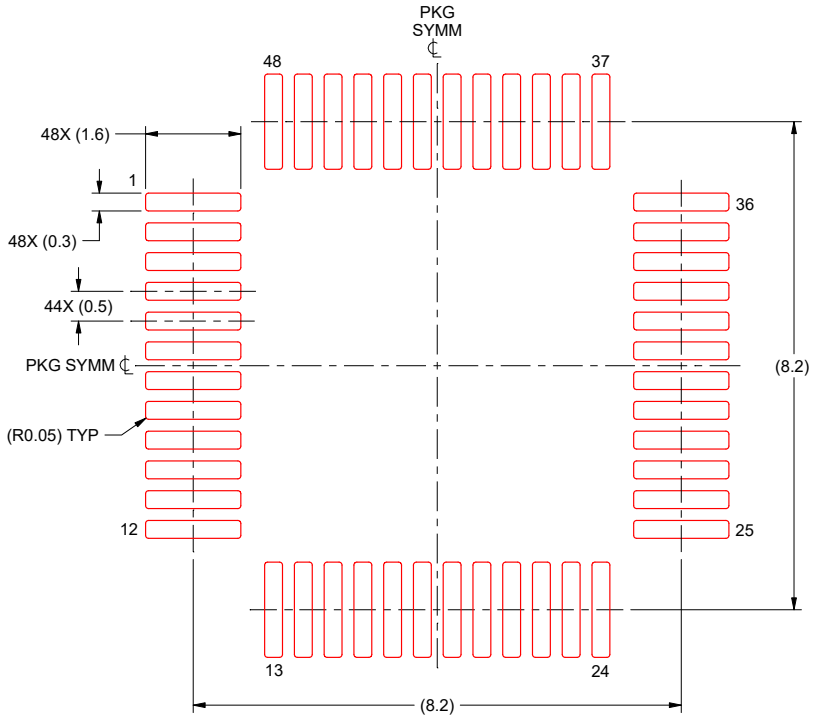
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

PT0048A — **LQFP - 1.6 mm max height**

LOW PROFILE QUAD FLATPACK

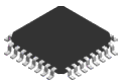


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

4215159/B 11/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

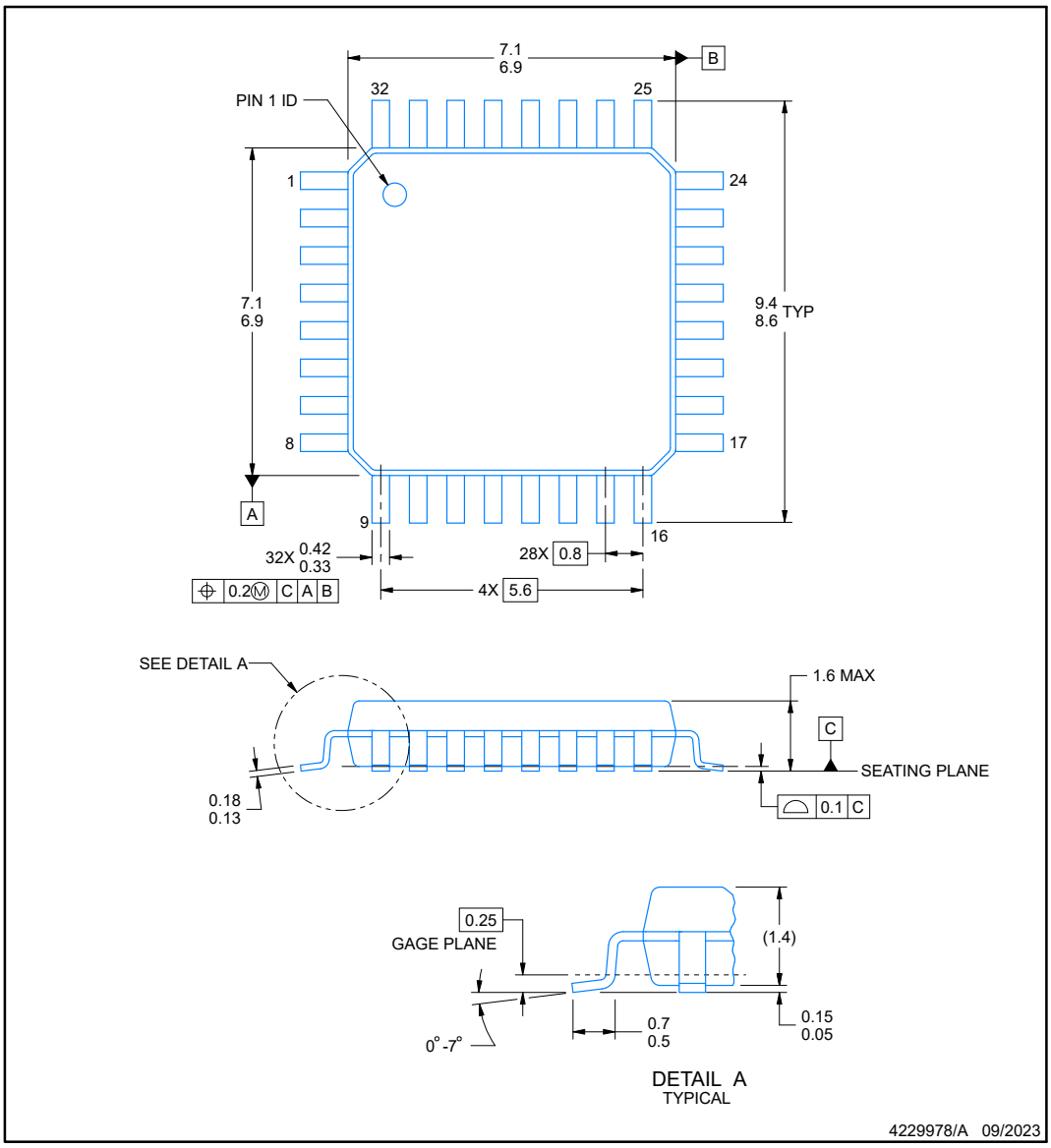


PACKAGE OUTLINE

VFC0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

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ADVANCE INFORMATION

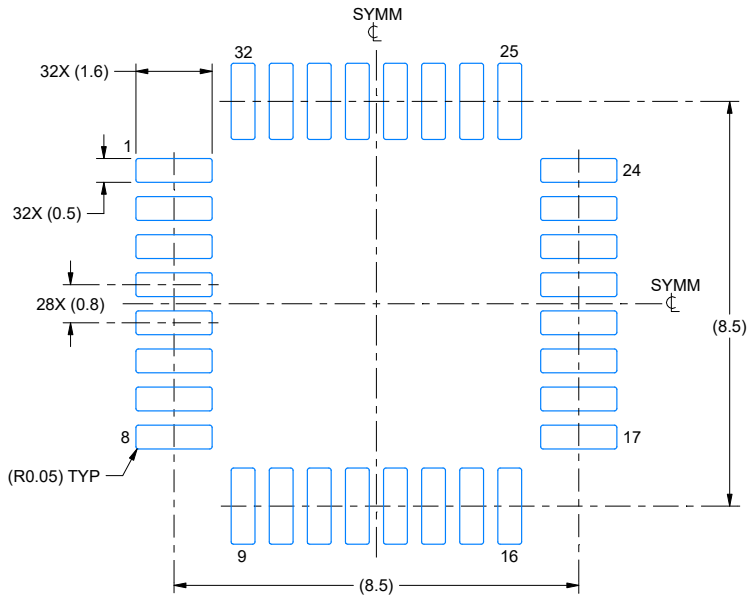
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

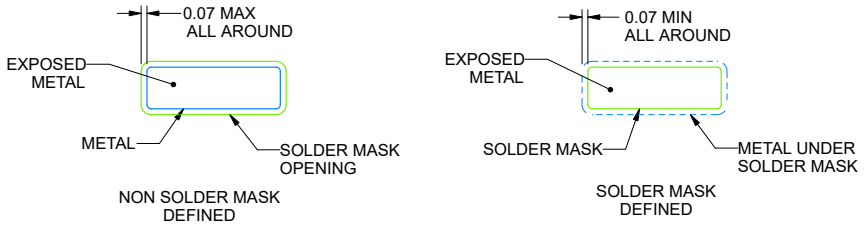
VFC0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4229978/A 09/2023

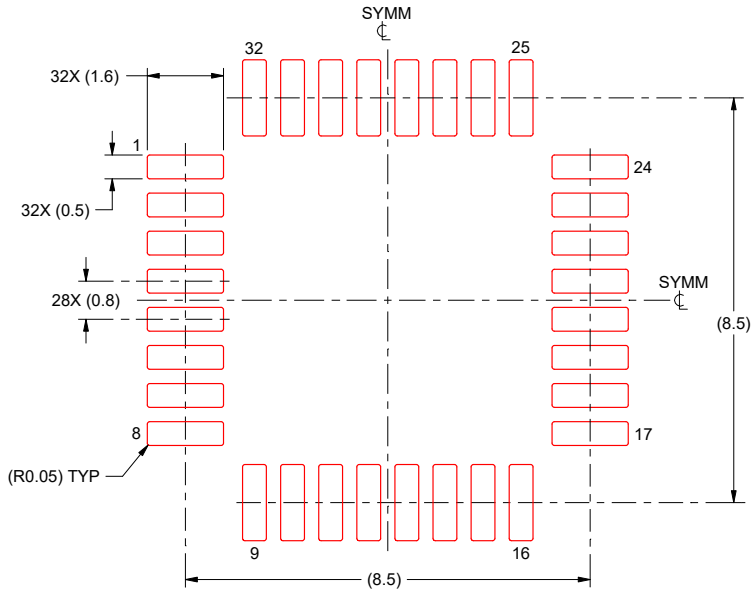
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VFC0032A — **LQFP - 1.6 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE 8X

4229978/A 09/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

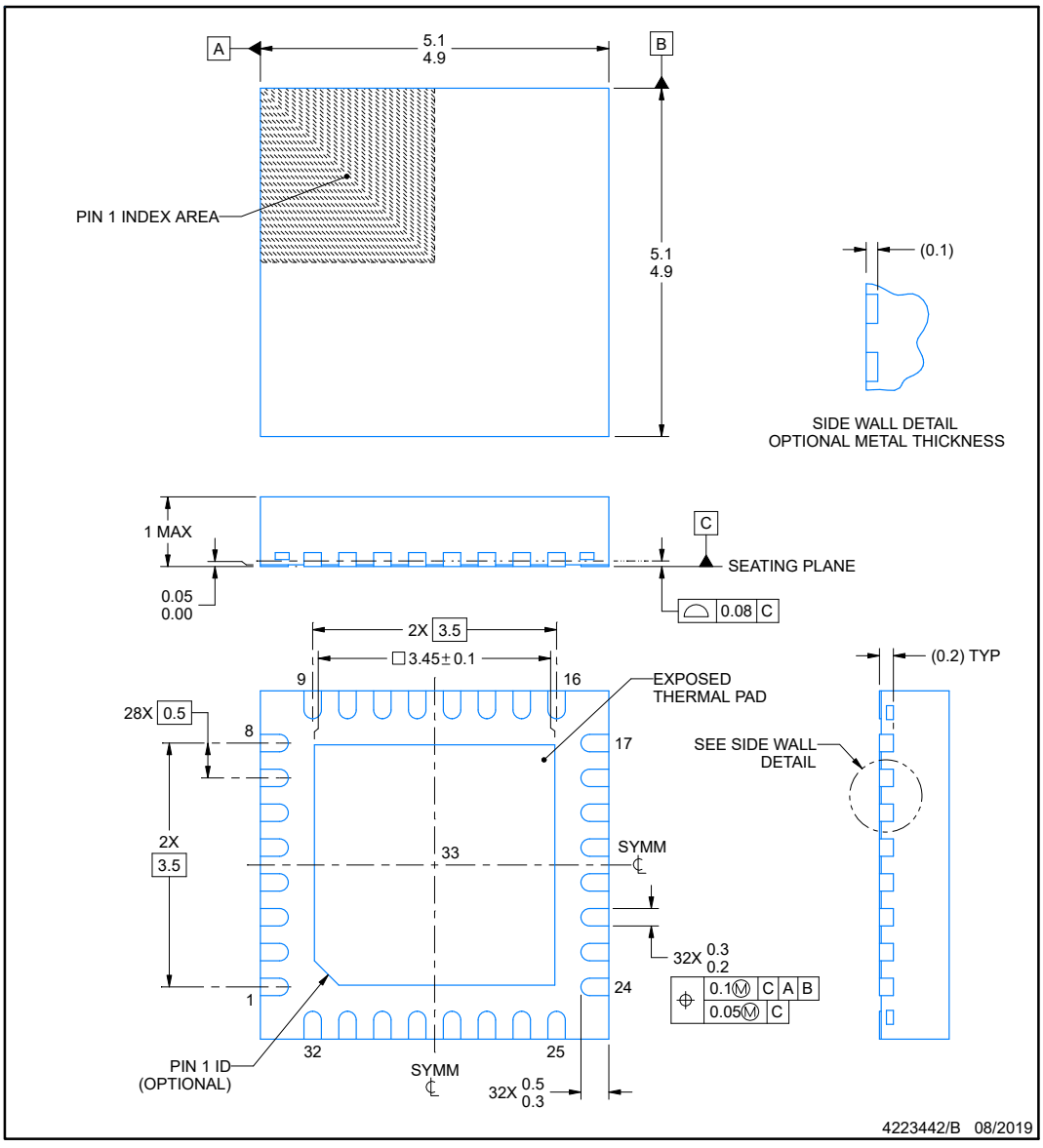
ADVANCE INFORMATION

PACKAGE OUTLINE

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



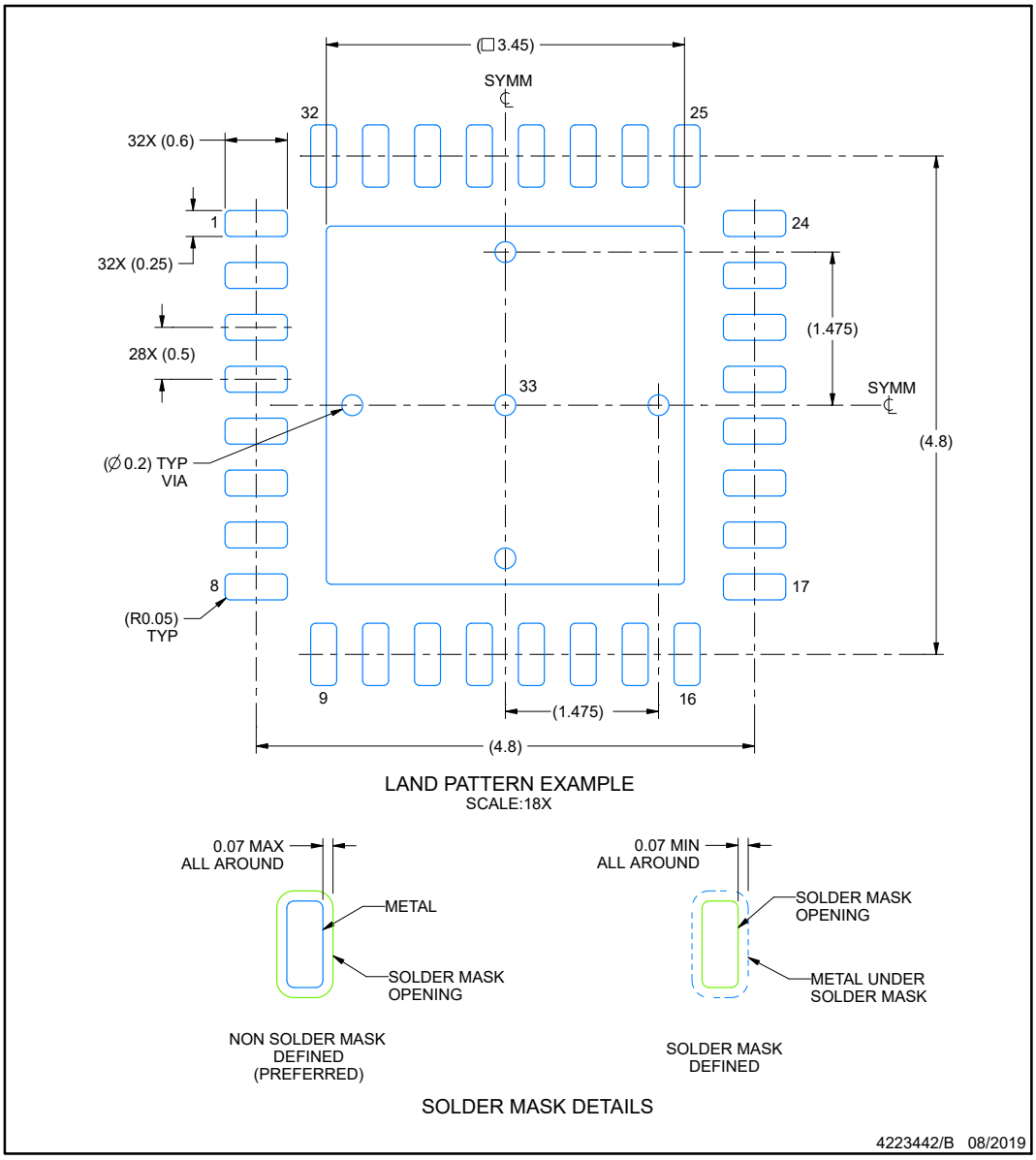
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

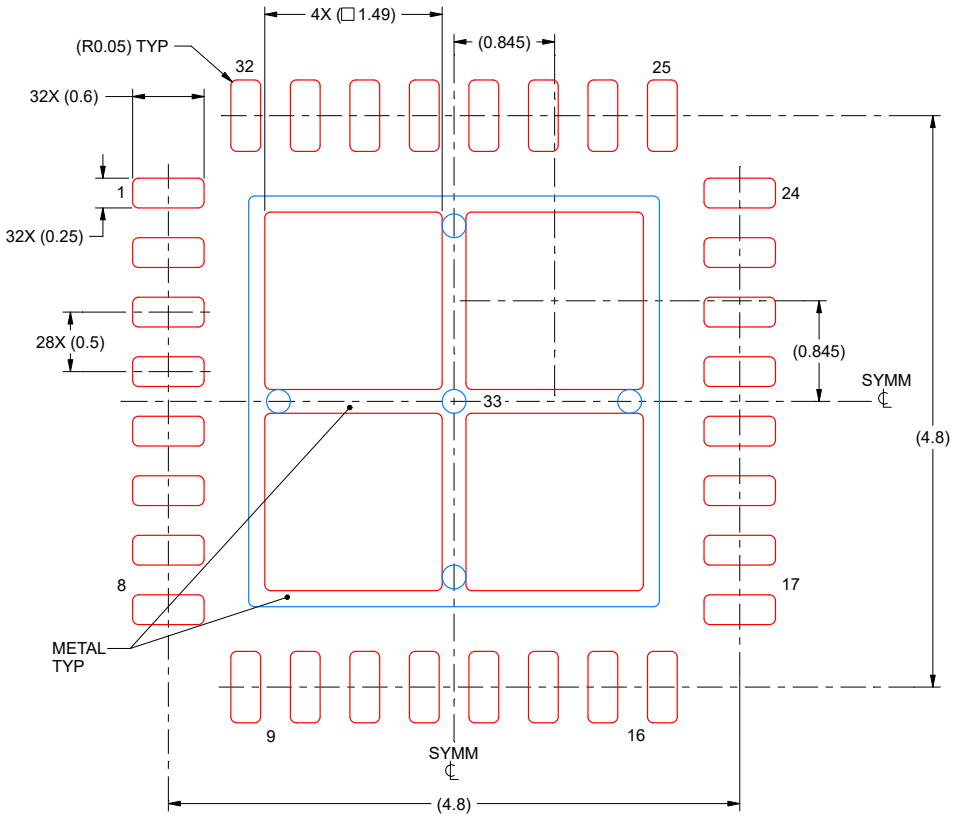
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RHB0032E — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

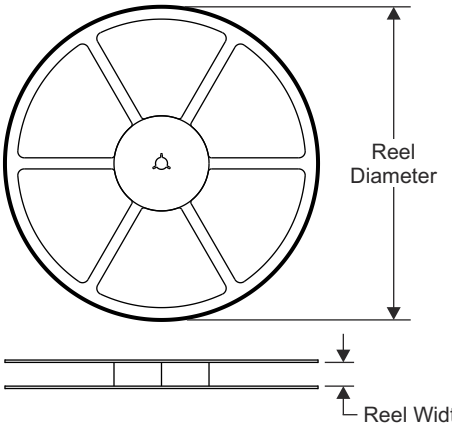
4223442/B 08/2019

NOTES: (continued)

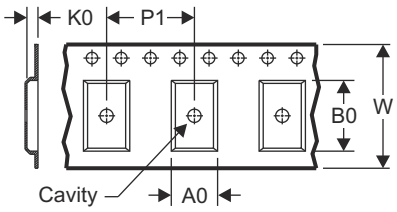
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

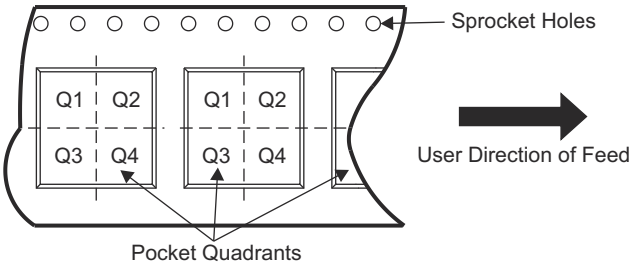


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

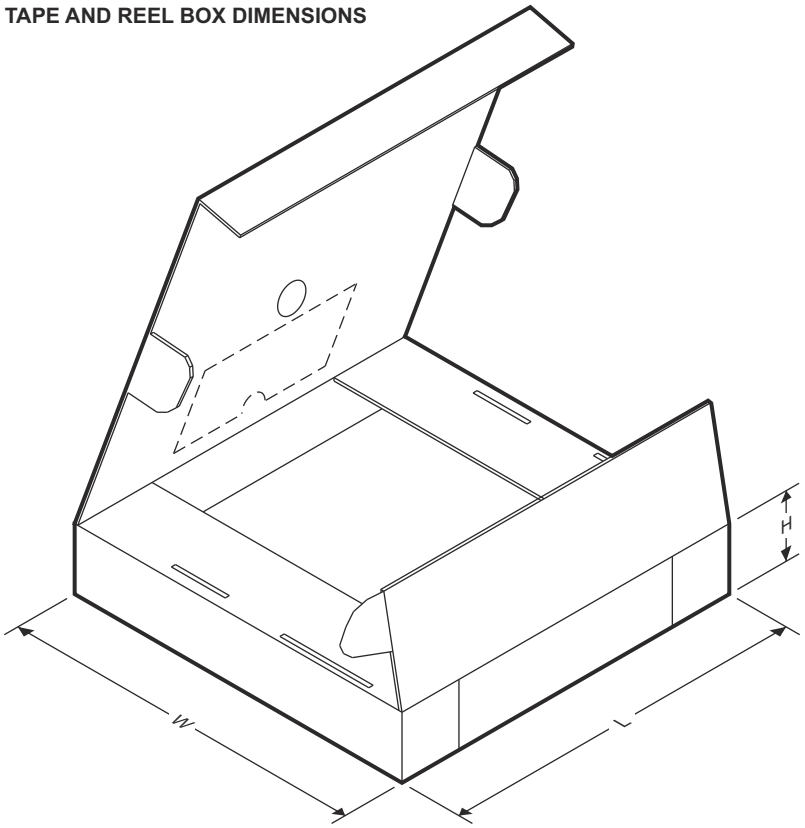
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XF28E120SCTRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
XF28E120SBTRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

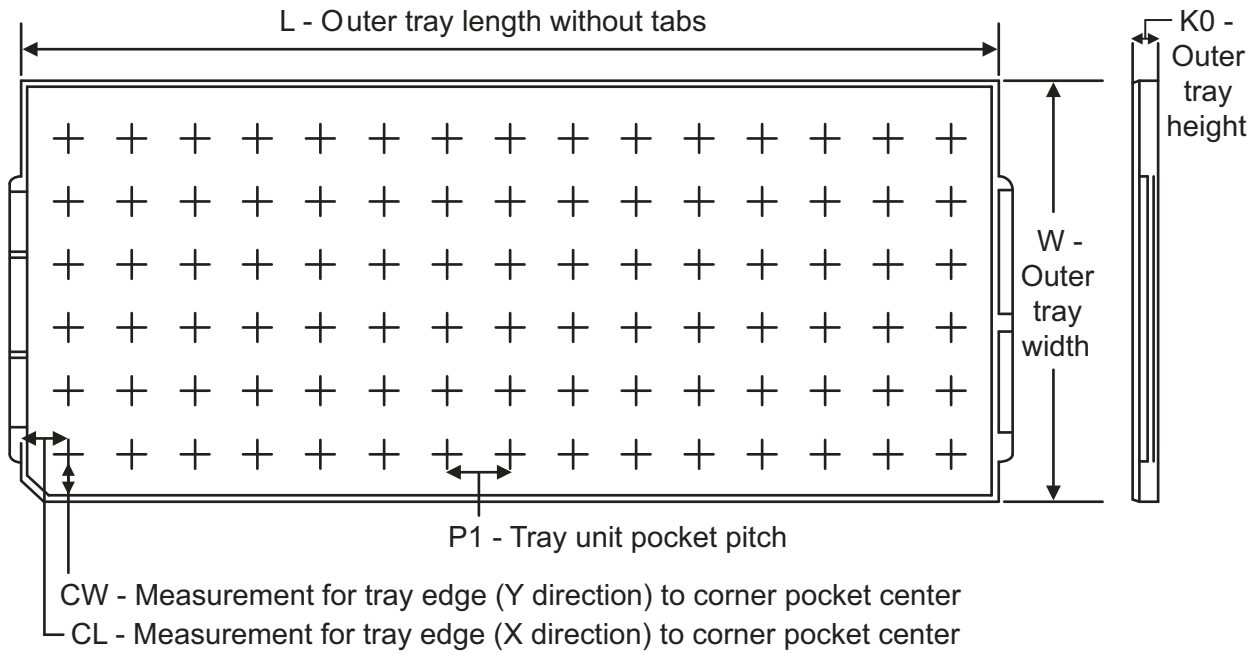
ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XF28E120SCTRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
XF28E120SBTRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

Device	Package Type	Package Name	Pins	SPQ	Unit Array Matrix	Max Temp. (Deg C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
XF28E120SCTPT	LQFP	PT	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
XF28E120SCTVFC	LQFP	VFC	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
XF28E120SBTRHBR	Active	Production	VQFN (RHB) | 32	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
XF28E120SCTPT	Active	Preproduction	LQFP (PT) | 48	250 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 105	
XF28E120SCTVFC	Active	Preproduction	LQFP (VFC) | 32	250 | JEDEC TRAY (10+1)	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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