

# CSD965200 Synchronous Buck Smart Power Stage

## 1 Features

- 100A peak current capability
- Thermally Enhanced Package (TEP)
- $R_{\theta JC (top)} < 0.4^{\circ}C/W$
- Reduced switch-node ringing
- Integrated clamping circuitry for avalanche free operation
- High-frequency operation (up to 2MHz)
- Temperature compensated bi-directional current sense with current mode reporting ( $5\mu A/A$ )
- Native TLVR support
- Body braking mode (BB)
- Forced continuous conduction mode (FCCM) operation
- Diode Emulation Mode (DEM)
- 4mm x 6mm QFN industry common footprint package
- Green, RoHS compliant without exemption
- Limp Mode Fault Reporting
  - TAO and IOUT signal handshaking scheme to report specific fault to controller
- Fault detection
  - High-side short (HSS)
- Fault protection
  - Over temperature (OT)
  - Cycle-by-cycle negative over current limiting (NOC)
  - High-Side and Low-Side positive over current protection
  - BOOT UVLO

## 2 Applications

- [Data center & enterprise computing rack server](#)
- [Hardware accelerator](#)
- [Network interface card \(NIC\)](#)
- [ASIC and high performance client](#)
- [ASIC power for networking and communications](#)
- [High phase count buck regulator solutions](#)

## 3 Description

The CSD965200 power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter. This product integrates the driver IC and power MOSFETs into one Pb-free monolithic design to complete the power stage switching function. There are VIN bypass capacitors integrated into the package for minimum loop inductance and improved ringing. This combination produces high-current, high-efficiency, and high-speed switching capability in a small industry standard 4mm x 6mm footprint.

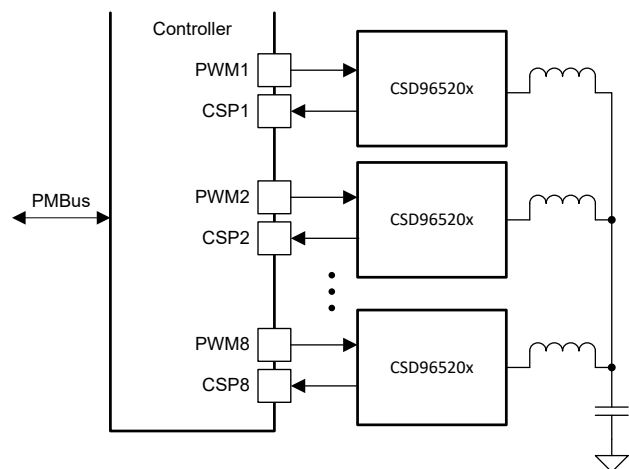
Furthermore, CSD965200 is built with a Thermally Enhanced Package (TEP) using additional top side cooling for improved heat dissipation. TEP yields performance benefit, especially at high load currents.

CSD965200 integrates accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. This power stage also includes cycle-by-cycle current limiting and protection based on HS FET current sense, HS FET short and over temperature detection and protection, negative over current detection, open pin detection, handshaking and system diagnosis when paired with the TPS536xx and TPS537xx series controllers.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
CSD965200	VBR (VQFN, 34)	4mm x 6mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

## 4 Device and Documentation Support

### 4.1 Device Support

#### 4.1.1 Third-Party Products Disclaimer

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### 4.2 Documentation Support

#### 4.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 4.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 4.5 Trademarks

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### 4.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 4.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 5 Revision History

DATE	REVISION	NOTES
October 2025	*	Initial release

## 6 Mechanical, Packaging, and Orderable Information

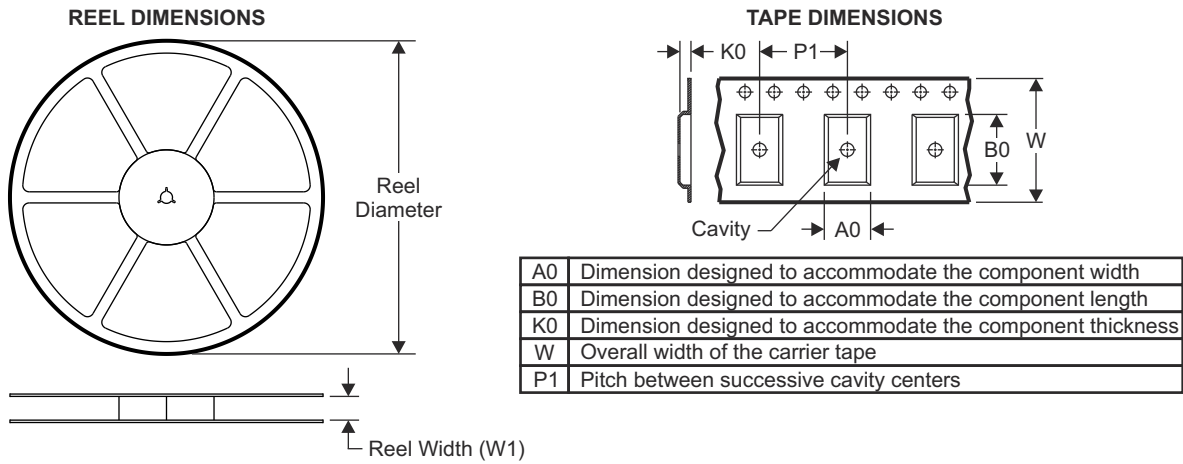
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 6.1 Package Option Addendum

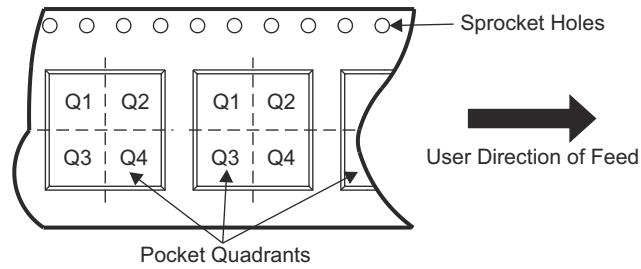
Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
CSD965200VBRR	PREVIEW	QFN	VBR	34	2500	Green	NiPdAu	Level-3-260C-168 hr	-40 to 125	965200

- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.  
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## 6.2 Tape and Reel Information



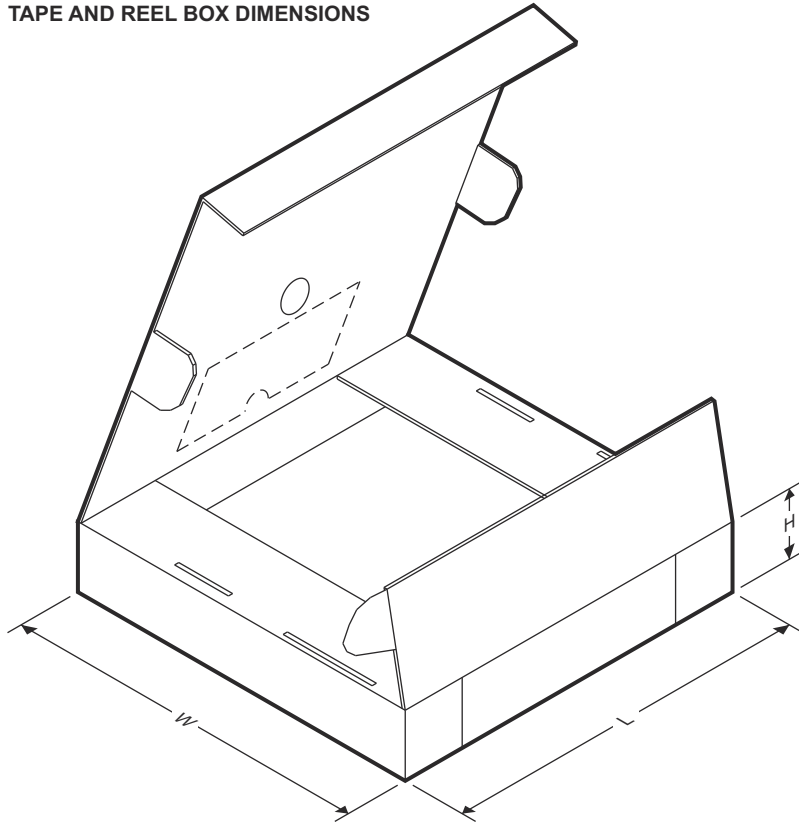
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD965200VBRR	QFN	VBR	34	2500	330	12.4	5.30	6.30	1.20	8.00	12.00	Q1

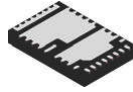
ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD965200VBRR	QFN	VBR	34	2500	367	367	38

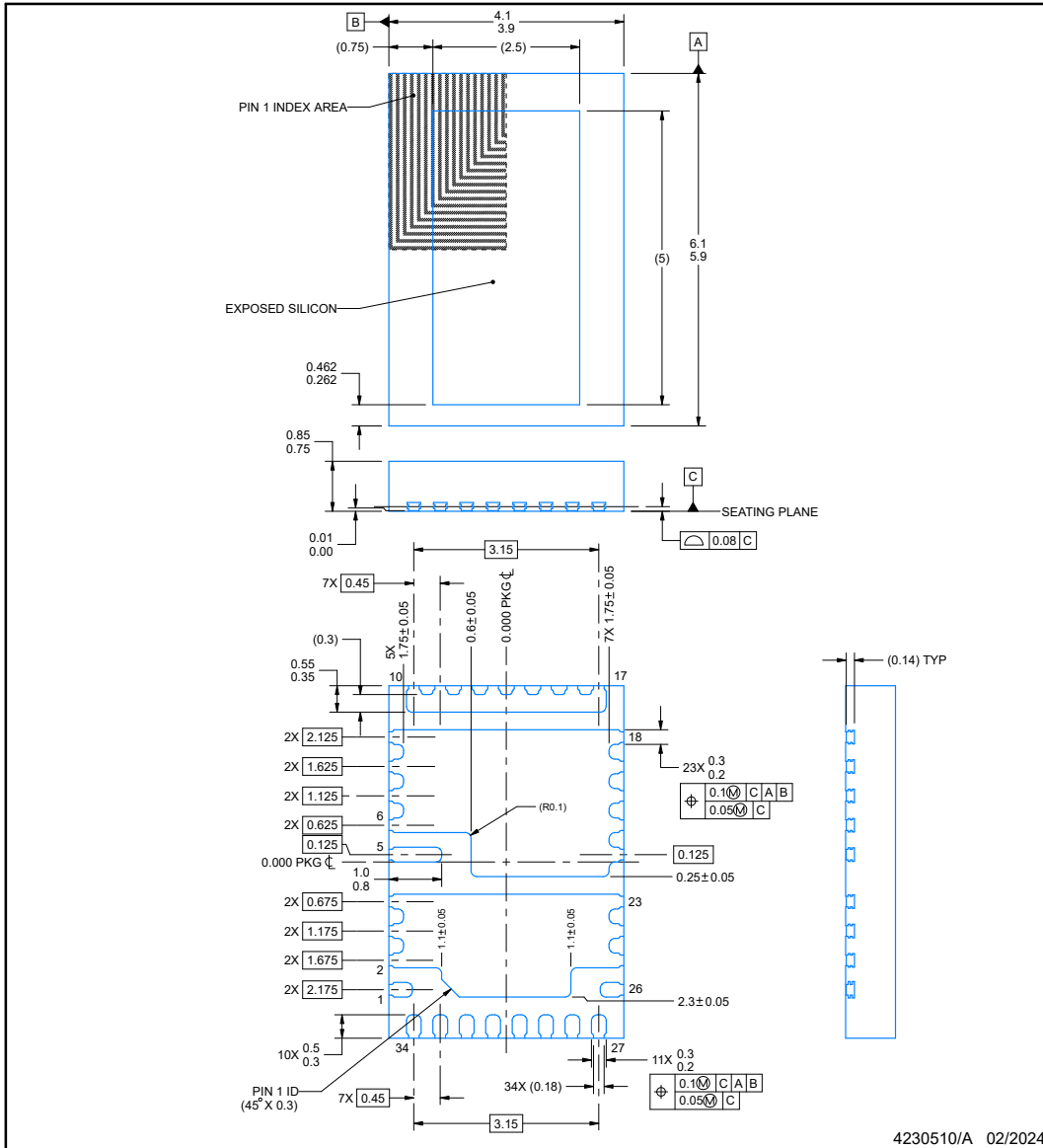


**PACKAGE OUTLINE**

**VBR0034A**

**WQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

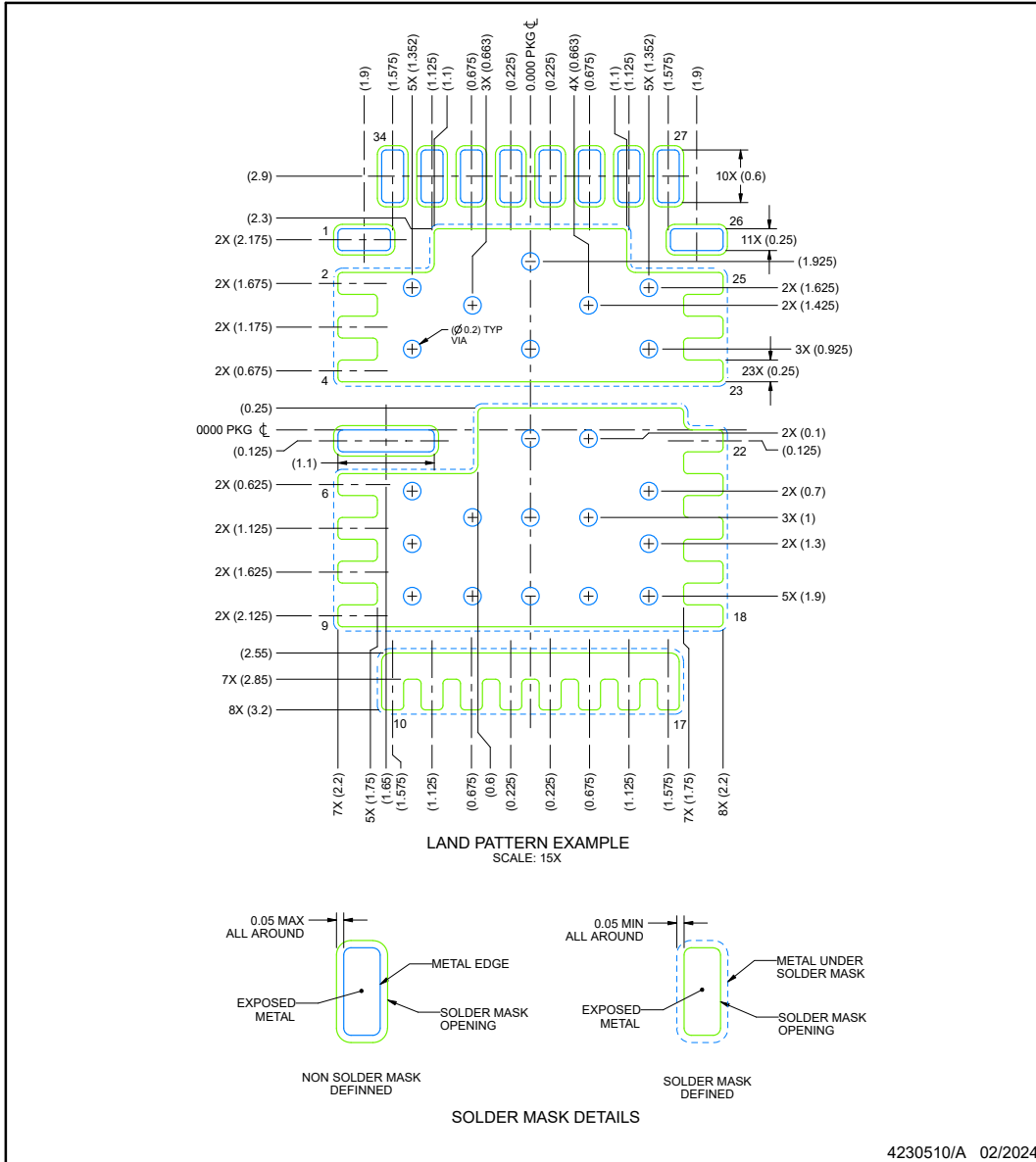
**ADVANCE INFORMATION**

**EXAMPLE BOARD LAYOUT**

**VBR0034A**

**WQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

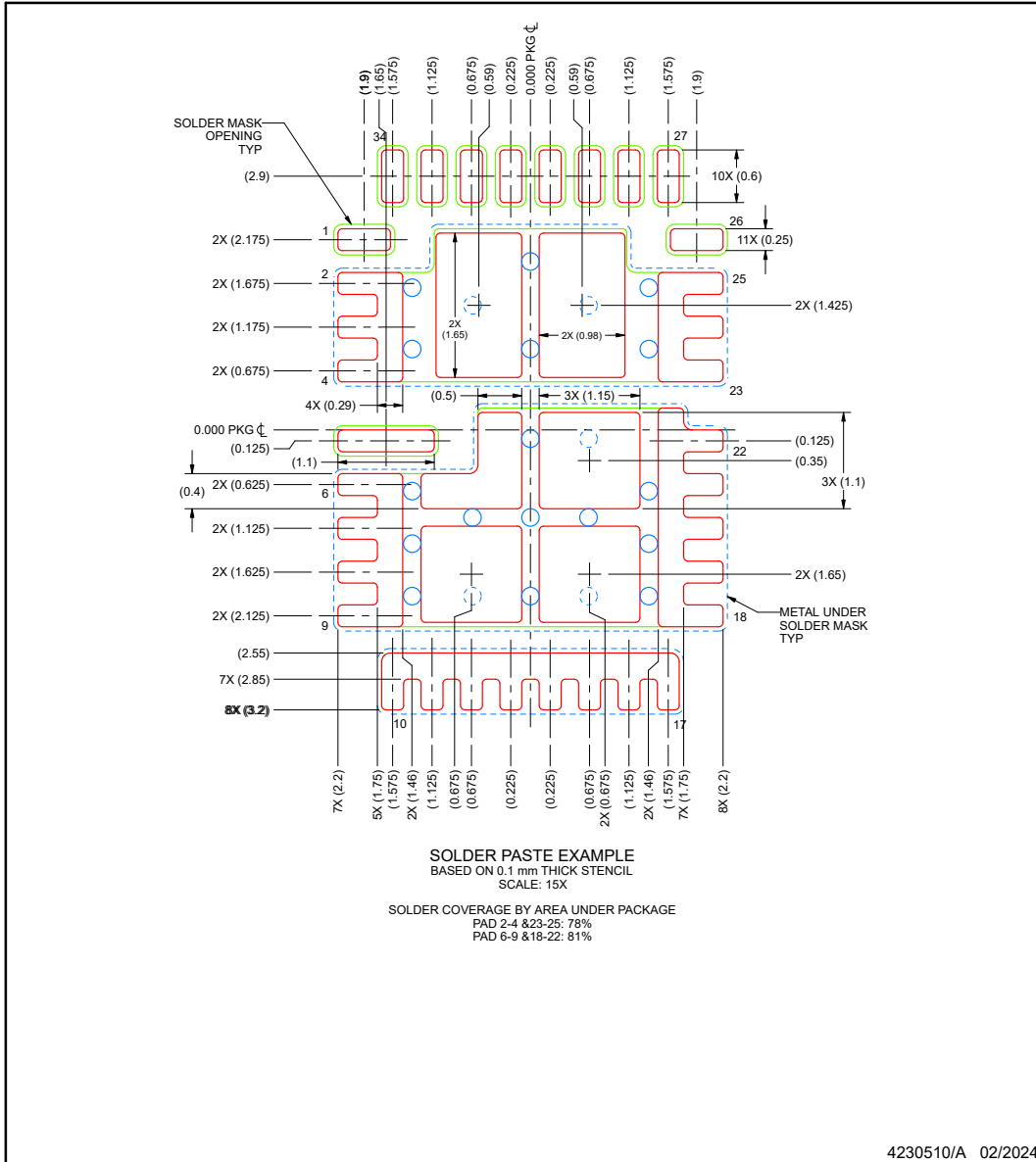
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN**

**VBR0034A**

**WQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**ADVANCE INFORMATION**

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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