DRV7167A 100-V, 70A Half-Bridge GaN Motor Driver Power Stage

1 Features

- 100V, Half-bridge GaN Motor Driver power stage with integrated driver supporting 48V systems
- Low GaN on-state resistance
  - 2.2 mΩ $R_{DS(ON)}$ (per FET) at T_A=25°C
- Enables efficient and high density power conversion
  - High output current capability: 70A_{rms}, 250A (pulsed, 300 µs)
  - Supports upto 500 kHz PWM switching frequency
  - Excellent propagation delay (20ns typical) and matching (2ns typical)
  - Turn-on and turn-off slew-rate control for both FETs
  - Zero-voltage detection (ZVD) reporting for optimizing dead-time in soft switching applications
  - Single PWM input option for IO-limited controllers
- 5V external bias power supply
  - Supports 3.3V and 5V input logic levels
- Integrated protection features
  - Short circuit protection in Independent Inout Mode (IIM)
  - Internal bootstrap supply voltage regulation to prevent GaN FET Overdrive
  - V_{DS} monitoring based cycle-by-cyle short-circuit protection
  - Fault indication for over-temperature, under-voltage and short-circuit events
  - Supply rail undervoltage lockout protection
- Package optimized for easy PCB layout
  - Exposed top QFN package for top-side cooling
  - Large GND pad for bottom-side cooling

2 Applications

- Humanoid Robots
- Collaborative robots
- Mobile Robots (AGV/AMR)
- 48V Servo Drives
- Drones
- E-bikes, E-Scooters, E-Mobility
- Power tools

3 Description

The DRV7167A is a 100V half-bridge power stage, with integrated gate-driver and enhancement-mode Gallium Nitride (GaN) FETs. The device consist of two 100V GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration.

GaN FETs provide significant advantages for power conversion as they have zero reverse recovery and very small input capacitance C_{ISS} and output capacitance C_{OSS}. All the devices are mounted on a completely bond-wire free package platform with minimized package parasitic elements. The DRV7167A is available in 7.0mm × 4.5mm × 0.89mm lead-free packages and can be easily mounted on PCBs.

The TTL logic compatible inputs can support 3.3V and 5V logic levels regardless of the GVDD voltage. A proprietary bootstrap voltage regulation technique ensures the gate voltages of the enhancement mode GaN FETs are within a safe operating range. The device supports turn-on and turn-off slew-rate control for both FETs, single PWM mode for use with IO-limited controllers, short-circuit protection (SCP) , Over-Temperature Detection (OTD) and zero-voltage detection (ZVD) reporting to minimize third quandrant condution time.

The device extends advantages of discrete GaN FETs by offering a more user-friendly interface. It is an ideal solution for applications requiring high-frequency, high-efficiency operation in a small form factor.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM) (3)
DRV7167A(2)	VBN (VQFN, 18)	7.00mm × 4.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Advance information. The products are in sampling and preproduction phase.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.

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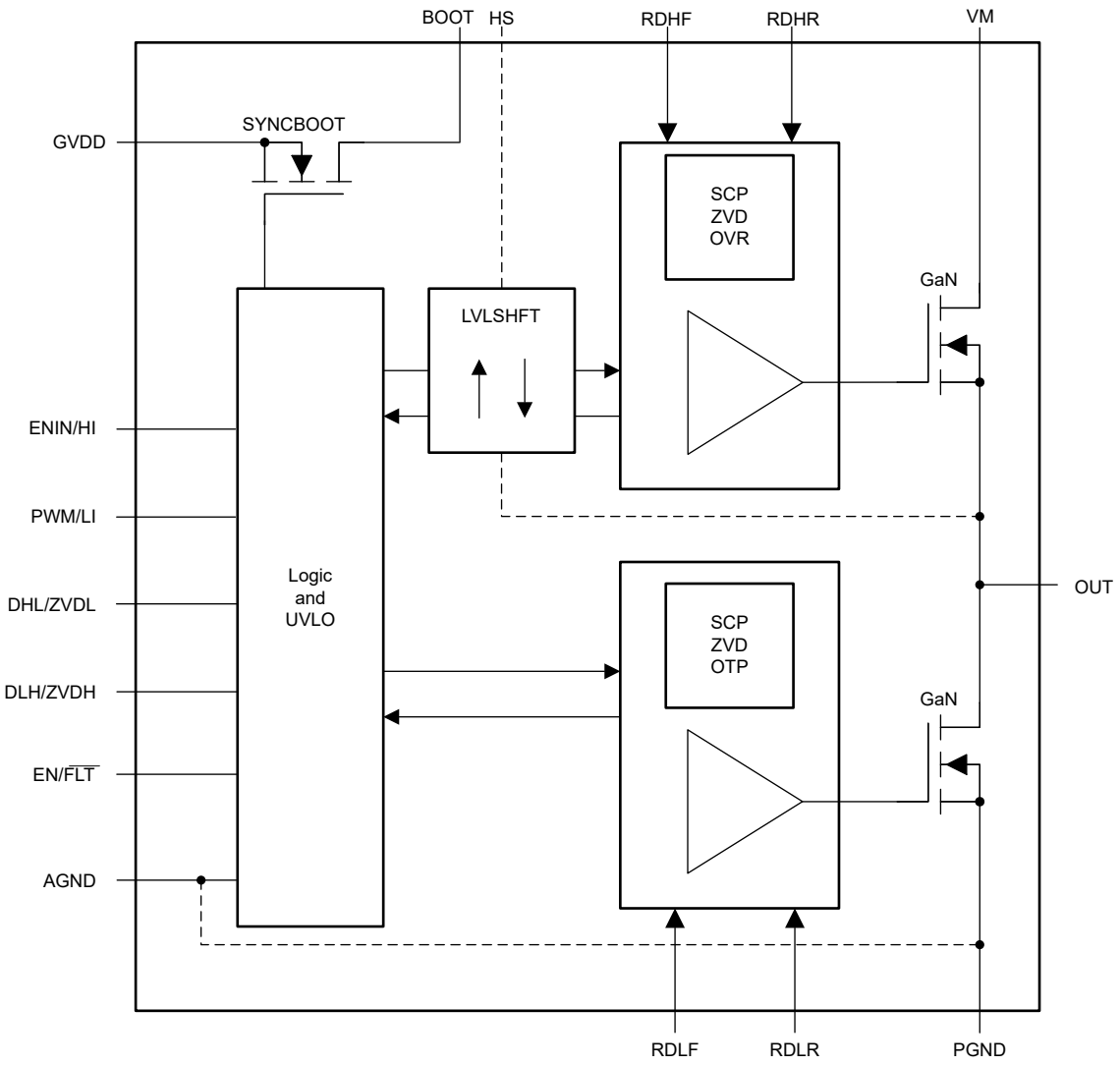

Table of Contents

ADVANCE INFORMATION

4 Pin Configuration and Functions

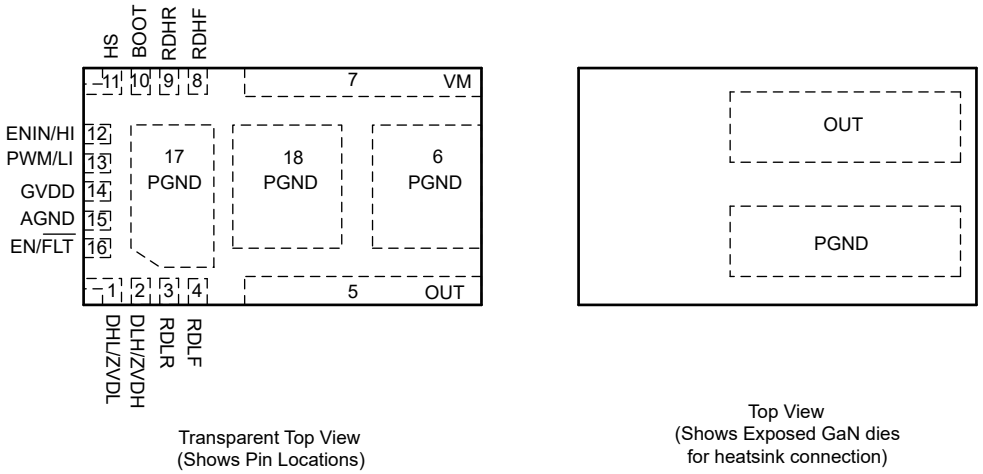

Figure 4-1. VBN Package, 18-Pin VQFN (Top View)

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Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
DHL/ZVDL	1	IO	In PWM mode, sets the dead time for high-to-low transition by connecting a resistor to AGND. In IIM mode, zero-voltage detection output signal to indicate if low-side FET achieves zero-voltage switching in current switching cycle. Note: Do not Tie ZVDL to GVDD.
DLH/ZVDH	2	IO	In PWM mode, sets the dead time for low-to-high transition by connecting a resistor to AGND. In IIM mode, zero-voltage detection output signal to indicate if high-side FET achieves zero-voltage switching in current switching cycle.
RDLR	3	I	Sets the slew-rate control for LS FET turn-on through resistor to AGND.
RDLF	4	I	Sets the slew-rate control for LS FET turn-off through resistor to AGND. Float this pin to enable PWM mode.
OUT	5	P	Switching node. Internally connected to HS pin.
PGND	6, 17, 18	G	Power ground. Low-side GaN FET source. Internally connected to low-side GaN FET source.
VM	7	P	Input voltage pin. Internally connected to high-side GaN FET drain.
RDHF	8	I	Sets the slew-rate control for HS FET turn-off through resistor to HS.
RDHR	9	I	Sets the slew-rate control for HS FET turn-on through resistor to HS. Note: Do not float RDHR pin.
BOOT	10	P	High-side gate driver bootstrap rail. Connect bypass capacitor to HS.
HS	11	P	High-side GaN FET source connection.
ENIN/HI	12	I	In PWM mode, enables gate-drive for both high-side and low-side FETs. In IIM mode, high-side gate driver control input.
PWM/LI	13	I	In PWM mode, PWM input. In IIM mode, low-side gate driver control input.
GVDD	14	P	5V device power supply.
AGND	15	G	Analog ground. Internally connected to low-side GaN FET source.
EN/$\overline{\text{FLT}}$	16	IO	Chip enable and Fault output pin. Connect to microcontoller output or to GVDD through 4.7 kΩ resistor.

(1) I = Input, O = Output, IO = Input/Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

See (1)

PARAMETER	MIN	MAX	UNIT
VM to PGND (test for 24hrs)	0	100	V
VM to PGND (up to 10,000 5ms pulses at 150°C)		120	V
BOOT to AGND		106	V
HS to AGND		100	V
HS to PGND (up to 10,000 5ms pulses at 150°C)		120	V
HI to AGND	-0.3	6	V
LI to AGND	-0.3	6	V
HI to AGND, 20ns transients, < 1Mhz frequency	-2	6	V
LI to AGND, 20ns transients, < 1Mhz frequency	-2	6	V
GVDD to AGND	-0.3	6	V
BOOT to HS	-0.3	6	V
BOOT to GVDD	0	100	V
OUT to PGND		100	V
IOUT from OUT pin (Continuous), T_J = 125℃		70	A
IOUT from OUT pin (Pulsed, 300 µs), T_J = 25℃		250	A
Junction Temperature, T_J	-40	175	°C
Storage Temperature, T_{stg}	-40	175	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
				V
		Charged-device model (CDM), corner pins, per JEDEC specification JESD22-C101(2)	±750	V
		Charged-device model (CDM), internal pins, per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Unless otherwise noted, voltages are with respect to AGND

		MIN	NOM	MAX	UNIT
GVDD		4.5	5	5.5	V
PWM/LI, ENIN/HI, EN Low Level Input				1	V
PWM/LI, ENIN/HI, EN High Level Input		3		VM+0.3	V
BOOT		V_{HS}+ 4		V_{HS}+ 5.5	V
f_{MAX}	Maximum switching frequency (50% Duty Cycle)			500	kHz
t_{PW}	Minimum input pulse width supported	10			ns
HS, OUT Slew rate(1)				TBD	V/ns

(1) Determined through design and characterization. Not tested in production.

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5.4 Thermal Information_DRV7167A

THERMAL METRIC (1)		DRV7167 QFN 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JC(Bot)}$	Junction-to-case (bottom) thermal resistance, low-side FET to PGND	5.4	°C/W
	Junction-to-case (bottom) thermal resistance, high-side FET to VM	6.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953 .

5.5 Electrical Characteristics

Unless otherwise noted, voltages are with respect to AGND and typical specifications are at 25°C (1); -40°C ≤ T_J ≤150°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER STAGE_DRV7167A						
$R_{DS(ON)HS}$	High-side GaN FET on-resistance	LI=0V, HI=GVDD=5V, BOOT-HS=5V, I(VM-OUT)=16A, T_J = 25°C		2.3	3.1	mΩ
$R_{DS(ON)LS}$	Low-side GaN FET on-resistance	LI=GVDD=5V, HI=0V, BOOT-HS=5V, I(OUT-PGND)=16A, T_J = 25°C		2.2	3	mΩ
V_{SD}	GaN source to drain 3rd quadrant conduction drop	I_{SD} = 500 mA, V_M floating, V_{GVDD} = 5 V, HI = LI = 0V		1.5		V
$I_{L-VM-OUT}$	Leakage from VM to OUT when the high-side GaN FET and low-side GaN FET are off	VM = 80V, OUT=0V, HI = LI = 0V, V_{GVDD} = 5V, T_J=25°C		10	150	µA
$I_{L-VM-OUT}$	Leakage from VM to OUT when the high-side GaN FET and low-side GaN FET are off	VM = 80V, OUT=0V, HI = LI = 0V, V_{GVDD} = 5V, T_J=90°C		20	300	µA
$I_{L-OUT-GND}$	Leakage from OUT to GND when the high-side GaN FET and low-side GaN FET are off	OUT = 80V, HI = LI = 0V, V_{GVDD} = 5V, T_J=25°C		10	150	µA
$I_{L-OUT-GND}$	Leakage from OUT to GND when the high-side GaN FET and low-side GaN FET are off	OUT = 80V, HI = LI = 0V, V_{GVDD} = 5V, T_J=90°C		20	300	µA
C_{ISS}	Input Capacitance of high side or low side HEMT	V_{DS}=50V, V_{GS}= 0V (HI = LI = 0V), T_J=25°C		1700		pF
C_{OSS}	Output Capacitance of high-side GaN FET or low-side GaN FET	V_{DS}=50V, V_{GS}= 0V (HI = LI = 0V), T_J=25°C		570		pF
$C_{OSS(ER)}$	Output Capacitance of high-side GaN FET or low-side GaN FET - Energy Related	V_{DS}=0 to 50V, V_{GS}= 0V (HI = LI = 0V), T_J=25°C		700		pF
$C_{OSS(TR)}$	Output Capacitance of high-side GaN FET or low-side GaN FET - Time Related	V_{DS}=0 to 50V, V_{GS}= 0V (HI = LI = 0V), T_J=25°C		880		pF
C_{RSS}	Reverse Transfer Capacitance of high side or low side HEMT	V_{DS}=50V, V_{GS}= 0V (HI = LI = 0V), T_J=25°C		4.3		pF
Q_G	Total Gate Charge of high side or low side HEMT	V_{DS}=50V, I_D= 16A, V_{GS}= 5V, T_J=25°C		12		nC
Q_{GD}	Gate to Drain Charge of high side or low side HEMT	V_{DS}=50V, I_D= 16A, T_J=25°C		1.2		nC
Q_{GS}	Gate to Source Charge of high side or low side HEMT	V_{DS}=50V, I_D= 16A, T_J=25°C		3.9		nC
Q_{OSS}	Output Charge (sum of high side HEMT, low side HEMT and gate-driver HV-Well charge)	V_{DS}=50V, I_D= 16A, T_J=25°C		90		nC
Q_{RR}	Source to Drain Reverse Recovery Charge			0		nC
t_{HIPLH}	Propagation delay: HI Rising(2)	LI=0V, GVDD=5V, BOOT-HS=5V, VM=48V		15	25	ns

ADVANCE INFORMATION

Unless otherwise noted, voltages are with respect to AGND and typical specifications are at 25°C [(1)]; -40°C ≤ T_J ≤150°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HIPHL}	Propagation delay: HI Falling[(2)]	LI=0V, GVDD=5V, BOOT-HS=5V, VM=48V		15	25	ns
t_{LIPLH}	Propagation delay: LI Rising[(2)]	HI=0V, GVDD=5V, BOOT-HS=5V, VM=48V		15	25	ns
t_{LIPHL}	Propagation delay: LI Falling[(2)]	HI=0V, GVDD=5V, BOOT-HS=5V, VM=48V		15	25	ns
t_{MON}	Delay Matching: LI high & HI low[(2)]			2	5	ns
t_{MOFF}	Delay Matching: LI low & HI high[(2)]			2	5	ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			10		ns
INPUT PINS (ENIN/HI, PWM/LI, EN)						
V_{IH}	High-Level Input Voltage Threshold	Rising Edge			2.1	V
V_{IL}	Low-Level Input Voltage Threshold	Falling Edge	1.2			V
V_{HYS}	Hysteresis between rising and falling threshold			300		mV
R_I	Input pull down resistance		200	300	500	kΩ
OUTPUT PINS (ZVDx)						
V_{OL}	Low level output voltage	I_{OL} = 3 mA			0.25	V
V_{OH}	High level output voltage	I_{OL} = -1.5 mA to 0 mA	2.6		3.5	V
UNDER/OVER VOLTAGE PROTECTION						
V_{GVDDR}	V_{GVDD} Rising edge threshold	Rising	3.3	3.6	3.9	V
V_{GVDDF}	V_{GVDD} Falling edge threshold		3.1	3.4	3.7	V
$V_{GVDD(hyst)}$	V_{GVDD} UVLO threshold hysteresis			200		mV
V_{BOOTR}	BOOT Rising edge threshold	Rising	3.3	3.6	3.9	V
V_{BOOTF}	BOOT Falling edge threshold		3.1	3.4	3.7	V
$V_{BOOT(hyst)}$	BOOT UVLO threshold hysteresis			200		mV
V_{BOOTth}	BOOT Regulation Voltage thresholds		4.5		5.3	V
t_{PWRUP}	Power Up time after Digital Reset				50	µs
SYNCRONOUS BOOTSTRAP						
V_{DH}	Forward voltage drop	$I_{VDD-BOOT}$ = 5mA		40		mV
		$I_{VDD-BOOT}$ = 50mA		400		mV
t_{SS}	BOOT power up time (With LI=High)	C_{BOOT} = 220 nF		2.2		µs
t_{SS}	BOOT power up time (With LI=High)	C_{BOOT} = 1 µF		10		µs
SUPPLY CURRENTS						
I_{GVDD}	GVDD Quiescent Current	LI = HI = 0V, GVDD = 5V, EN=0		0.3		mA
I_{GVDD}	GVDD Quiescent Current	LI = HI = 0V, GVDD = 5V		0.9	3.5	mA
I_{GVDD}	GVDD Quiescent Current	LI=GVDD=5V, HI=0V		1.8	7	mA
I_{GVDDO}	Total GVDD Operating Current	f = 500 kHz, 50% Duty cycle, V_M = 48V		12	15	mA
I_{BOOT}	BOOT Quiescent Current	LI = HI = 0V, GVDD = 5V, BOOT-HS = 5V		0.5	1	mA
I_{BOOT}	BOOT Quiescent Current	LI=0V, HI=GVDD=5V, BOOT-HS=5V, VM=48V		0.8	3.5	mA
I_{BOOTO}	BOOT Operating Current	f = 500 kHz, 50% Duty cycle, GVDD = 5V, BOOT-HS = 5V, V_M = 48V		5.6	8	mA
SLEW RATE CONTROL (EFFECTIVE GATE RESISTANCE)						
Rgfh	RDHF = 0 Ω	Voltage across driver FET = 1.2V		0.3		Ω
	RDHF = 4 kΩ			1.3		
	RDHF = 8 kΩ			2.6		
	RDHF =16 kΩ			5.3		
Rgfl	RDLF = 0 Ω	Voltage across driver FET = 1.2V		0.3		Ω
	RDLF = 4 kΩ			1.3		
	RDLF = 8 kΩ			2.6		
	RDLF =16 kΩ			5.3		

ADVANCE INFORMATION

Unless otherwise noted, voltages are with respect to AGND and typical specifications are at 25℃ (1); -40℃ ≤ T_J ≤150℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rgrh	RDHR = 0 Ω	Voltage across driver FET = 1.2V		0.8		Ω
	RDHR = 4 kΩ			3.6		
	RDHR = 8 kΩ			7		
	RDHR =16 kΩ			14		
Rgrl	RDLR = 0 Ω	Voltage across driver FET = 1.2V		0.8		Ω
	RDLR = 4 kΩ			3.6		
	RDLR = 8 kΩ			7		
	RDLR =16 kΩ			14		
DEAD TIME CONTROL						
t_{DEAD_MIN}	Minimum Dead Time	DLH, DHL = 0Ω; Minimum Dead time setting.	5	7.5	10	ns
t_{DEAD_MAX}	Maximum Dead Time	DLH, DHL = 100kΩ; Maximum Dead time setting.	32	40	48	ns
OCP						
V_{DSAT}	Saturation protection voltage threshold			0.75		V
t_{BLANK}	Blanking time for V_{DSAT} detection		38	60	88	ns
t_{SATFLT}	Time to indicate FLT upon V_{DS} overvoltage detection after blanking time			28.7		ns
ZVD Output (Active Low)						
V_{THRESH_ZVD}	ZVD Detector Threshold		0.8		1.0	V
t_{3RD_ZVD}	Minimum third quadrant time that can be detected by ZVD detector (Low Side)	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time	6	10	14	ns
t_{3RD_ZVD}	Minimum third quadrant time that can be detected by ZVD detector (High Side)	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time	6	10	14	ns
$t_{DLY\_ZVD\_L}$	Delay between V_{THRESH_ZVD} cross vs ZVD output going low	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time		20	30	ns
$t_{DLY\_ZVD\_H}$	Delay between V_{THRESH_ZVD} cross vs ZVD output going low	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time		20	30	ns
t_{WD_ZVD}	ZVD pulse width	For a 0 to -1.5V to 0 pulse with 100ps rise/ fall time	40	65	95	ns
OTD						
OTD+	Over Temperature Detect high threshold		145	165	182	℃
OTD-	Over Temperature Detect high threshold		135	154	170	℃
OTD_{HYS}	Over Temperature Detect high threshold			12		℃
FAULT						
I_{FLT}	Fault pin pull down current	V_{FLT} = 0.4 V	3			mA
t_{FLTDLY}	Time to indicate FLT after fault occurs			20		ns
t_{FLT}	Min fault indication time		10			µs
t_{ENBLK}	Time after FLT release, after which EN=0 is effective		1			µs

(1) Parameters that show only a typical value are determined by design and may not be tested in production
(2) See *Propagation Delay and Mismatch Measurement* section

ADVANCE INFORMATION

6 Parameter Measurement Information

6.1 Propagation Delay and Mismatch Measurement

Figure 6-1 shows the typical test setup used to measure the propagation mismatch. As the gate drives are not accessible, pullup and pulldown resistors in this test circuit are used to indicate when the low-side GaN FET turns ON and the high-side GaN FET turns OFF and vice versa to measure the t_{MON} and t_{MOFF} parameters. Resistance values used in this circuit for the pullup and pulldown resistors are in the order of 1 kΩ; the current sources used are 2 A.

Figure 6-2 through Figure 6-5 show propagation delay measurement waveforms. For turnon propagation delay measurements, the current sources are not used. For turnoff time measurements, the current sources are set to 2 A, and a voltage clamp limit is also set, referred to as $VM_{(CLAMP)}$. When measuring the high-side component turnoff delay, the current source across the high-side FET is turned on, the current source across the low-side FET is off, HI transitions from high-to-low, and output voltage transitions from V_M to $V_{M(CLAMP)}$. Similarly, for low-side component turnoff propagation delay measurements, the high-side component current source is turned off, and the low-side component current source is turned on, LI transitions from high to low and the output transitions from GND potential to $V_{M(CLAMP)}$. The time between the transition of LI and the output change is the propagation delay time.

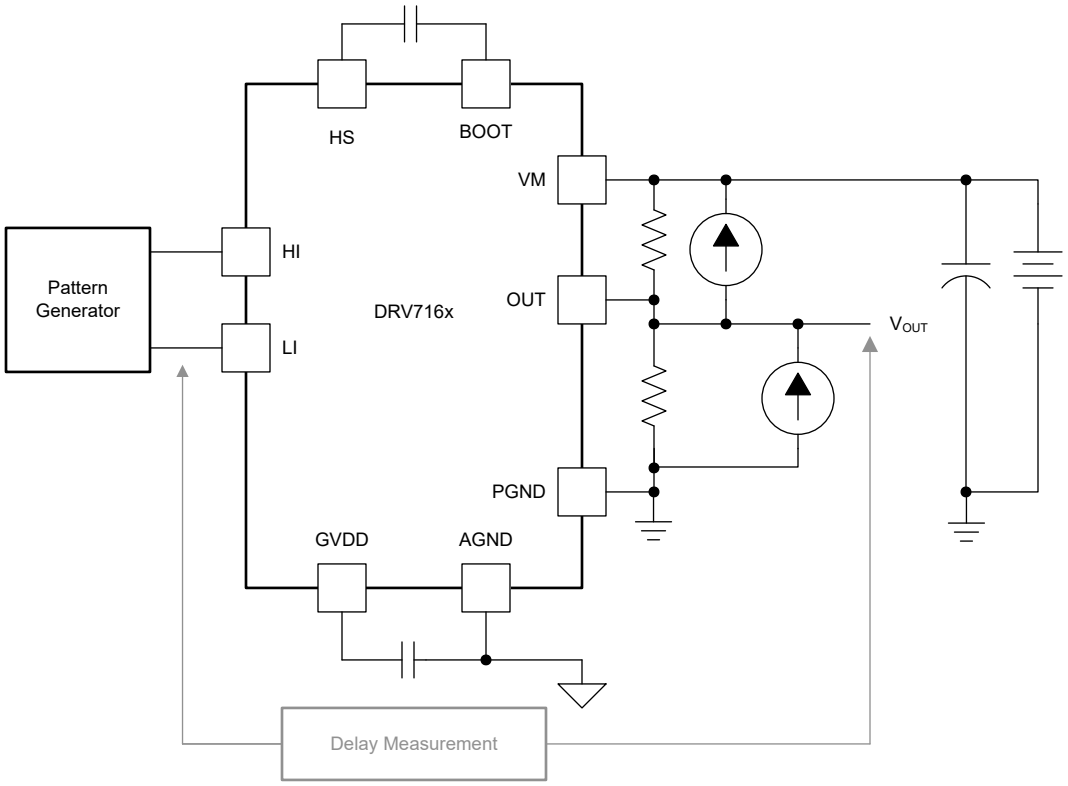

Figure 6-1. Propagation Delay and Propagation Mismatch Measurement

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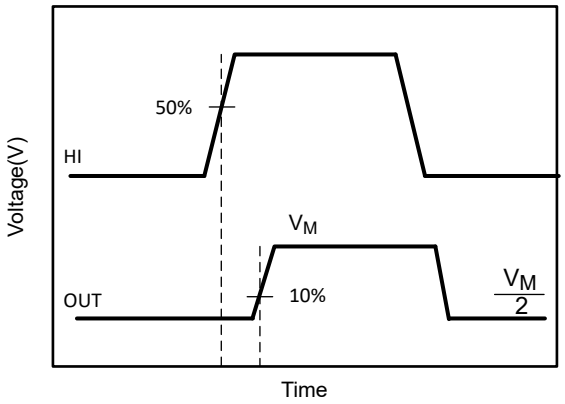

Figure 6-2. High-Side Gate Driver Turnon

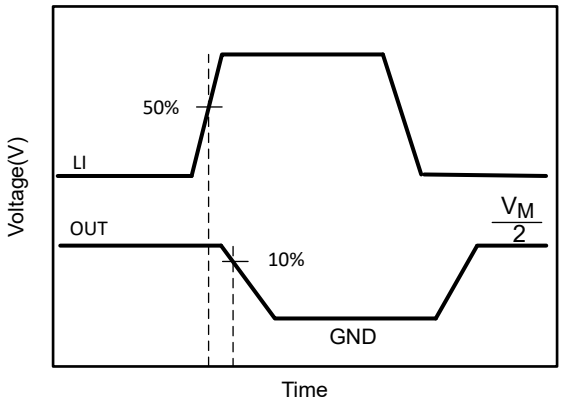

Figure 6-3. Low-Side Gate Driver Turnon

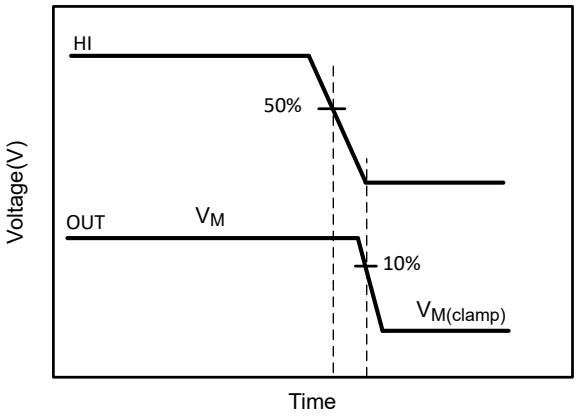

Figure 6-4. High-Side Gate Driver Turnoff

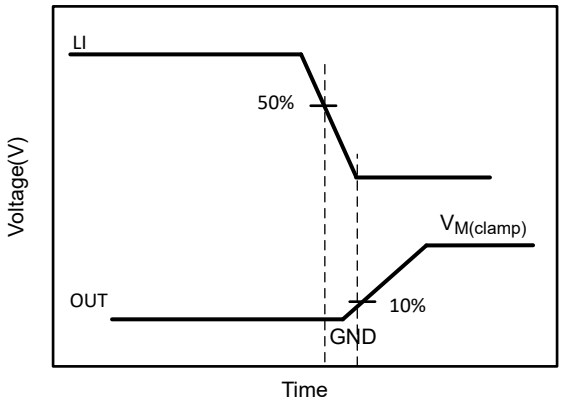

Figure 6-5. Low-Side Gate Driver Turnoff

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

Figure 7-1 shows the DRV7167A, half-bridge, GaN power stage with highly integrated high-side and low-side gate drivers and two GaN FETs in a half-bridge configuration. The device can be used in many isolated and non-isolated topologies allowing very simple integration. The package is designed to minimize the loop inductance while keeping the PCB design simple. The drive strengths for turnon and turnoff are optimized to ensure high voltage slew rates without causing any excessive ringing on the gate or power loop. The device includes several features to improve system performance and protection.

7.2 Functional Block Diagram

Figure 7-1 shows the functional block diagram of the DRV7167A device with integrated high-side and low-side GaN FETs.

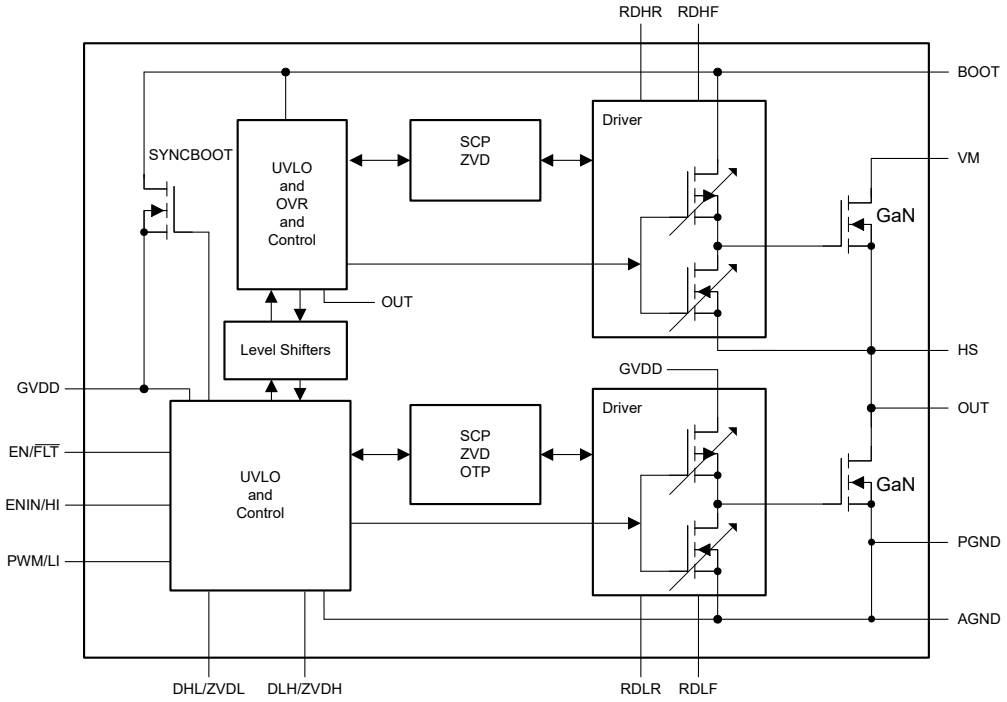

Figure 7-1. Functional Block Diagram

ADVANCE INFORMATION

7.3 Feature Description

The DRV7167A device brings ease of designing high power density boards without the need for underfill while maintaining creepage and clearance requirements. The propagation delays between the high-side gate driver and low-side gate driver are matched to allow very tight control of dead time. Controlling the dead time is critical in GaN-based applications to maintain high efficiency. In DRV7167A HI and LI can be controlled independently. A very small propagation mismatch between the HI and LI to the drivers for both the falling and rising thresholds ensures dead times of < 10 ns. At the same time, the device also features a single PWM mode, with resistor settings for dead-time adjustment, for use with IO-limited controllers. Co-packaging the GaN FET half-bridge with the driver ensures minimized common source inductance. This minimized inductance has a significant performance impact on hard-switched topologies.

The built-in bootstrap circuit with overvoltage regulation prevents the high-side gate drive from exceeding the GaN FETs maximum gate-to-source voltage (Vgs) without any additional external circuitry. The built-in driver has an undervoltage lockout (UVLO) on the GVDD and bootstrap (BOOT-HS) rails. When the voltage is below the UVLO threshold voltage, the device ignores both the HI and LI signals to prevent the GaN FETs from being partially turned on. Below UVLO, if there is sufficient voltage (V_{GVDD} > 2.5 V), the driver actively pulls the high-side and low-side gate driver output low. The UVLO threshold hysteresis prevents chattering and unwanted turnon due to voltage spikes.

V_{DS} monitoring based short-circuit proteciton is implemented on both FETs. Zero-voltage detection (ZVD) reporting enables optimization of the dead-time to minimize third quandrant condution time.

Use an external V_{GVDD} bypass capacitor with a value of 1 µF or higher. TI recommends a size of 0402 to minimize trace length to the pin. Place the bypass and bootstrap capacitors as close as possible to the device to minimize parasitic inductance.

7.3.1 Control Inputs

In Independent Input Mode (IIM), the DRV7167A's inputs pins are independently controlled with TTL input thresholds and can can support 3.3-V and 5-V logic levels regardless of the GVDD voltage.

The DRV7167A implements overlap protection functionality (interlock), to prevent a shoot-through condition if both HI and LI are asserted high. If both HI and LI are asserted, both the high-side and low-side GaN FETs are turned off.

When used in PWM mode, the DRV7167A operates from a single PWM input, with the dead-times between low-to-high and high-to-low transitions set by external resistors on DLH and DHL pins respectively.

7.3.2 Start-up and UVLO

The DRV7167A has an UVLO on both the GVDD and BOOT (bootstrap) supplies. When the GVDD voltage is below the threshold voltage of 3.8 V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also, if there is insufficient GVDD voltage, the UVLO actively pulls the high- and low-side GaN FET gates low. When the BOOT to HS bootstrap voltage is below the UVLO threshold of 3.2 V, only the high-side GaN FET gate is pulled low. Both UVLO threshold voltages have 200 mV of hysteresis to avoid chattering.

Table 7-1. V_{GVDD} UVLO Feature Logic Operation

CONDITION (V_{BOOT}-V_{HS} > V_{BOOTR} for all cases below)	HI	LI	OUT
GVDD - V_{AGND} < V_{GVDDR} during device start-up	H	L	Hi-Z
GVDD - V_{AGND} < V_{GVDDR} during device start-up	L	H	Hi-Z
GVDD - V_{AGND} < V_{GVDDR} during device start-up	H	H	Hi-Z
GVDD - V_{AGND} < V_{GVDDR} during device start-up	L	L	Hi-Z
GVDD - V_{AGND} < V_{GVDDF} after device start-up	H	L	Hi-Z
GVDD - V_{AGND} < V_{GVDDF} after device start-up	L	H	Hi-Z
GVDD - V_{AGND} < V_{GVDDF} after device start-up	H	H	Hi-Z
GVDD - V_{AGND} < V_{GVDDF} after device start-up	L	L	Hi-Z

Table 7-2. $V_{BOOT-HS}$ UVLO Feature Logic Operation

CONDITION (V_{GVDD} > V_{GVDDR} for all cases below)	HI	LI	OUT
V_{BOOT}-V_{HS} < V_{BOOTR} during device start-up	H	L	Hi-Z
V_{BOOT}-V_{HS} < V_{BOOTR} during device start-up	L	H	PGND
V_{BOOT}-V_{HS} < V_{BOOTR} during device start-up	H	H	PGND
V_{BOOT}-V_{HS} < V_{BOOTR} during device start-up	L	L	Hi-Z
V_{BOOT}-V_{HS} < V_{BOOTF} after device start-up	H	L	Hi-Z
V_{BOOT}-V_{HS} < V_{BOOTF} after device start-up	L	H	PGND
V_{BOOT}-V_{HS} < V_{BOOTF} after device start-up	H	H	PGND
V_{BOOT}-V_{HS} < V_{BOOTF} after device start-up	L	L	Hi-Z

7.3.3 Bootstrap Supply Regulation

The high-side bias voltage is generated using a bootstrap technique and is internally regulated at 5 V (typical). This regulation prevents the gate voltage from exceeding the maximum gate-source voltage rating of the enhancement-mode GaN FETs.

7.3.4 Level Shift

The level-shift circuit is the interface from the high-side input HI to the high-side driver stage, which is referenced to the switch node (HS). The level shift allows control of the high-side GaN FET gate driver output, which is referenced to the HS pin and provides excellent delay matching with the low-side driver.

7.3.5 Zero Voltage Detection (ZVD) Reporting

The DRV7167A supports Zero-Voltage Detection (ZVD) to indicate whether the high-side and low-side FETs transitioned to third-qadrant in any transition. This information is reported on ZVDH (for high-side FET) and ZVDL (for low-side FET) pins. This feature is only available in the IIM mode.

For the low-side FET if in a particular transition the switch node falls V_{THRESH_ZVD} below AGND for a time period greater than t_{3RD_ZVD}, a low pulse of t_{WD_ZVD} is generated with a delay of $t_{DLY\_ZVD\_L}$.

For the high-side FET if in a particular transition the switch node rises V_{THRESH_ZVD} above VM for a time period greater than t_{3RD_ZVD}, a low pulse of t_{WD_ZVD} is generated after a one PWM cycle, with a delay of $t_{DLY\_ZVD\_H}$ from the corresponding LI transition.

A controller using DRV7167A can use the ZVD information to adjust dead-times and minimze the third quadrant conduction time of the high-side and low-side FETs.

7.3.6 Short Circuit Protection (SCP)

The DRV7167A implements drain-to-source voltage, V_{DS}, monitoring based short-circuit proteciton on both FETs. After either FET is turned on through HI/LI=high, the device waits for a time t_{BLANK}, following which the V_{DS}voltage of the FET is sensed. If the voltage is greater than V_{DSAT}, a short circuit is inferred. Thereafter the FET is turned off to prevent damage. This protection operates on a cycle-by-cycle basis. That is, every HI/LI logic low-to-high cycle turns on the FET. If the V_{DS} exceeds the set threshold, the short circuit protection turns off the FET for the remainder of the HI/LI logic-high duration.

7.3.7 Over Temperature Detection (OTD)

The DRV7167A monitors the die temperature of the integrated gate-driver and indicates a fault when the OTD+ threshold is exceeded. The device does not take any other action, for example, it does not turn-off the GaN FETs upon detecting over-temperature, leaving any such protection action to the external PWM controller.

Depending on the operating conditions, and system thermal design, there could be a temperature difference between the GaN FETs and the integrated driver, so OTD may be reliably used for protection, but not for system power derating or optimization.

7.3.8 Fault Indication

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The DRV7167A indicates three kind of faults on the EN/FLT pin: short-circuit event on the low-side GaN FET, UVLO event on the GVDD supply, and over-temperature event on the driver. Once asserted, the active low fault signal remains asserted as long any of the three faults exist, and for tFLT after all faults cease to exist.

7.4 Device Functional Modes

The DRV7167A operates in normal mode and UVLO mode. See *Section 7.3.2* for information on UVLO operation mode. In the normal mode, the output state is dependent on the states of the HI and LI pins.

Table 7-3 lists the output states for different input pin combinations for DRV7167A . This device supports overlap protection/interlock functionality. If both HI and LI are asserted, both GaN FETs in the power stage are turned off.

Table 7-3. Truth Table (DRV7167A)

HI	LI	HIGH-SIDE GaN FET	LOW-SIDE GaN FET	OUT
L	L	OFF	OFF	Hi-Z
L	H	OFF	ON	PGND
H	L	ON	OFF	VM
H	H	OFF	OFF	Hi-Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DRV7167A GaN power stage is a versatile building block for Motor Driver applications. The high-performance gate driver IC integrated in the package helps minimize the parasitics and results in extremely fast switching of the GaN FETs. The device design is highly optimized for half-bridge configurations.

8.2 Typical Application

Figure 8-1 shows a BLDC Motor Driver application with GVDD connected to a 5-V supply. It is critical to optimize the power loop (loop impedance from VM capacitor to PGND). Having a high power loop inductance causes significant ringing in the OUT node and also causes the associated power loss. The DRV7167A has VM and PGND pins next to each other. This enables the VM capacitor to be placed very close to DRV7167A on the top layer of the PCB, minimizing power loop inductance.

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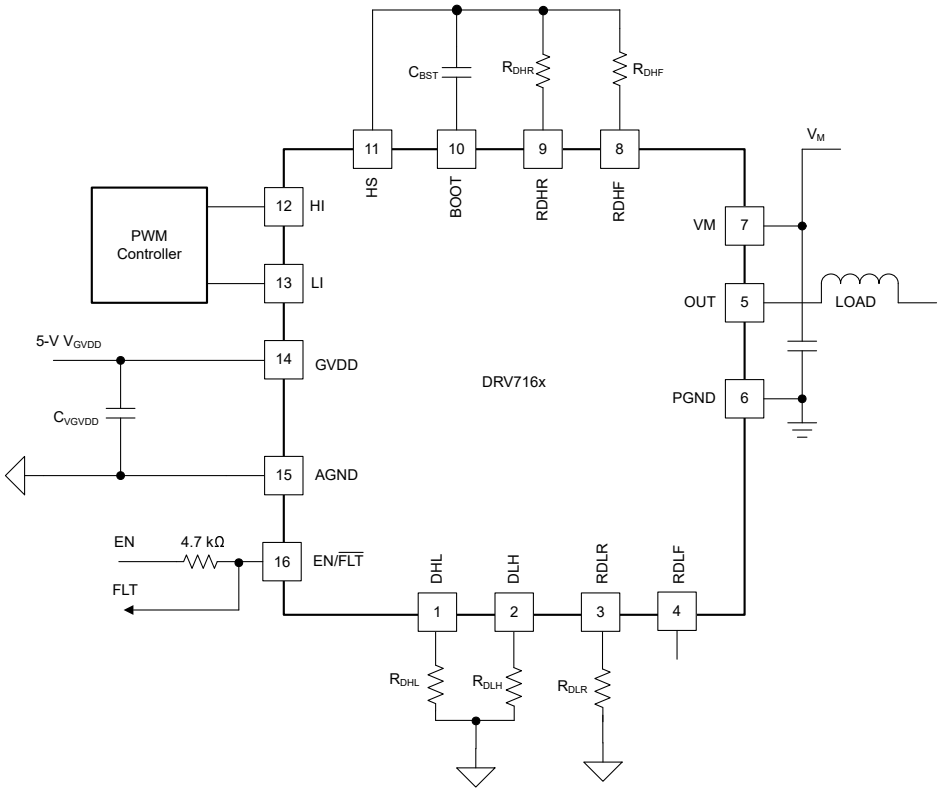

Figure 8-1. Typical Connection Diagram For a BLDC Motor Driver

8.2.1 Typical Application - PWM Mode

Figure 8-2 shows a BLDC Motor Driver application with PWM mode, where the controller only provides one PWM control signal, and the high-side and low-side signals, with adjustable deadtime, are generated internal to the DRV7167A. Resistors R_{DHL} and R_{DLH} can be used to set the high-to-low and low-to-high deadtimes. Floating pin RDLF sets the DRV7167A to PWM mode. Consequently turn-off drive strength for the low-side FET is not adjustable in PWM mode.

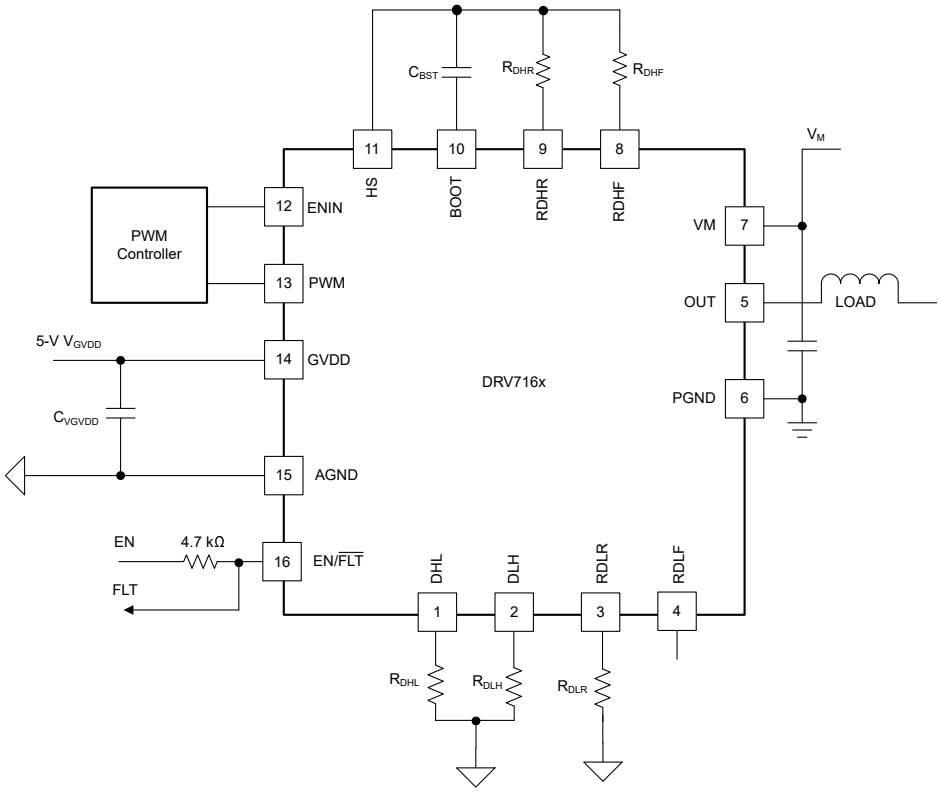

Figure 8-2. Typical Connection Diagram For a BLDC Motor Driver with PWM Mode

8.3 Power Supply Recommendations

The recommended bias supply voltage range for DRV7167A is from 4.5 V to 5.5 V. Note that the gate voltage of the low-side GaN FET is not clamped internally. Hence, it is important to keep the GVDD bias supply within the recommended operating range to prevent exceeding the low-side GaN transistor gate breakdown voltage.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the GVDD voltage drops, the device continues to operate in normal mode as far as the voltage drop does not exceeds the hysteresis specification, $V_{GVDD(hyst)}$. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 4.5 V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of DRV7167A to avoid triggering device-shutdown.

Place a local bypass capacitor between the GVDD and AGND pins. This capacitor must be located as close as possible to the device. A low ESR, ceramic surface-mount capacitor is recommended. TI recommends using 2 capacitors across GVDD and AGND: a 100 nF ceramic surface-mount capacitor for high frequency filtering placed very close to GVDD and AGND pin, and another surface-mount capacitor, 1 µF to 10 µF, for IC bias requirements.

8.4 Layout

8.4.1 Layout Guidelines

To maximize the efficiency benefits of fast switching, it is extremely important to optimize the board layout such that the power loop impedance is minimal. When using a multilayer board (more than 2 layers), power loop parasitic impedance is minimized by having the return path to the input capacitor (between VM and PGND), small and directly underneath the first layer as shown in Figure 8-3 and Figure 8-4. Loop inductance is reduced due to flux cancellation as the return current is directly underneath and flowing in the opposite direction.

Insufficient attention to the above power loop layout guidelines can result in excessive overshoot and undershoot on the switch node.

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It is also critical that the GVDD capacitors and the bootstrap capacitors are as close as possible to the device and in the first layer. Carefully consider the AGND connection of DRV7167A device. It must NOT be directly connected to PGND so that PGND noise does not directly shift AGND and cause spurious switching events due to noise injected in HI and LI signals.

Refer DRV7167A EVM for an actual layout based on these recommendations.

8.4.2 Layout Examples

Placements shown in Figure 8-3 and in the cross section of Figure 8-4 show the suggested placement of the device with respect to sensitive passive components, such as VM, bootstrap capacitors (HS and BOOT) and GVDD capacitors. Use appropriate spacing in the layout to reduce creepage and maintain clearance requirements in accordance with the application pollution level. Inner layers if present can be more closely spaced due to negligible pollution.

The layout must be designed to minimize the capacitance at the OUT node. Use as small an area of copper as possible to connect the device OUT pin to the inductor, or transformer, or other output load. Furthermore, ensure that the ground plane or any other copper plane has a cutout so that there is no overlap with the OUT node, as this would effectively form a capacitor on the printed circuit board. Additional capacitance on this node reduces the advantages of the advanced packaging approach of the DRV7167A and may result in reduced performance.

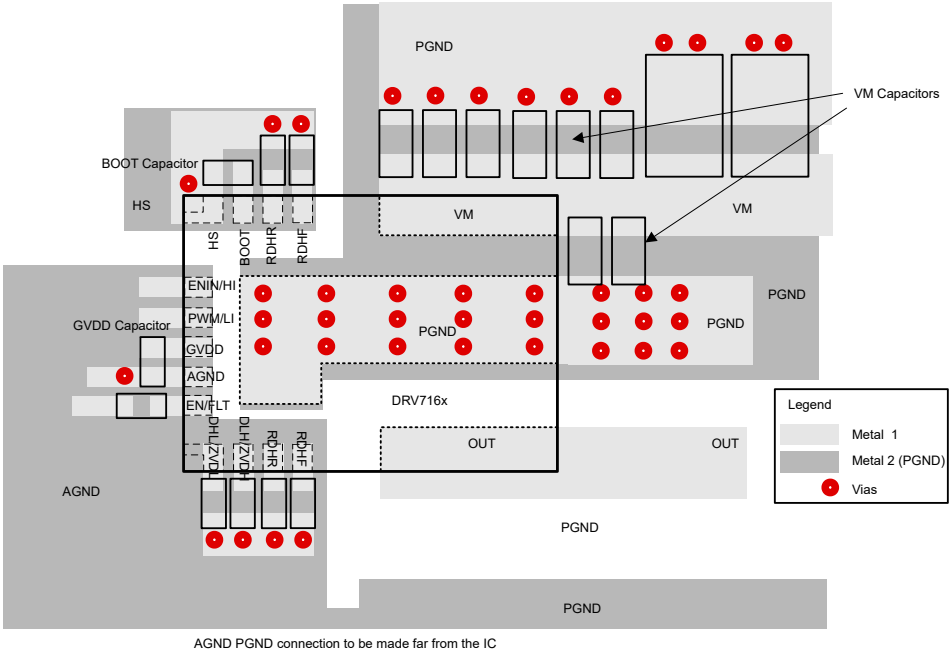

Figure 8-3. External Component Placement (Multi-layer PCB)

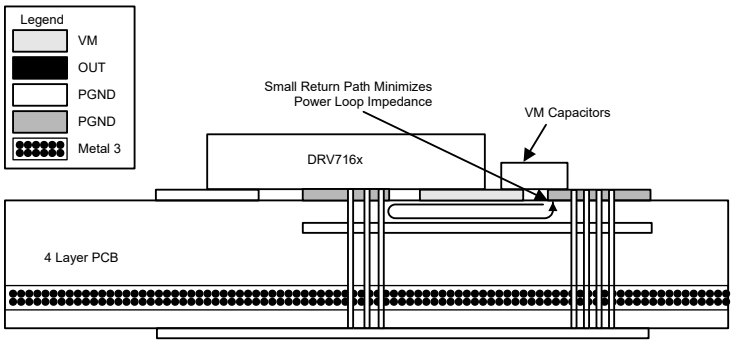

Figure 8-4. Four-Layer Board Cross Section With Return Path Directly Underneath for Power Loop

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

Layout Guidelines for LMG2100R044 GaN Power Stage Module

Using the LMG2100R044: GaN Half-Bridge Power Module Evaluation Module

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2025	*	Initial Release

ADVANCE INFORMATION

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

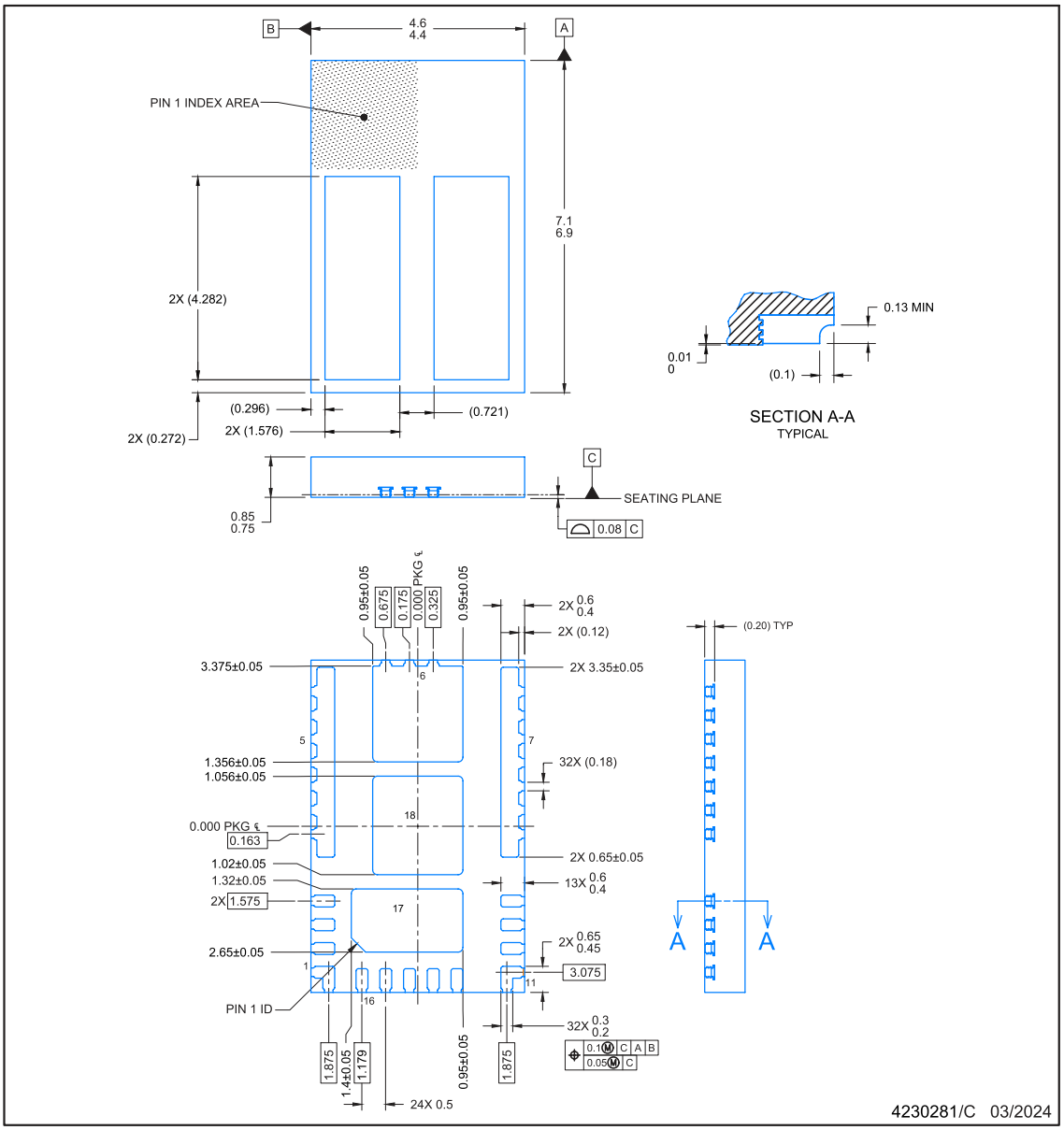
11.1 Package Information

11.1.1 Mechanical Data

PACKAGE OUTLINE

VBN0018A — **VQFN-FCRLF - 0.85 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

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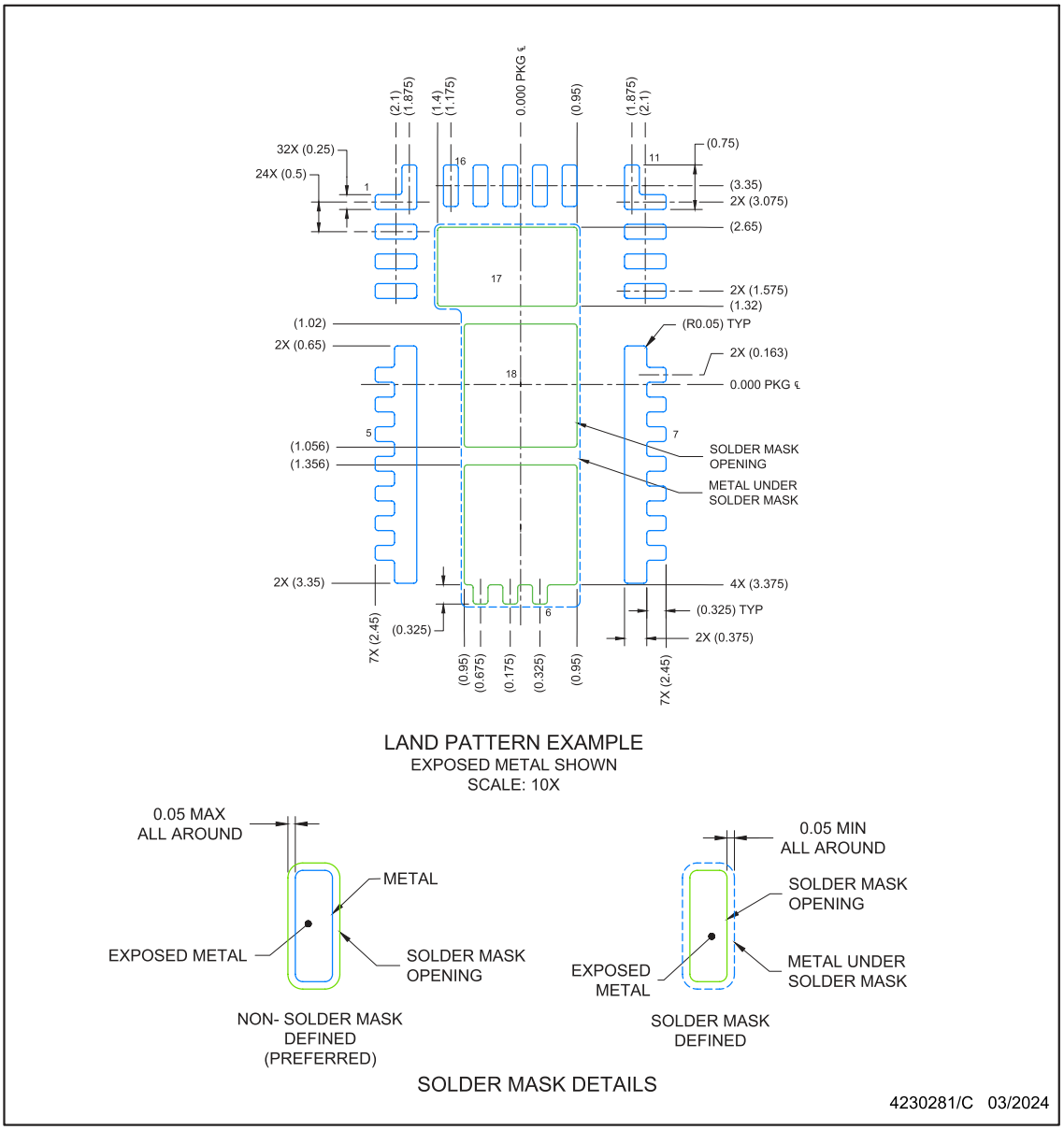
EXAMPLE BOARD LAYOUT

VBN0018A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES: (continued)

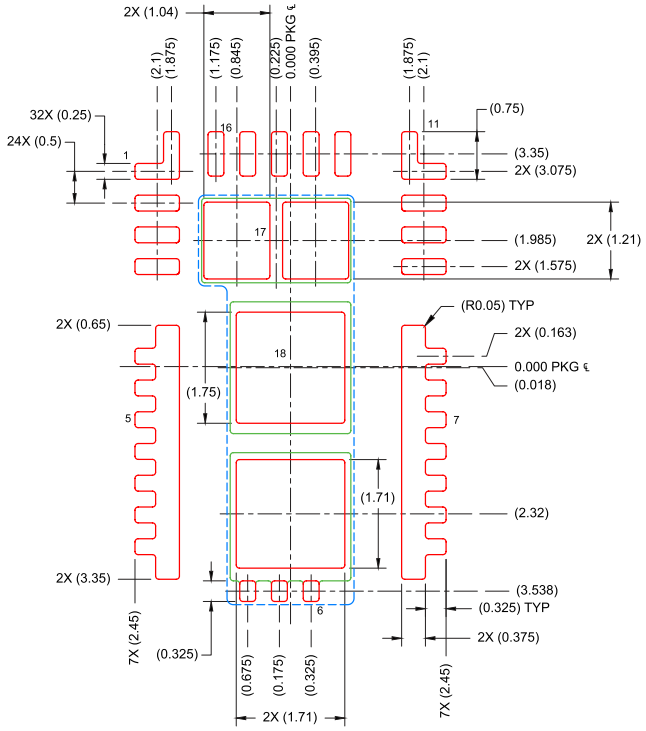
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VBN0018A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PAD 6: 78%
PAD 17: 81%
PAD 18: 76%

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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GENERIC PACKAGE VIEW

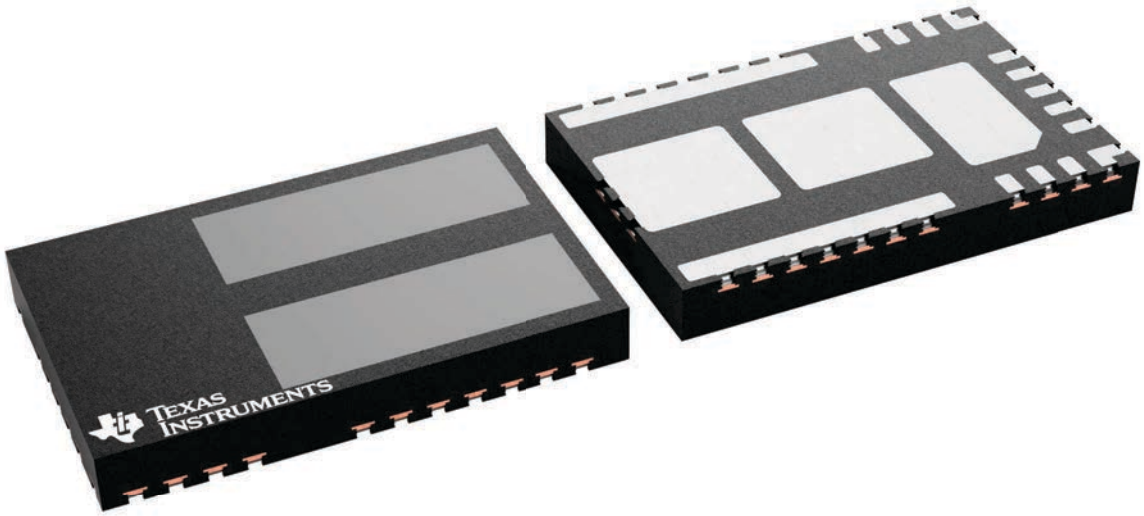
VBN 18

VQFN-FCRLF - 0.85 mm max height

4.5 x 7, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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