TRF1305A2 15dB-Gain, Dual-Channel, DC to > 5.8GHz BW, RF Fully Differential Amp

1 Features

- Three performance-optimized power gain variants:
  - 15dB (TRF1305A2)
  - 10dB (TRF1305B2)
  - 5dB (TRF1305C2)
- Fixed gain can be reduced with external resistors
- Wide large-signal RF bandwidth:
  - D2D: 5.8GHz (3dB), 5.2GHz (1dB)
  - S2D: 6.1GHz (3dB), 5.2GHz (1dB)
- OP1dB (differential 100Ω load):
  - D2D: 15dBm (2GHz), 11.6dBm (4GHz)
  - S2D: 15.2dBm (2GHz), 11.8dBm (4GHz)
- OIP3 (P_O = 1dBm/tone):
  - D2D: 32.5dBm (2GHz), 21dBm (4GHz)
  - S2D: 33dBm (2GHz), 22dBm (4GHz)
- Noise Figure:
  - D2D: 9.2dB (2GHz), 11.7dB (4GHz)
  - S2D: 9.6dB (2GHz), 11.4dB (4GHz)
- Slew rate: 25kV/µs
- Large input (±1V) and output (±0.5V) common-mode voltage ranges
- Flexible configurations and modes:
  - Single-ended input, differential output (S2D)
  - Differential input, differential output (D2D)
  - AC- or DC-coupled input/output
  - Adjustable output common-mode voltage
  - Input common-mode range extension mode
- Supports 5V, single or split supplies
- Active power dissipation: 503mW per channel
- Power-down for each channel

2 Applications

- RF sampling or GSPS ADC driver
- Test and measurement
- Wireless communications test
- RF digitizers
- Oscilloscopes (DSOs)
- High speed digitizer
- Spectrum analyzer
- Vector signal transceiver (VST)
- Mass spectrometry systems
- Common-mode level shifting
- IQ mixer interface

3 Description

The TRF1305A2 is a very high performance, closed-loop, dual-channel RF amplifier that has an operational bandwidth from true-dc to > 5.8GHz. The device has excellent performance to drive high-speed, high-performance ADCs, such as the ADC12DJ5200RF and ADC32RF5x with a dc- or ac-coupled interface. The amplifier is optimized for use in RF, zero and complex IF, and high-speed time-domain applications. The device is optimized for performance in the fixed gain configuration. If lower gain is desired, use external resistors.

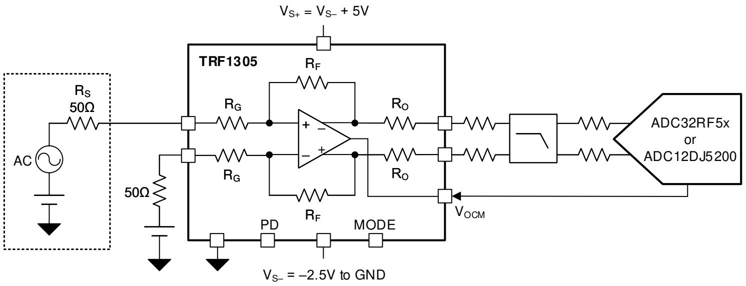
The TRF1305A2 features a VOCM pin that allows setting different output common-mode and input common-mode voltages; for example, level-shifting or for most IQ down-converter ADC-interface applications that have differing dc common-mode voltages. The TRF1305A2 also features a floating two-rail split or single-supply option, and a MODE pin that allows extending the input common-mode range closer to the supplies. The device also has a power-down feature to turn-off each channel individually.

The device uses TI's proprietary advanced BiCMOS process and is available in a space-saving, 2.5mm × 3mm, 16-pin, WQFN-FCRLF package.

Device Information

PART NUMBER[1]	POWER GAIN	PACKAGE[2]
TRF1305A2	15dB	RYP (WQFN-FCRLF, 16)
TRF1305B2	10dB	
TRF1305C2	5dB	

(1) See Section 4.
(2) For more information, see Section 11.



TRF1305A2 in S2D Configuration Driving a High-Speed ADC

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4 Device Comparison Table

DEVICE	GAIN	CHANNEL COUNT
TRF1305A1	15dB	1
TRF1305B1	10dB	
TRF1305C1	5dB	
TRF1305A2	15dB	2
TRF1305B2	10dB	
TRF1305C2	5dB	

5 Pin Configuration and Functions

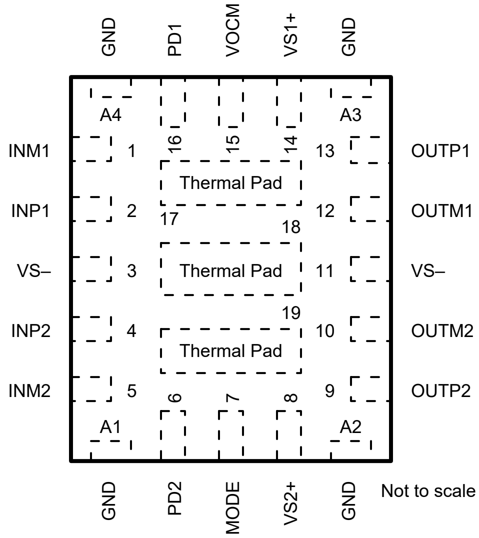

Figure 5-1. RYP Package (Dual-Channel), 16-Pin WQFN-FCRLF (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	A1, A2, A3, A4	—	Ground. Connect to ground plane on the board. Internally shorted to the thermal pad.
INM1	1	Input	Negative side of differential input signal for channel 1 (Ch1).
INM2	5	Input	Negative side of differential input signal for channel 2 (Ch2).
INP1	2	Input	Positive side of differential input signal for channel 1 (Ch1).
INP2	4	Input	Positive side of differential input signal for channel 2 (Ch2).
MODE	7	Input	Mode selection pin. For details, see the Mode Pin section.
OUTM1	12	Output	Negative side of differential output signals for Ch1.
OUTM2	10	Output	Negative side of differential output signals for Ch2.
OUTP1	13	Output	Positive side of differential output signals for Ch1.
OUTP2	9	Output	Positive side of differential output signals for Ch2.
PD1	16	Input	Power-down signal for Ch1, referenced to GND. Supports both 1.8V and 3.3V logic. Logic 0 or open = channel enabled. Logic 1 = channel powered down.
PD2	6	Input	Power-down signal for Ch2, referenced to GND. Supports both 1.8V and 3.3V Logic. Logic 0 or open = channel enabled. Logic 1 = channel powered down.
VOCM	15	Input	Output common-mode voltage input pin. Common for both channels. Float the pin to set the output common-mode voltage to V_{S-} + 2.5V.
VS–	3, 11	Power	Negative supply pin. Common for both channels.
VS1+	14	Power	Positive supply pin for Ch1. Maintain that $V_{S1+} = V_{S2+}$.
VS2+	8	Power	Positive supply pin for Ch2. Maintain that $V_{S1+} = V_{S2+}$.
Thermal Pad	17, 18, 19	—	Thermal pad. Connect to heat-dissipating ground plane on the board. Internally shorted to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{S-}	Negative supply voltage, referenced to GND		–3	0.3	V
V_{S+}	Positive supply voltage, ensure that $V_{S1+} = V_{S2+}$		–0.3	$V_{S-} + 5.5$	V
V_S	Total supply voltage, $V_S = V_{S+} – V_{S-}$		–0.3	5.5	V
P_{IN}	Input RF power(2)			20	dBm
V_{PD}	PD pin voltage, referenced to GND	$V_{S+} \geq 3.3V$	–0.3	3.6	V
		$V_{S+} < 3.3V$	–0.3	$V_{S+} + 0.3$	
V_{OCM}	VOCM pin voltage		$V_{S-} + 1$	$V_{S-} + 4$	V
V_{MODE}	MODE pin voltage		$V_{S-} – 0.3$	$V_{S-} + 3.3$	V
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) When device supplies are present; otherwise, limit swing at the device pins to $V_{S-} \pm 0.3V$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S-}	Negative supply voltage	–2.5		0	V
V_S	Total supply voltage, $V_S = V_{S+} – V_{S-}$	4.75	5	5.25	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TRF1305A2	UNIT
		RYP (WQFN-FCRLF)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.7	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics - AC Specifications in D2D Configuration

at T_A = 25°C, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output with differential source impedance (Z_S) = 100Ω, differential output load (Z_L) = 100Ω, external input resistor network (see Figure 8-6), and inputs de-embedded up to R_{IN_SH} and outputs up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth (3dB)	P_{IN} = –20dBm at each input			5.8		GHz
	Small-signal bandwidth (1dB)	P_{IN} = –20dBm at each input			5.2		
LSBW	Large-signal bandwidth (3dB)	Differential P_{IN} = –8dBm			5.8		GHz
	Large-signal bandwidth (1dB)	Differential P_{IN} = –8dBm			5.2		
Sdd21	Power gain	f = 500MHz			14.4		dB
		f = 4GHz			15.9		
	Gain variation over temperature	f = 4GHz, T_A = –40°C to +85°C			1.3		dB
Sdd11	Input return loss	f = 10MHz to 5GHz			–11		dB
Sdd12	Reverse isolation	f < 5GHz (device enabled)			–25		dB
	Gain mismatch between channels	f = 10MHz to 5GHz			±0.1		dB
	Phase mismatch between channels	f = 10MHz to 5GHz			±0.5		°
	Crosstalk between channels	f = 1GHz			–62		dBc
OP1dB	Output 1dB compression point	f = 500MHz			15.5		dBm
		f = 1GHz			15.4		
		f = 2GHz			15		
		f = 3GHz			13.7		
		f = 4GHz			11.6		
		f = 5GHz			9.1		
HD2	Second-order harmonic distortion	V_O = 2V_{PP} (P_O = 7dBm)	f = 500MHz		–82		dBc
			f = 1GHz		–69		
			f = 2GHz		–66		
			f = 3GHz		–60		
			f = 4GHz		–58		
HD3	Third-order harmonic distortion	V_O = 2V_{PP} (P_O = 7dBm)	f = 500MHz		–67		dBc
			f = 1GHz		–56		
			f = 2GHz		–53		
			f = 3GHz		–62		
			f = 4GHz		–51		
OIP2	Output second-order intercept point	P_O = 1dBm per tone, 2MHz spacing	f = 500MHz		80		dBm
			f = 1GHz		71		
			f = 2GHz		62		
			f = 3GHz		57		
			f = 4GHz		55		
			f = 5GHz		51		
OIP3	Output third-order intercept point	P_O = 1dBm per tone, 2MHz spacing	f = 500MHz		45		dBm
			f = 1GHz		39.5		
			f = 2GHz		32.5		
			f = 3GHz		26		
			f = 4GHz		21		
			f = 5GHz		18		

6.5 Electrical Characteristics - AC Specifications in D2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output with differential source impedance (Z_S) = 100Ω, differential output load (Z_L) = 100Ω, external input resistor network (see Figure 8-6), and inputs de-embedded up to R_{IN_SH} and outputs up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise figure	f = 500MHz		7.3		dB
		f = 1GHz		7.8		
		f = 2GHz		9.2		
		f = 3GHz		10.8		
		f = 4GHz		11.7		
		f = 5GHz		12.1		
NSD	Output noise spectral density	f = 500MHz		–152		dBm/Hz
		f = 1GHz		–151.5		
		f = 2GHz		–149.8		
		f = 3GHz		–147.2		
		f = 4GHz		–146.2		
		f = 5GHz		–147.9		

6.6 Electrical Characteristics - AC Specifications in S2D Configuration

at T_A = 25°C, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), and input and outputs de-embedded up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth (3dB)	P_{IN} = –20dBm at each input			6.1		GHz
	Small-signal bandwidth (1dB)	P_{IN} = –20dBm at each input			5.2		
LSBW	Large-signal bandwidth (3dB)	Single-ended P_{IN} = –8dBm			6.1		GHz
	Large-signal bandwidth (1dB)	Single-ended P_{IN} = –8dBm			5.2		
Sds21	Power gain	f = 500MHz			14.8		dB
		f = 4GHz			15		
	Gain variation over temperature	f = 4GHz, T_A = –40°C to +85°C			1.5		dB
Sss11	Input return loss	f = 10MHz to 3GHz(1)			–11		dB
Sss11	Input return loss	f = 4GHz(1)			–10		
Sss11	Input return loss	f = 5GHz(1)			–8		
Ssd12	Reverse isolation	f < 5GHz (device enabled)			–25		dB
	Gain mismatch between channels	f = 10MHz to 5GHz			±0.1		dB
	Phase mismatch between channels	f = 10MHz to 5GHz			±1		°
	Crosstalk between channels	f = 1GHz			–48		dBc
G_{IMB}	Differential output gain imbalance	f < 5GHz, P_{IN} = –20dBm with 50Ω Z_S			±0.1		dB
PH_{IMB}	Differential output phase imbalance	f < 5GHz, P_{IN} = –20dBm with 50Ω Z_S			±1.2		°
OP1dB	Output 1dB compression point	f = 500MHz			15.4		dBm
		f = 1GHz			15.7		
		f = 2GHz			15.2		
		f = 3GHz			13.8		
		f = 4GHz			11.8		
		f = 5GHz			10		
HD2	Second-order harmonic distortion	V_O = $2V_{PP}$ (P_O = 7dBm)	f = 500MHz		–60		dBc
			f = 1GHz		–58		
			f = 2GHz		–48		
			f = 3GHz		–50		
			f = 4GHz		–46		
HD3	Third-order harmonic distortion	V_O = $2V_{PP}$ (P_O = 7dBm)	f = 500MHz		–69		dBc
			f = 1GHz		–59		
			f = 2GHz		–54		
			f = 3GHz		–58		
			f = 4GHz		–48		
OIP2	Output second-order intercept point	P_O = 1dBm per tone, 2MHz spacing	f = 500MHz		70		dBm
			f = 1GHz		61		
			f = 2GHz		50		
			f = 3GHz		51		
			f = 4GHz		51		
			f = 5GHz		51		

6.6 Electrical Characteristics - AC Specifications in S2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), and input and outputs de-embedded up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OIP3	Output third-order intercept point	P_O = 1dBm per tone, 2MHz spacing	f = 500MHz		44		dBm
			f = 1GHz		39		
			f = 2GHz		33		
			f = 3GHz		28		
			f = 4GHz		22		
			f = 5GHz		19		
NF	Noise figure	f = 500MHz			7.8		dB
		f = 1GHz			8		
		f = 2GHz			9.6		
		f = 3GHz			10.5		
		f = 4GHz			11.4		
		f = 5GHz			12		
NSD	Output noise spectral density	f = 500MHz			–151.3		dBm/Hz
		f = 1GHz			–151.2		
		f = 2GHz			–149.6		
		f = 3GHz			–148.5		
		f = 4GHz			–147		
		f = 5GHz			–147.6		

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(1) See Section 8.1.1.1, for method to improve input return loss.

6.7 Electrical Characteristics - DC and Timing Specifications

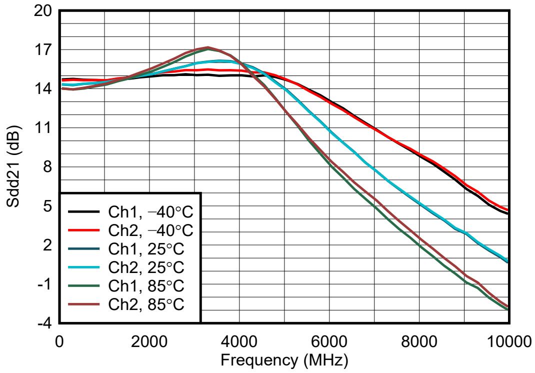
at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, Z_L = 100Ω, and specifications apply to both S2D and D2D configuration (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC PERFORMANCE						
$V_{OD\text{-}MAX}$	Max differential output voltage	f = 1GHz		4		V_{PP}
	Slew rate	2V V_O step, dc coupled, V_{S+} = 2.5V, V_{S-} = –2.5V		25		kV/µs
	Output differential offset voltage			±3		mV
	Overdrive recovery time	dc coupled, V_{S+} = 2.5V, V_{S-} = –2.5V, from 2 × overdrive of each SE output to each output voltage settling to < ±50mV		6		ns
COMMON-MODE						
V_{ICM}	Input common-mode voltage	Default range(1)	V_{S-} + 1.5		V_{S-} + 3.5	V
V_{OCM}	Output common-mode voltage		V_{S-} + 2		V_{S-} + 3	V
	Output common-mode offset voltage from V_{OCM} voltage		–20		20	mV
IMPEDANCE						
$Z_{IN\text{-}SE}$	Single-ended input impedance	S2D, at INP pin with 50Ω termination on INM pin		45.8		Ω
$Z_{IN\text{-}DIFF}$	Differential input impedance	D2D, at the device pins		13.5		Ω
		D2D, at R_{IN_SH}, see Figure 8-6		59.7		
$Z_{O\text{-}DIFF}$	Differential output impedance	f = near dc		8		Ω
POWER SUPPLY						
I_{QA}	Active quiescent current	Both channels active		201		mA
		One channel active, other is powered down		112		
I_{QPD}	Power-down quiescent current	Both channels powered down		23		mA
POWER DOWN						
V_{PD_Hi}	PD pin logic high	Referenced to GND, see Section 6.1	1.35			V
V_{PD_Lo}	PD pin logic low	Referenced to GND, see Section 6.1			0.3	V
I_{PD_Bias}	PD bias current (current on PD pin)	PD = high (1.8V logic)		10.5	15	µA
		PD = high (3.3V logic)		19	30	
t_{ON}	Turn-on time	S2D, dc coupled, V_{S+} = 2.5V, V_{S-} = –2.5V, from 50% V_{PD} transition to 90% RF out		25		ns
t_{OFF}	Turn-off time	S2D, dc coupled, V_{S+} = 2.5V, V_{S-} = –2.5V, from 50% V_{PD} transition to 10% RF out		20		ns

(1) V_{ICM} range can be extended closer to V_{S+} or V_{S-} in D2D configuration. See also Section 7.4.1.

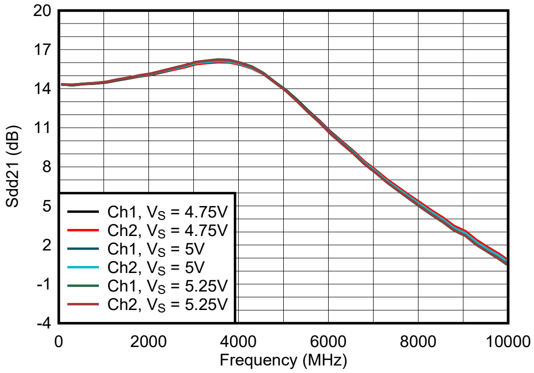
6.8 Typical Characteristics: D2D Configuration

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



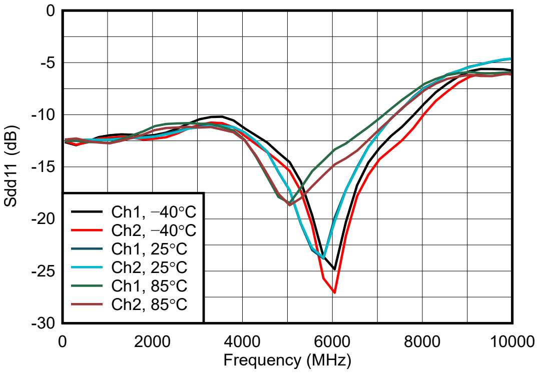
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-1. Power Gain (Sdd21) Across Temperature



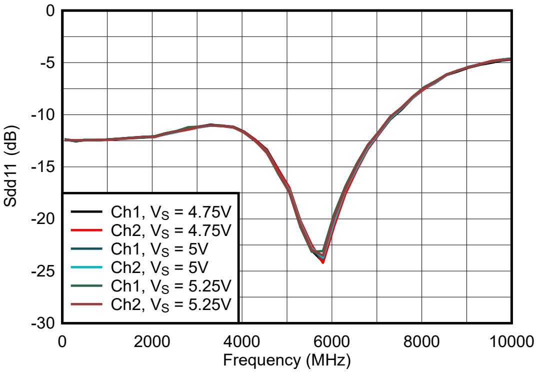
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-2. Power Gain (Sdd21) Across Supply Voltage



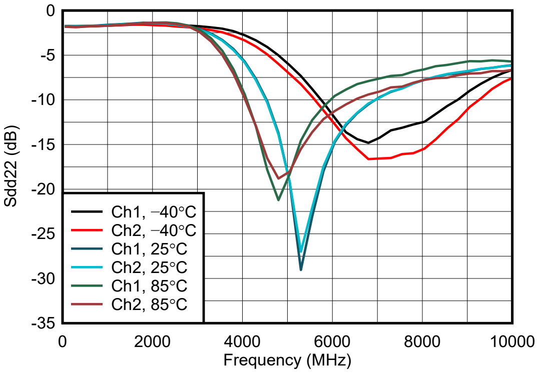
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-3. Input Return Loss (Sdd11) Across Temperature



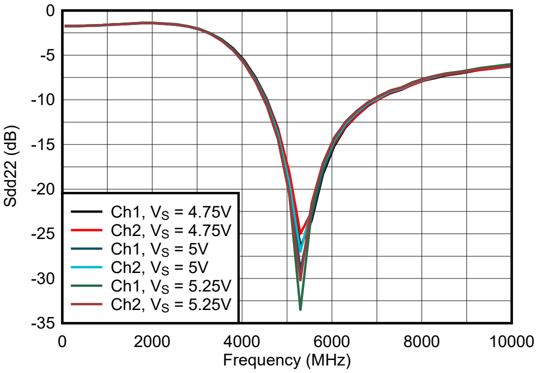
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-4. Input Return Loss (Sdd11) Across Supply Voltage



P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-5. Output Return Loss (Sdd22) Across Temperature

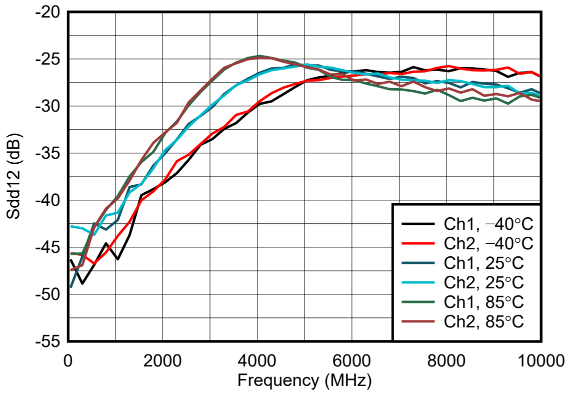


P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-6. Output Return Loss (Sdd22) Across Supply Voltage

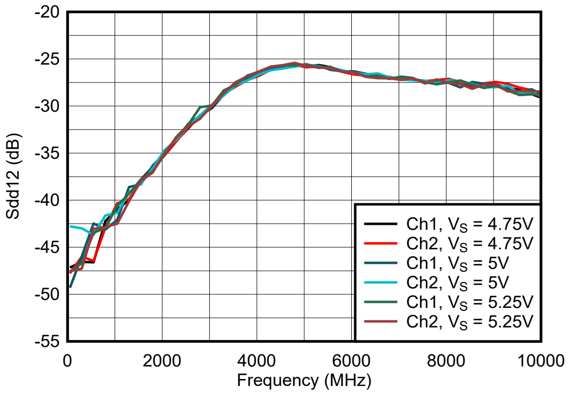
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



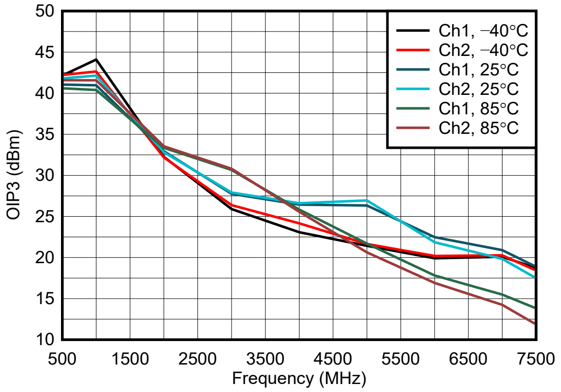
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-7. Reverse Isolation (Sdd12) Across Temperature



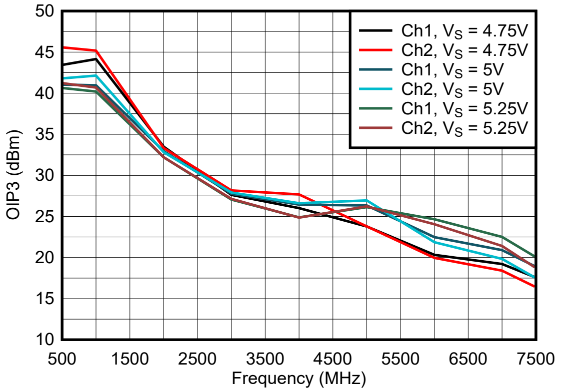
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-8. Reverse Isolation (Sdd12) Across Supply Voltage



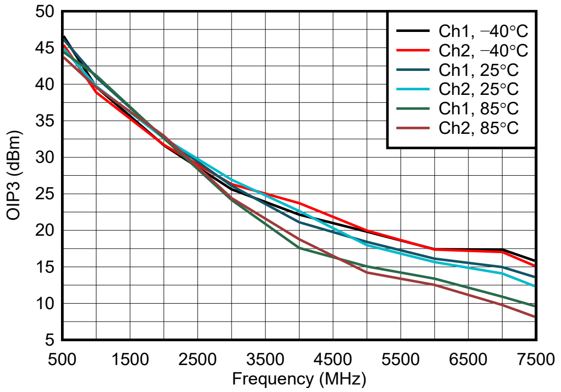
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-9. OIP3 Across Temperature



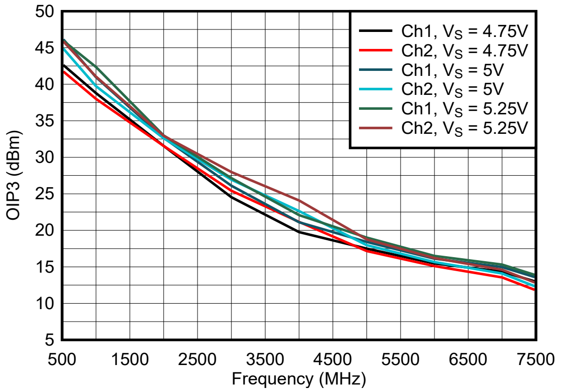
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-10. OIP3 Across Supply Voltage



P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-11. OIP3 Across Temperature

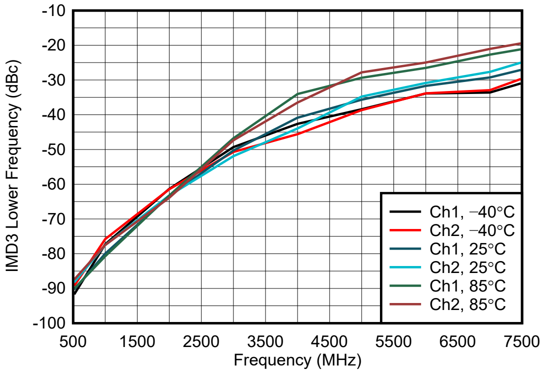


P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-12. OIP3 Across Supply Voltage

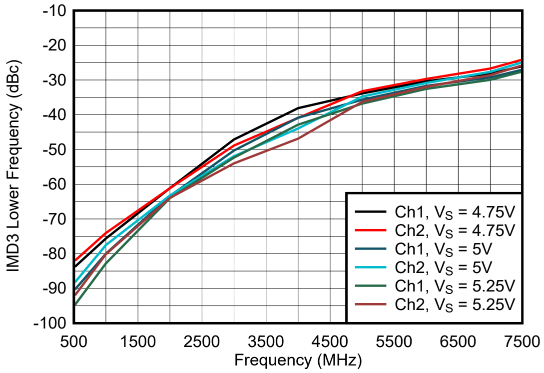
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



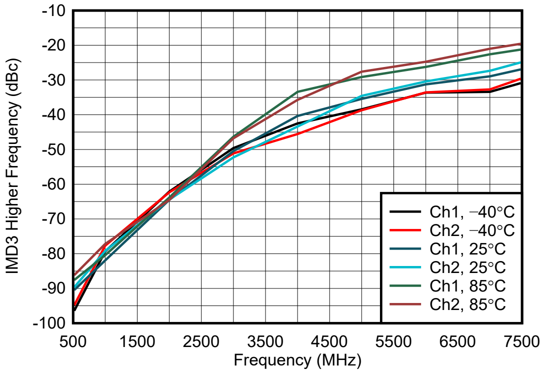
At $(2f_1 – f_2)$ frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-13. IMD3 Lower Across Temperature



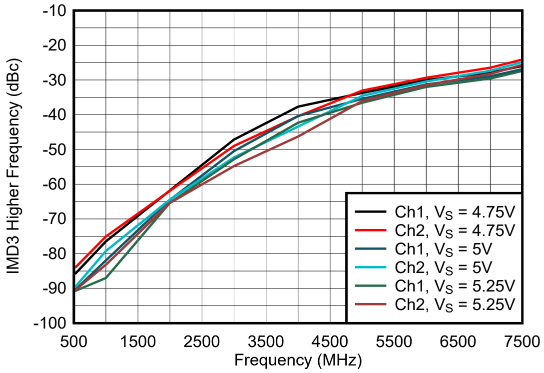
At $(2f_1 – f_2)$ frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-14. IMD3 Lower Across Supply Voltage



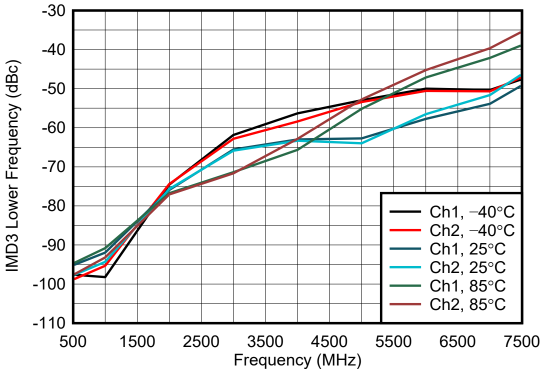
At $(2f_2 – f_1)$ frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-15. IMD3 Higher Across Temperature



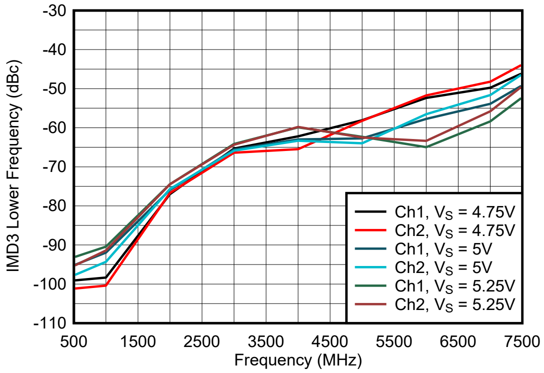
At $(2f_2 – f_1)$ frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-16. IMD3 Higher Across Supply Voltage



At $(2f_1 – f_2)$ frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-17. IMD3 Lower Across Temperature

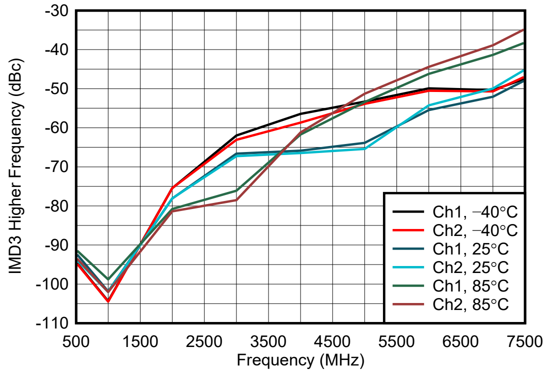


At $(2f_1 – f_2)$ frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-18. IMD3 Lower Across Supply Voltage

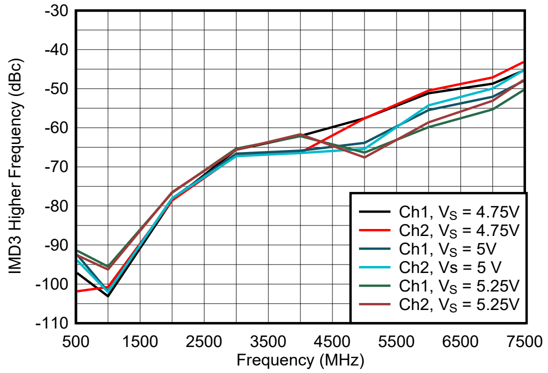
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



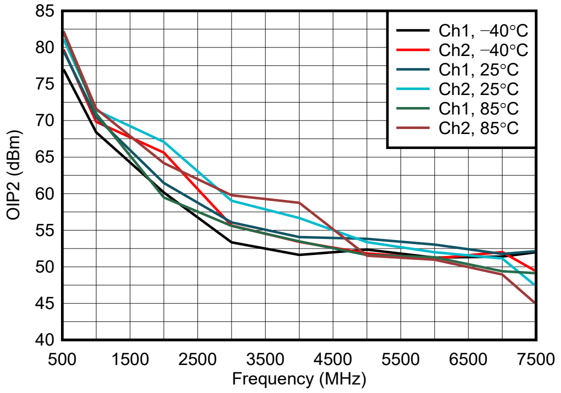
At ($2f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-19. IMD3 Higher Across Temperature



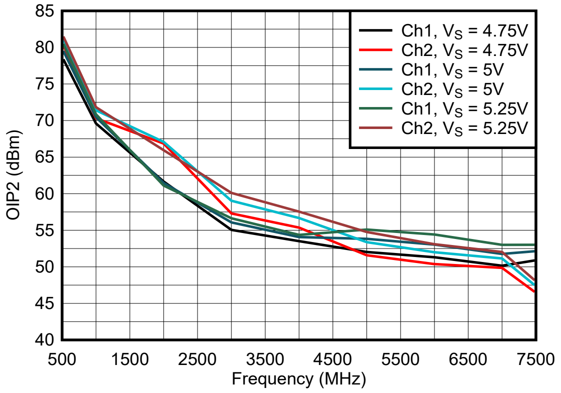
At ($2f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-20. IMD3 Higher Across Supply Voltage



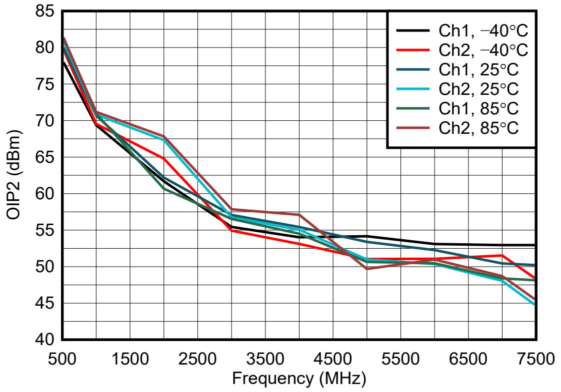
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-21. OIP2 Across Temperature



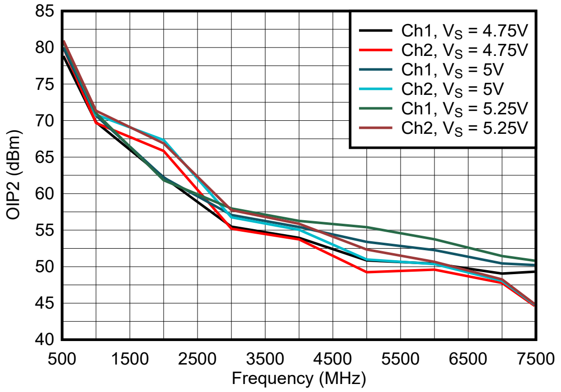
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-22. OIP2 Across Supply Voltage



P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-23. OIP2 Across Temperature

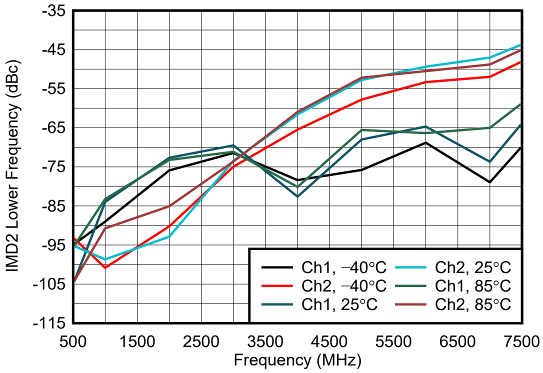


P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-24. OIP2 Across Supply Voltage

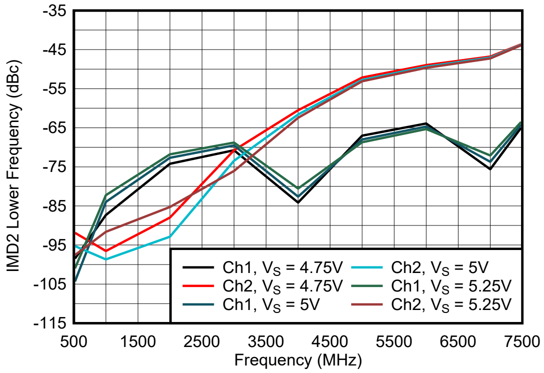
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



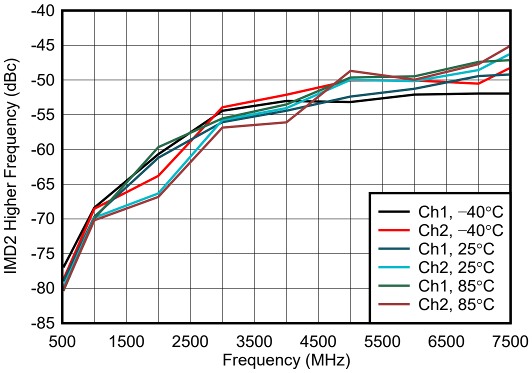
At ($f_2 - f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-25. IMD2 Lower Across Temperature



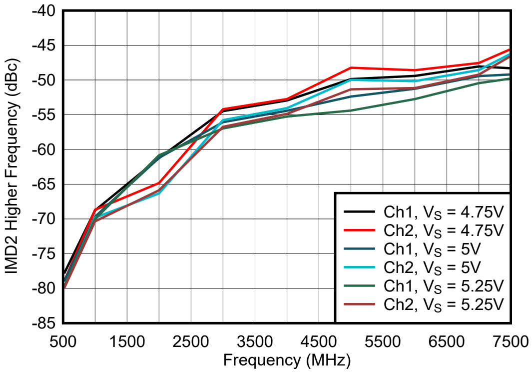
At ($f_2 - f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-26. IMD2 Lower Across Supply Voltage



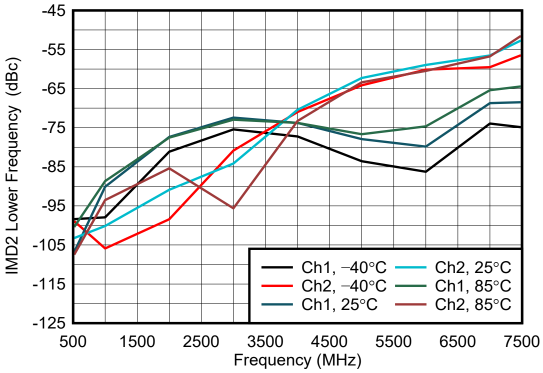
At ($f_1 + f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-27. IMD2 Higher Across Temperature



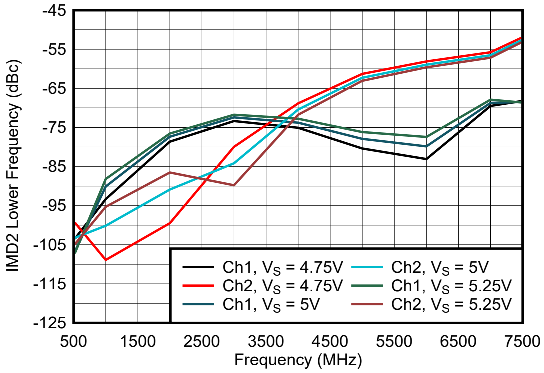
At ($f_1 + f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-28. IMD2 Higher Across Supply Voltage



At ($f_2 - f_1$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-29. IMD2 Lower Across Temperature

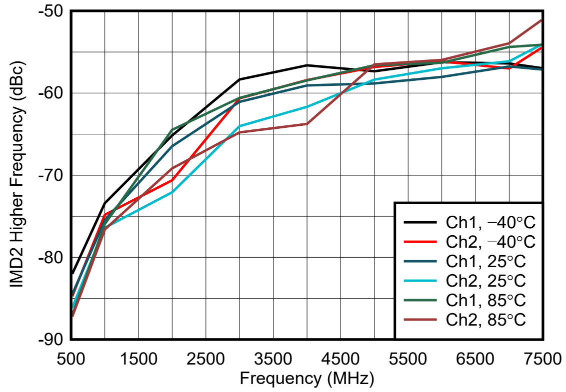


At ($f_2 - f_1$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-30. IMD2 Lower Across Supply Voltage

6.8 Typical Characteristics: D2D Configuration (continued)

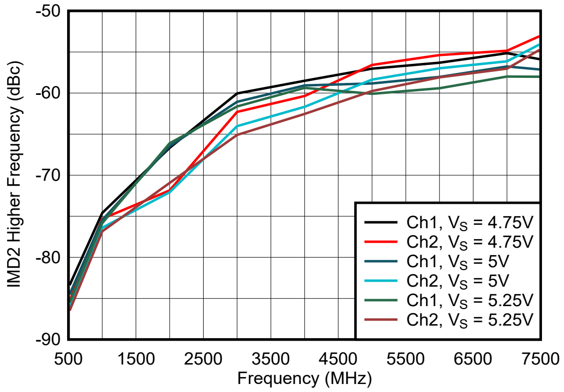
at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



At (f_1 + f_2) frequency where $f_1 < f_2$,

P_O = –5dBm/tone, 2MHz tone spacing

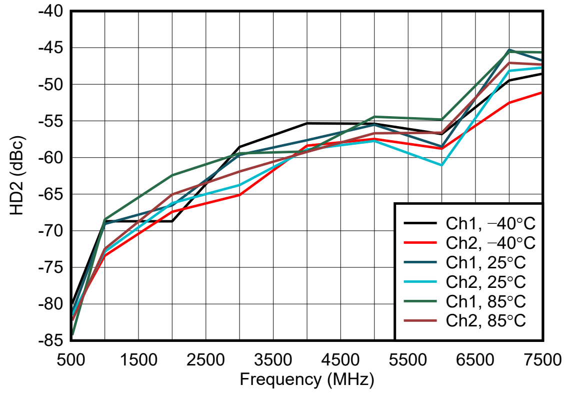
Figure 6-31. IMD2 Higher Across Temperature



At (f_1 + f_2) frequency where $f_1 < f_2$,

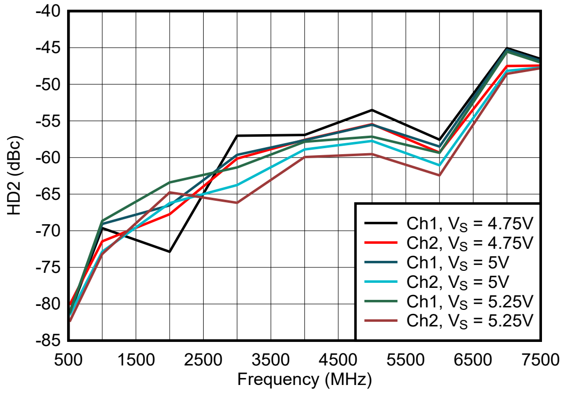
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-32. IMD2 Higher Across Supply Voltage



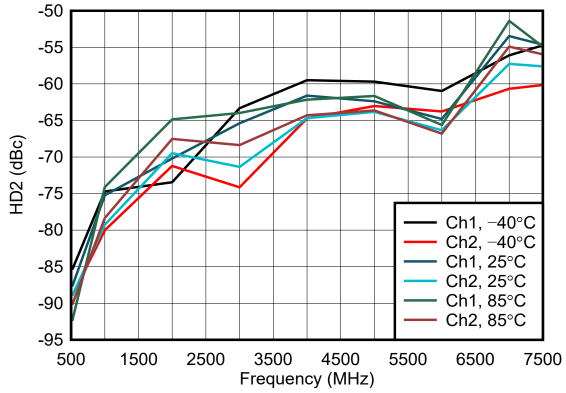
P_O = 7dBm

Figure 6-33. HD2 Across Temperature



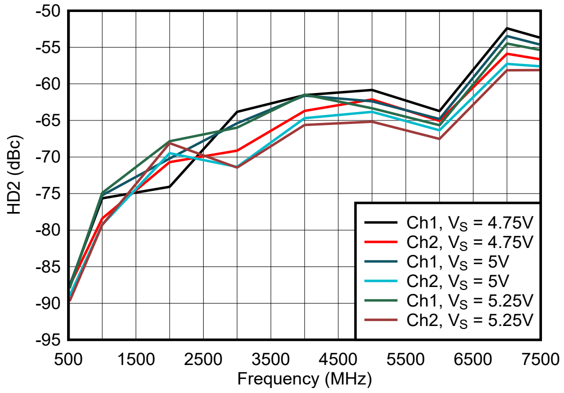
P_O = 7dBm

Figure 6-34. HD2 Across Supply Voltage



P_O = 1dBm

Figure 6-35. HD2 Across Temperature



P_O = 1dBm

Figure 6-36. HD2 Across Supply Voltage

6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

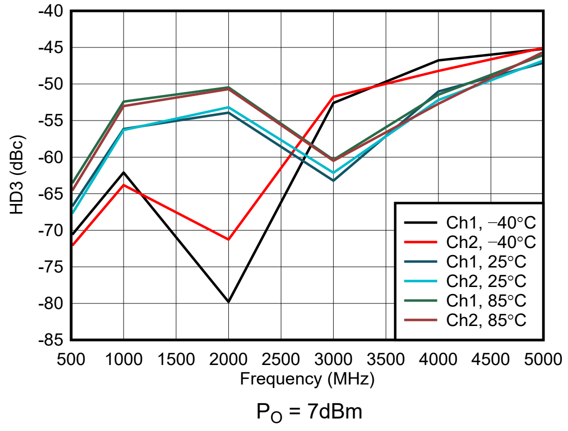


Figure 6-37. HD3 Across Temperature

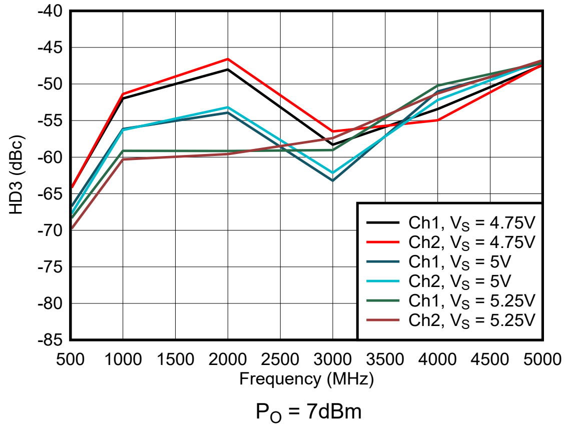


Figure 6-38. HD3 Across Supply Voltage

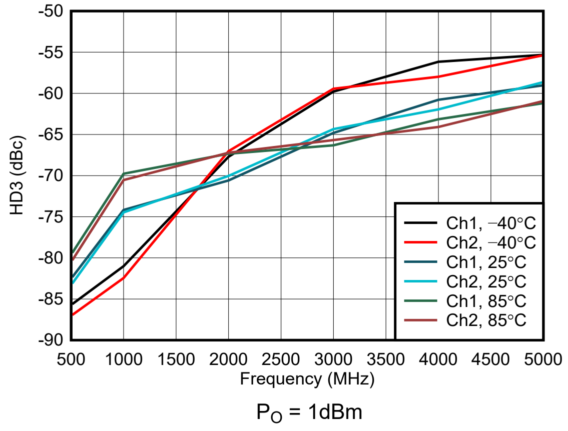


Figure 6-39. HD3 Across Temperature

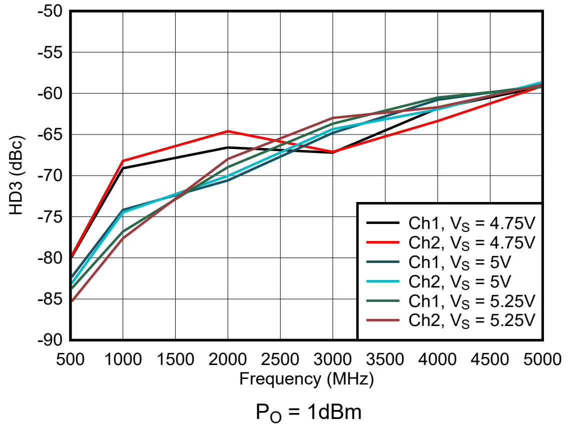


Figure 6-40. HD3 Across Supply Voltage

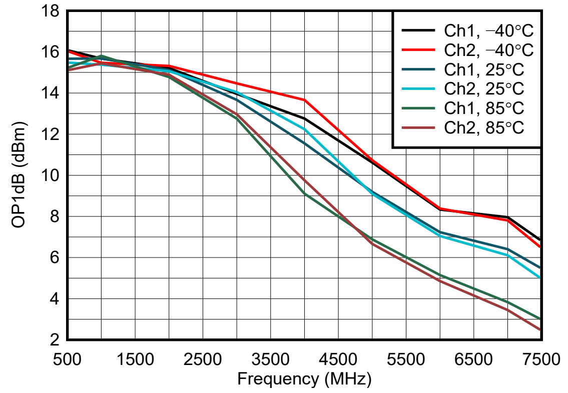


Figure 6-41. OP1dB Across Temperature

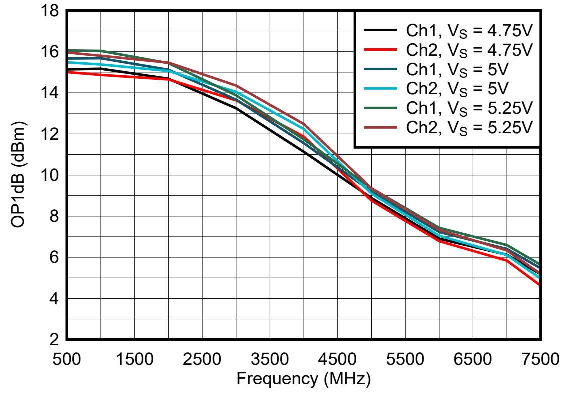


Figure 6-42. OP1dB Across Supply Voltage

6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

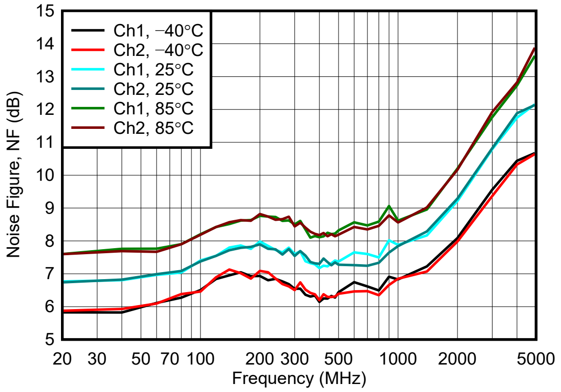


Figure 6-43. Noise Figure Across Temperature

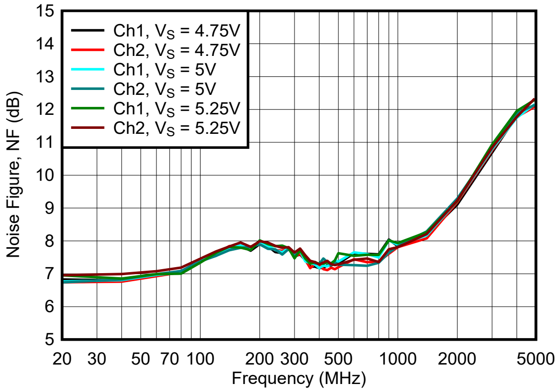
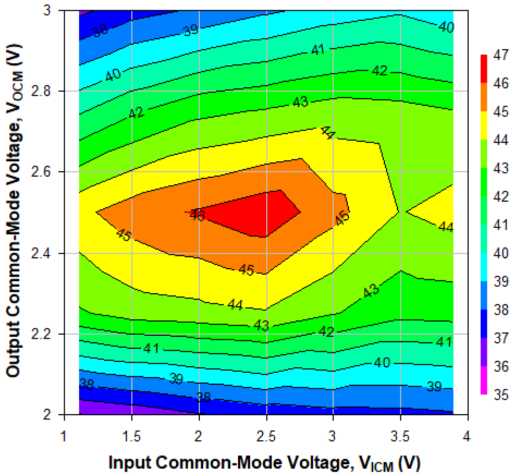
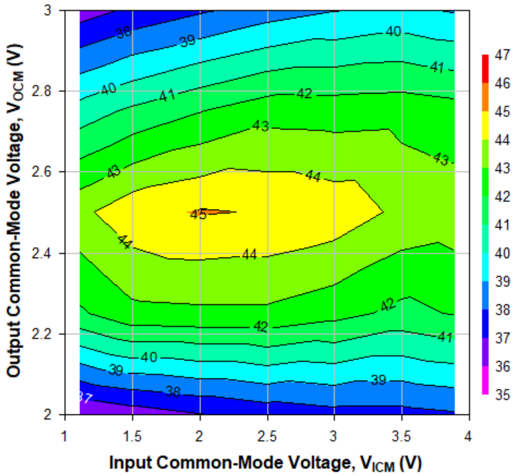


Figure 6-44. Noise Figure Across Supply Voltage



P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-45. OIP3 Across V_{ICM} and V_{OCM} at 500MHz, Ch1

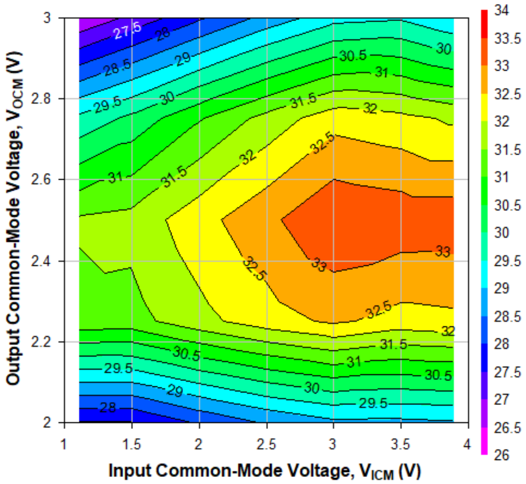


P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-46. OIP3 Across V_{ICM} and V_{OCM} at 500MHz, Ch2

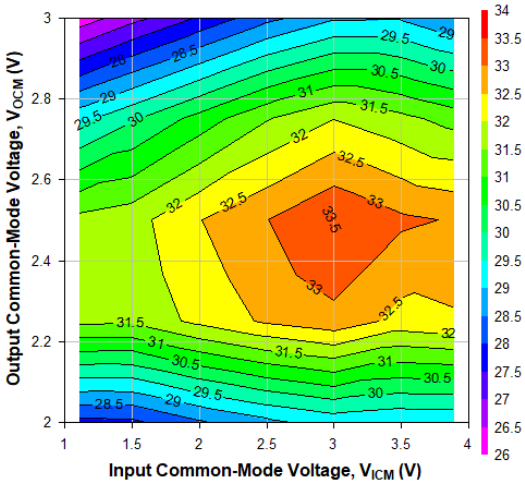
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



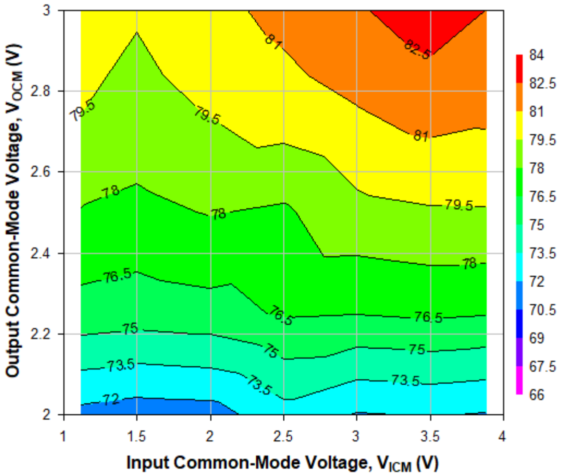
P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-47. OIP3 Across V_{ICM} and V_{OCM} at 2GHz, Ch1



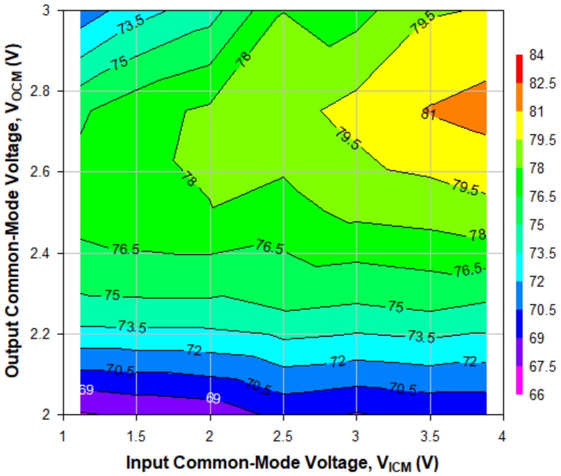
P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-48. OIP3 Across V_{ICM} and V_{OCM} at 2GHz, Ch2



P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-49. OIP2 Across V_{ICM} and V_{OCM} at 500MHz, Ch1

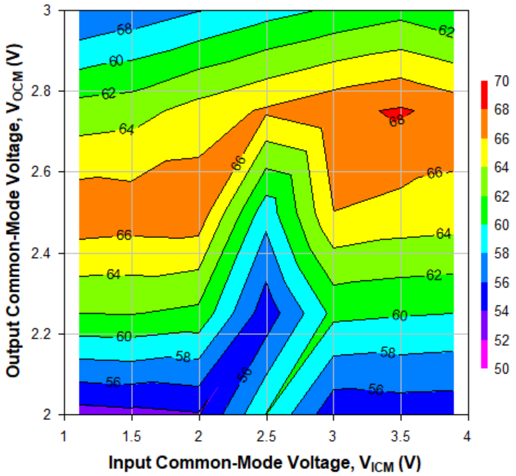


P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-50. OIP2 Across V_{ICM} and V_{OCM} at 500MHz, Ch2

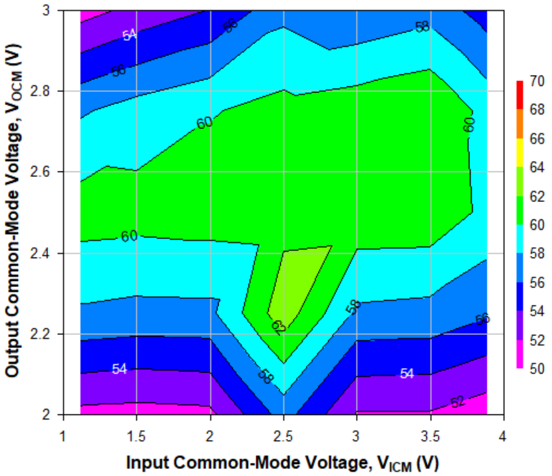
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



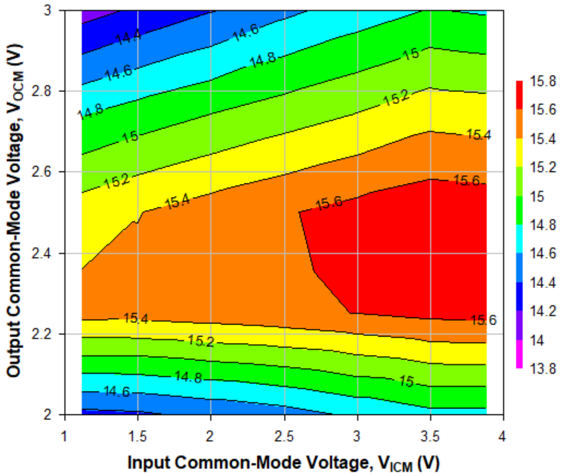
P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-51. OIP2 Across V_{ICM} and V_{OCM} at 2GHz, Ch1



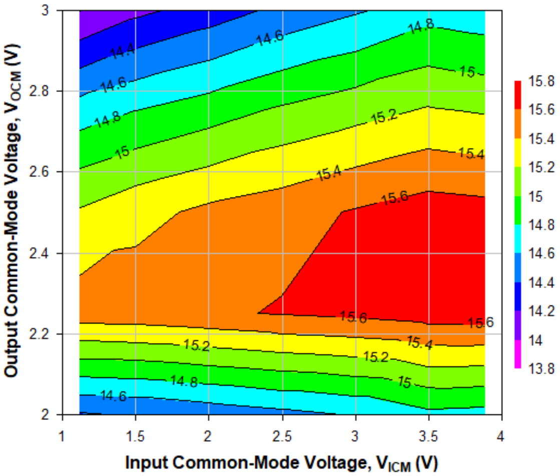
P_O = 1dBm/tone, 2MHz tone spacing, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-52. OIP2 Across V_{ICM} and V_{OCM} at 2GHz, Ch2



dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-53. OP1dB Across V_{ICM} and V_{OCM} at 500MHz, Ch1

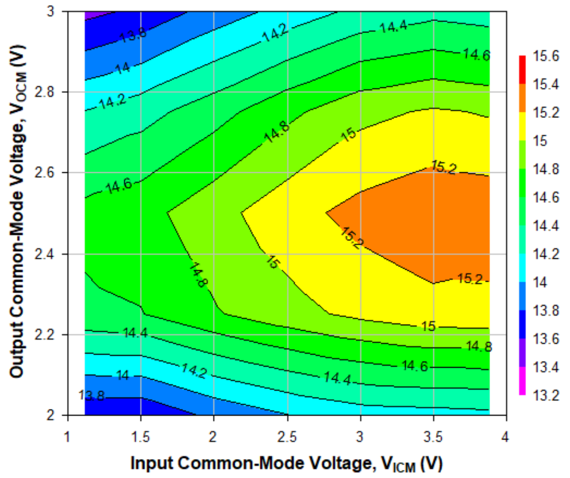


dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-54. OP1dB Across V_{ICM} and V_{OCM} at 500MHz, Ch2

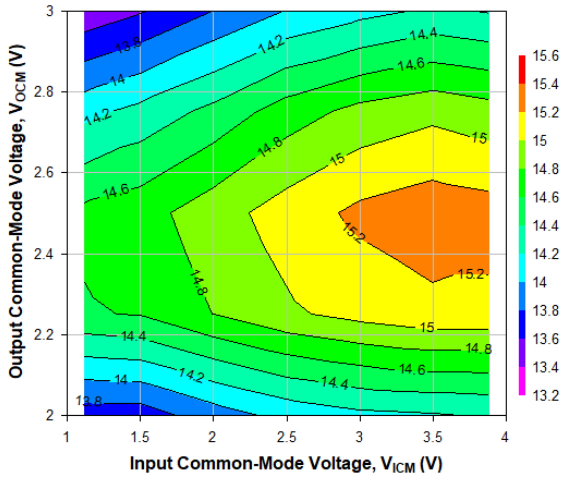
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



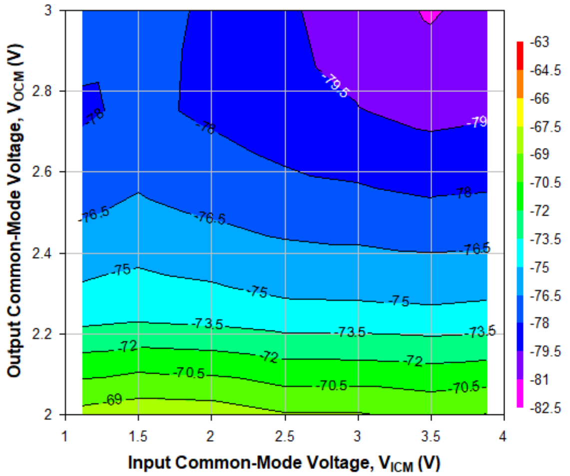
dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-55. OP1dB Across V_{ICM} and V_{OCM} at 2GHz, Ch1



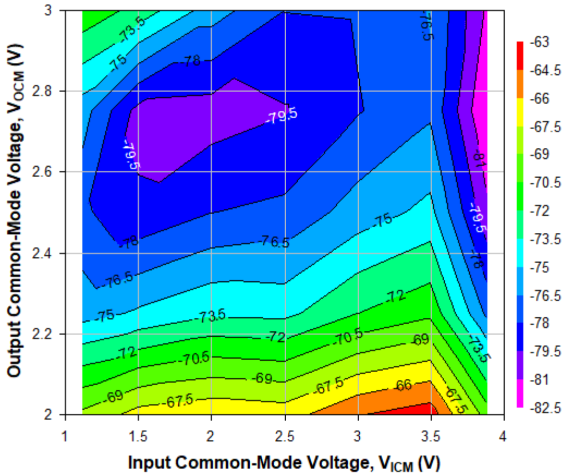
dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-56. OP1dB Across V_{ICM} and V_{OCM} at 2GHz, Ch2



P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-57. HD2 Across V_{ICM} and V_{OCM} at 500MHz, Ch1

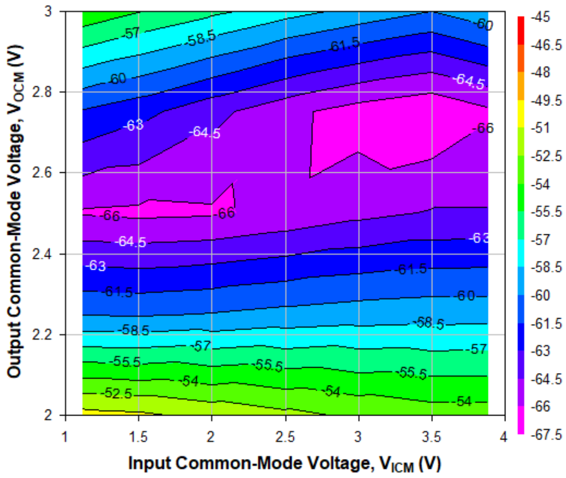


P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-58. HD2 Across V_{ICM} and V_{OCM} at 500MHz, Ch2

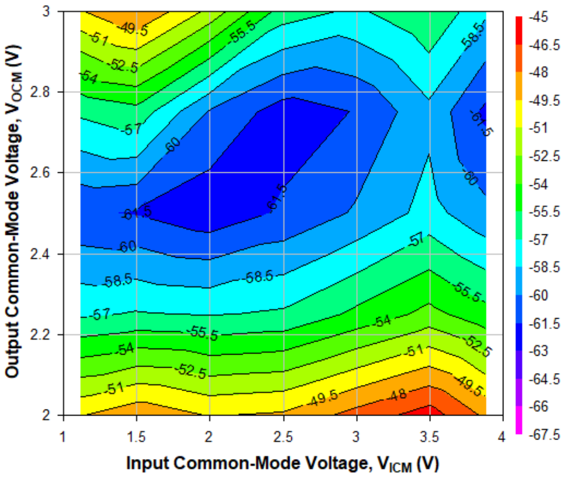
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



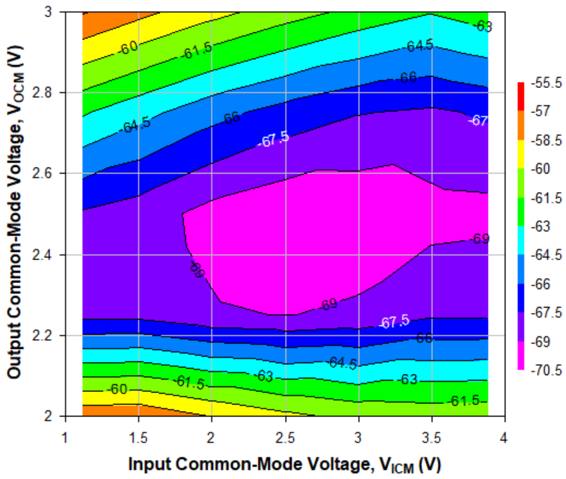
P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-59. HD2 Across V_{ICM} and V_{OCM} at 2GHz, Ch1



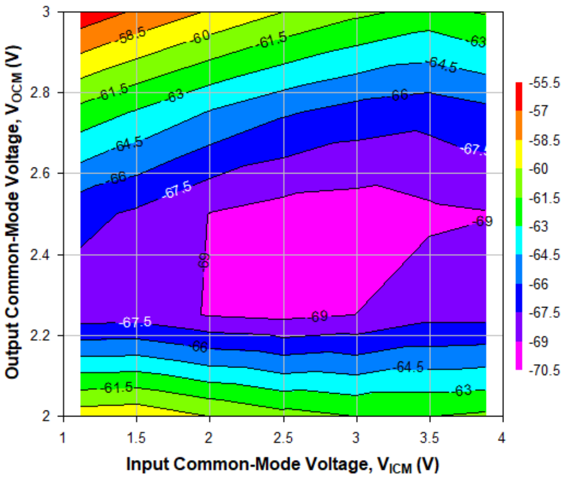
P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-60. HD2 Across V_{ICM} and V_{OCM} at 2GHz, Ch2



P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-61. HD3 Across V_{ICM} and V_{OCM} at 500MHz, Ch1

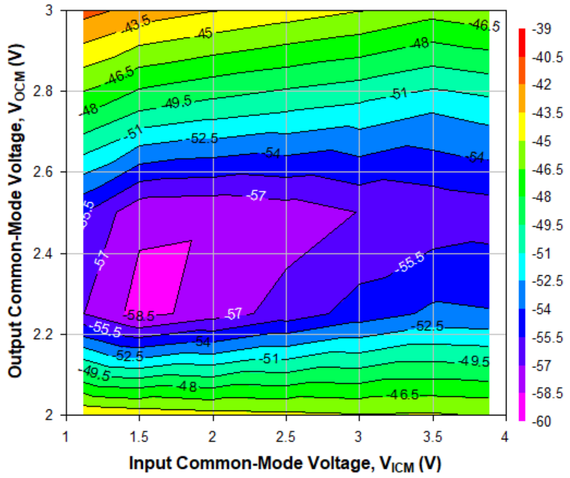


P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-62. HD3 Across V_{ICM} and V_{OCM} at 500MHz, Ch2

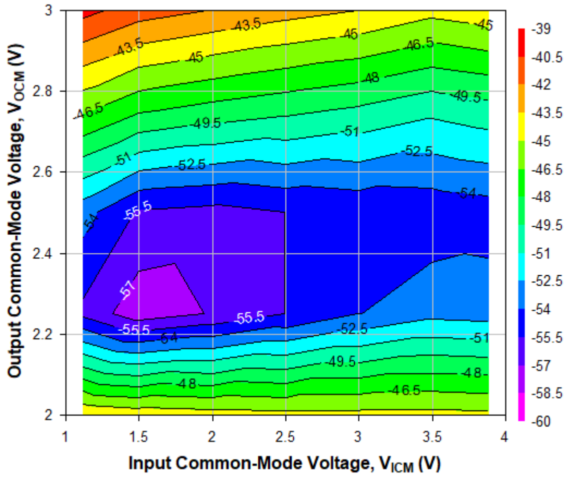
6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



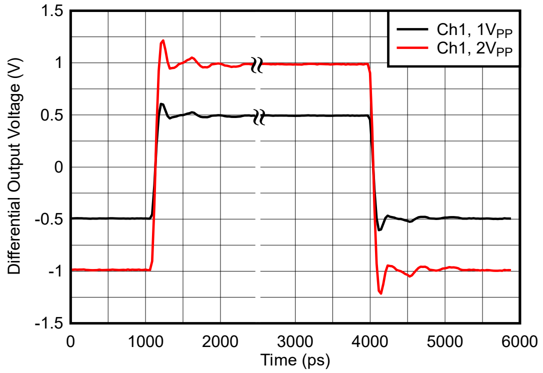
P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-63. HD3 Across V_{ICM} and V_{OCM} at 2GHz, Ch1



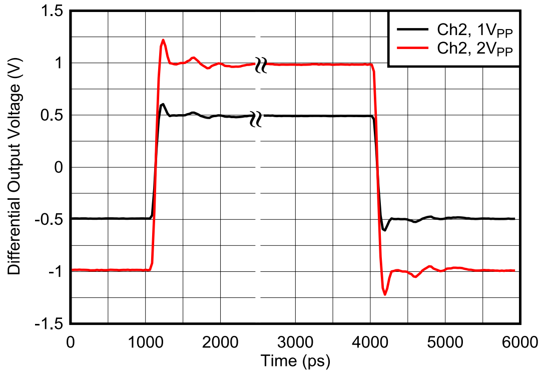
P_O = 7dBm, dc-coupled inputs with V_{ICM} forced through bias tees

Figure 6-64. HD3 Across V_{ICM} and V_{OCM} at 2GHz, Ch2



DC-coupled, V_{S+} = 2.5V, V_{S-} = –2.5V

Figure 6-65. Step Response



DC-coupled, V_{S+} = 2.5V, V_{S-} = –2.5V

Figure 6-66. Step Response

6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

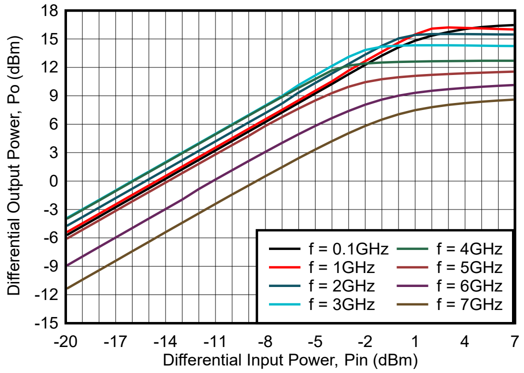


Figure 6-67. Differential Output Power Across Differential Input Power, Ch1

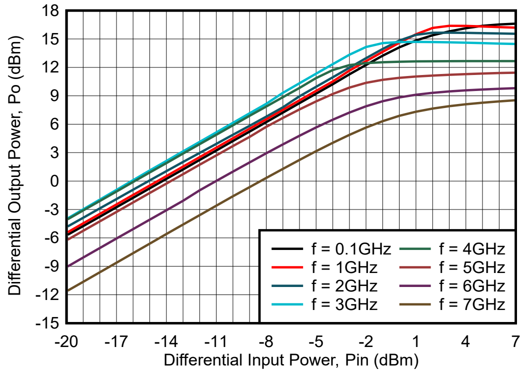
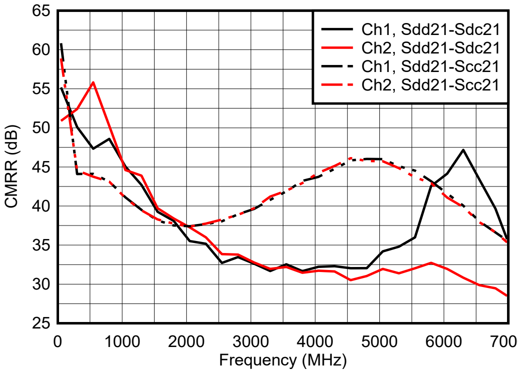
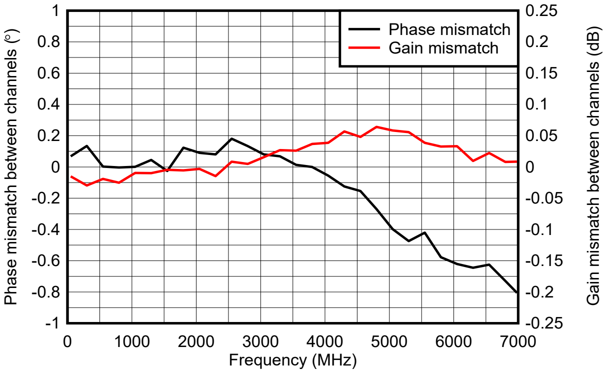


Figure 6-68. Differential Output Power Across Differential Input Power, Ch2



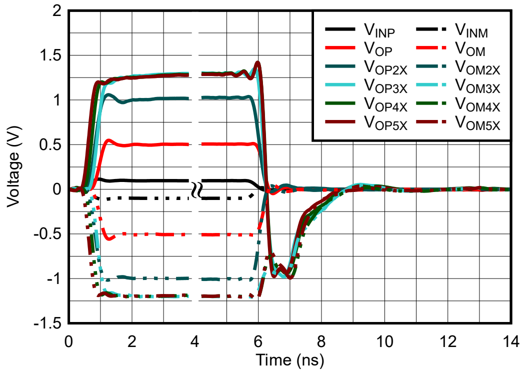
P_{IN} = –20dBm at each driven input pin with 50Ω source, *c* in Sdc21 and Scc21 is for common-mode

Figure 6-69. Common-Mode Rejection Ratio (CMRR)



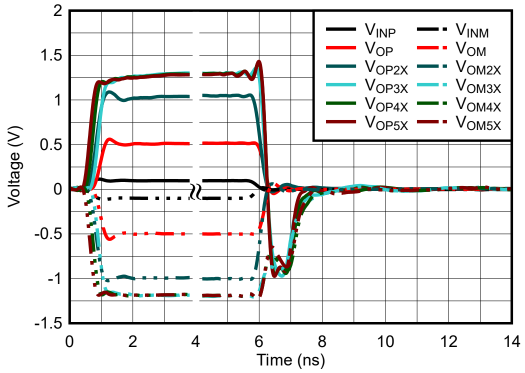
P_{IN} = –20dBm at each driven input pin with 50Ω source

Figure 6-70. Gain and Phase Mismatch Between Channels



DC-coupled, V_{S+} = 2.5V, V_{S-} = –2.5V, 2 to 5 times output voltages are with an input voltage 2 to 5 times of VIN as shown, respectively

Figure 6-71. Overdrive Recovery Response, Ch1

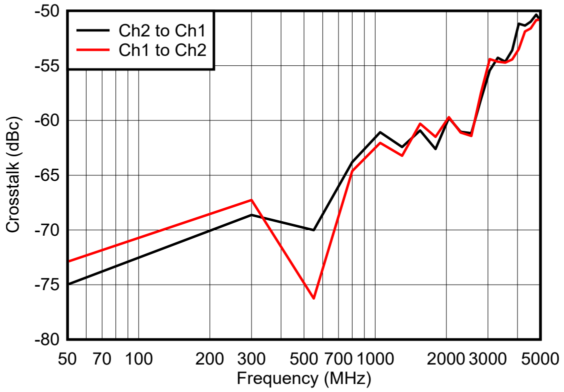


DC-coupled, V_{S+} = 2.5V, V_{S-} = –2.5V, 2 to 5 times output voltages are with an input voltage 2 to 5 times of VIN as shown, respectively

Figure 6-72. Overdrive Recovery Response, Ch2

6.8 Typical Characteristics: D2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see Figure 8-6), inputs de-embedded up to R_{IN_SH} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

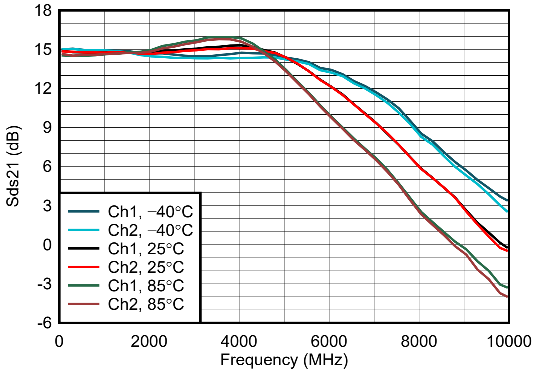


P_{IN} = –20dBm at each driven input pin with 50Ω source

Figure 6-73. Crosstalk

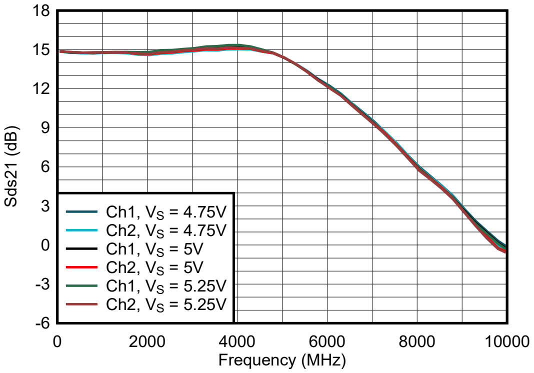
6.9 Typical Characteristics: S2D Configuration

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



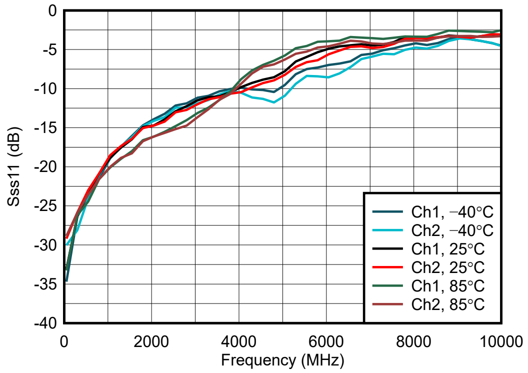
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-74. Power Gain (Sds21) Across Temperature



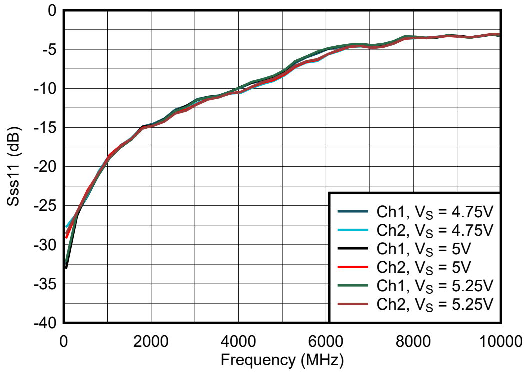
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-75. Power Gain (Sds21) Across Supply Voltage



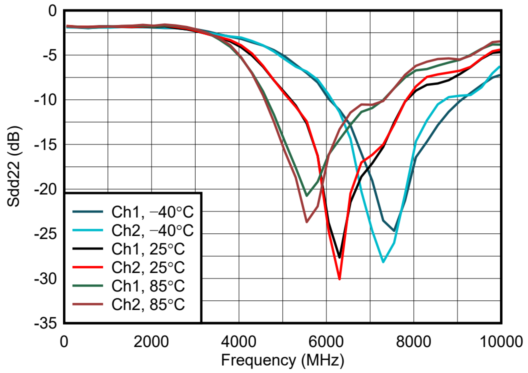
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-76. Input Return Loss (Sss11) Across Temperature



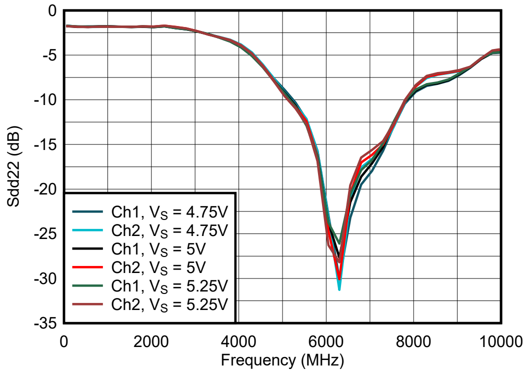
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-77. Input Return Loss (Sss11) Across Supply Voltage



P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-78. Output Return Loss (Sdd22) Across Temperature

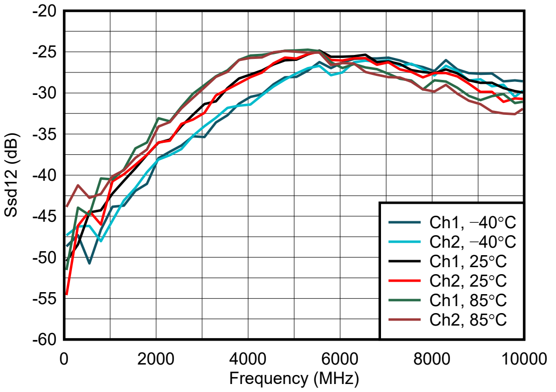


P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-79. Output Return Loss (Sdd22) Across Supply Voltage

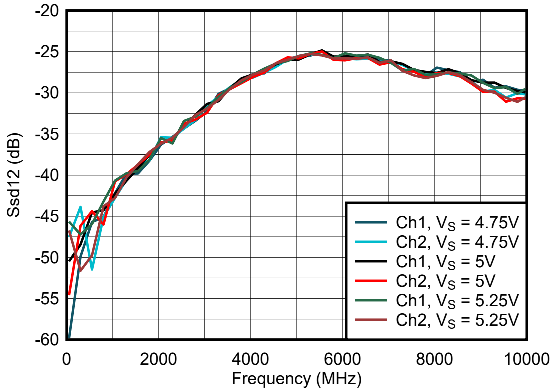
6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



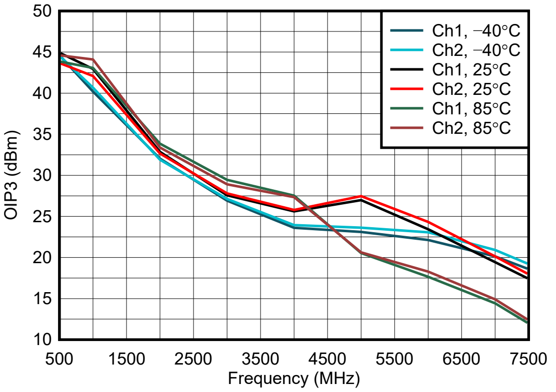
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-80. Reverse Isolation (Ssd12) Across Temperature



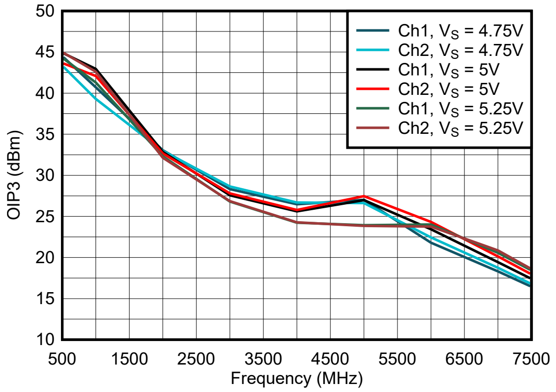
P_{IN} = –20dBm with 50Ω source at all excited ports, nonexcited ports are terminated with 50Ω

Figure 6-81. Reverse Isolation (Ssd12) Across Supply Voltage



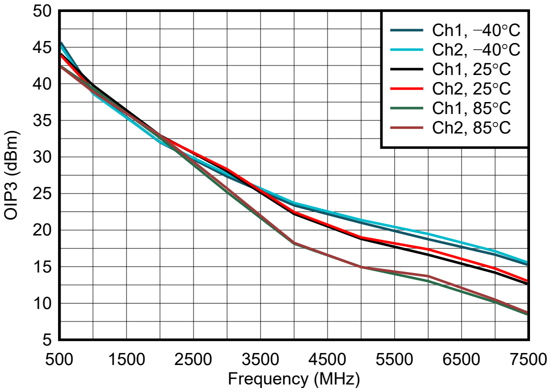
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-82. OIP3 Across Temperature



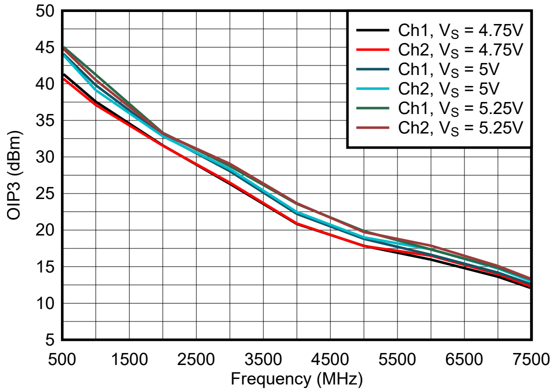
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-83. OIP3 Across Supply Voltage



P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-84. OIP3 Across Temperature

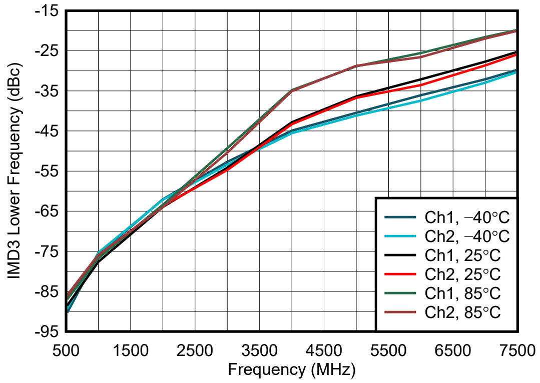


P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-85. OIP3 Across Supply Voltage

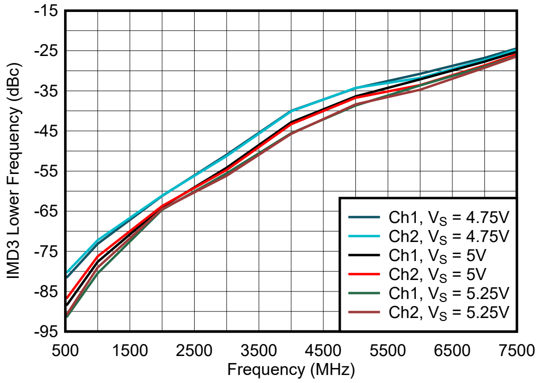
6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



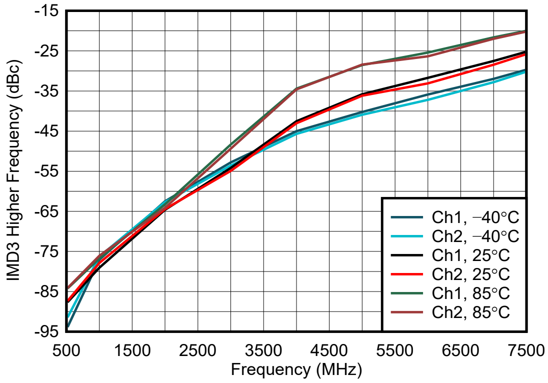
At ($2f_1 – f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-86. IMD3 Lower Across Temperature



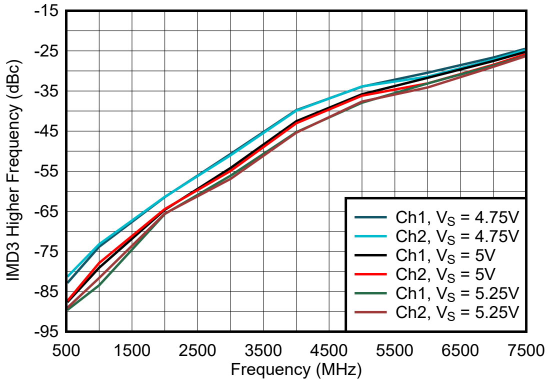
At ($2f_1 – f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-87. IMD3 Lower Across Supply Voltage



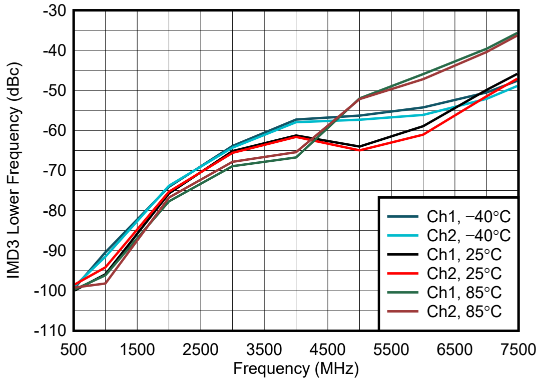
At ($2f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-88. IMD3 Higher Across Temperature



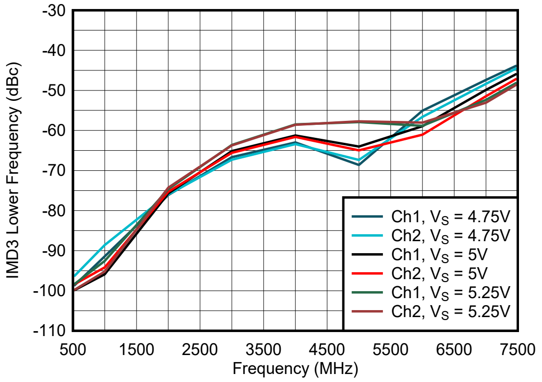
At ($2f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-89. IMD3 Higher Across Supply Voltage



At ($2f_1 – f_2$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-90. IMD3 Lower Across Temperature

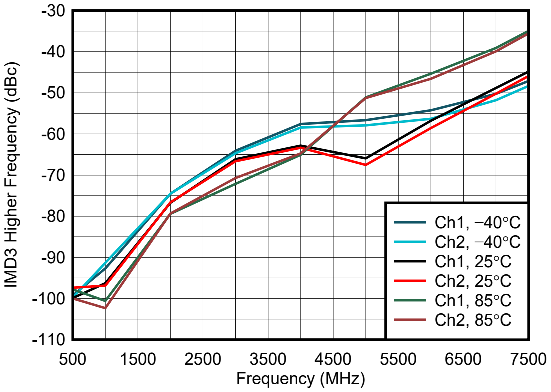


At ($2f_1 – f_2$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-91. IMD3 Lower Across Supply Voltage

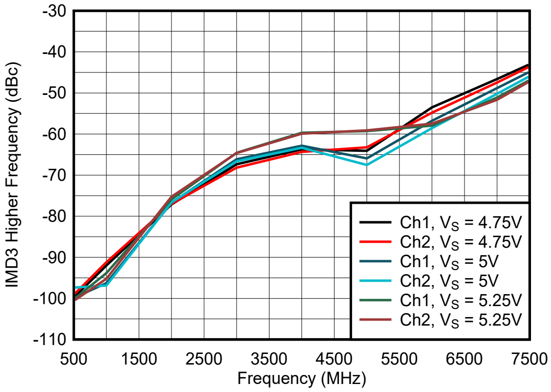
6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



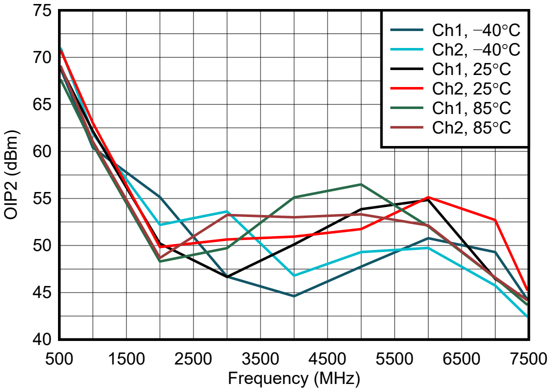
At $(2f_2 – f_1)$ frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-92. IMD3 Higher Across Temperature



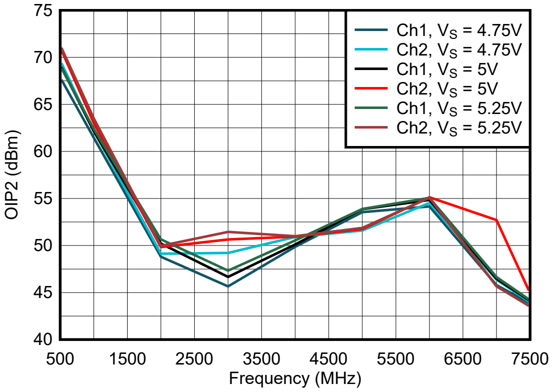
At $(2f_2 – f_1)$ frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-93. IMD3 Higher Across Supply Voltage



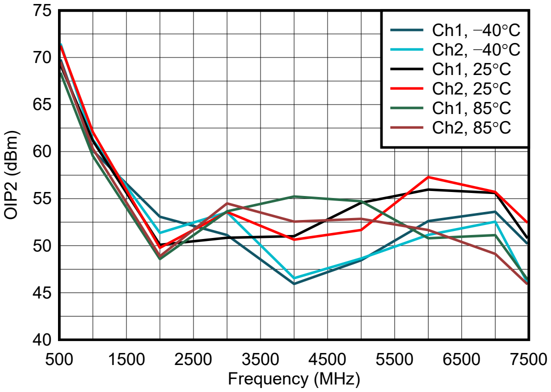
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-94. OIP2 Across Temperature



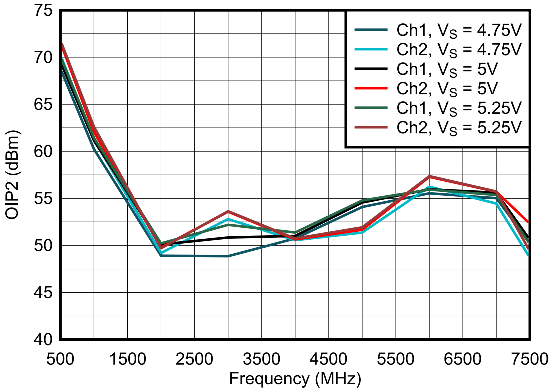
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-95. OIP2 Across Supply Voltage



P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-96. OIP2 Across Temperature

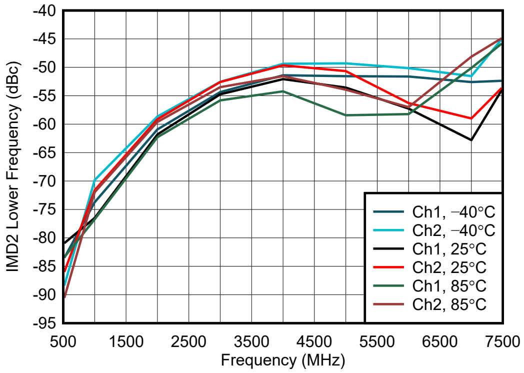


P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-97. OIP2 Across Supply Voltage

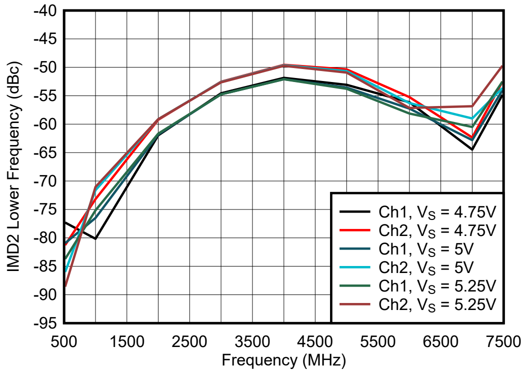
6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



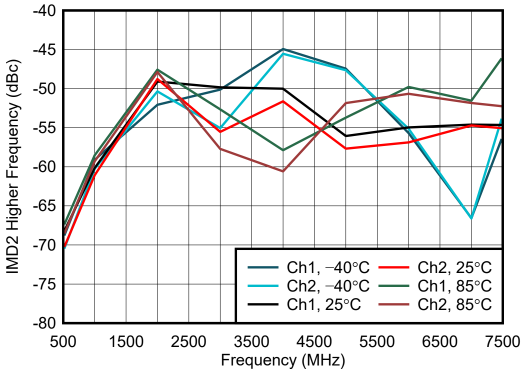
At ($f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-98. IMD2 Lower Across Temperature



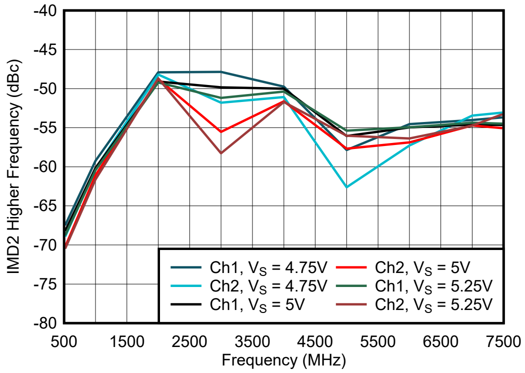
At ($f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-99. IMD2 Lower Across Supply Voltage



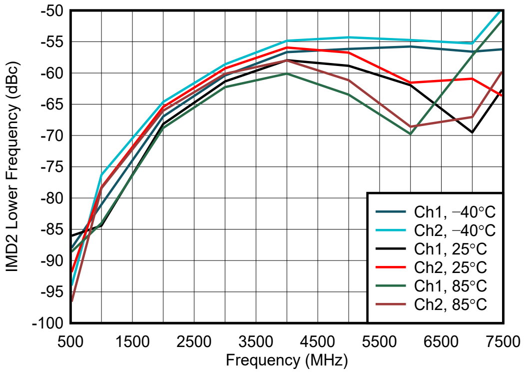
At ($f_1 + f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-100. IMD2 Higher Across Temperature



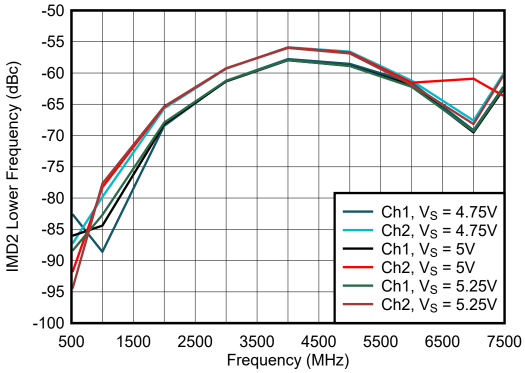
At ($f_1 + f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

Figure 6-101. IMD2 Higher Across Supply Voltage



At ($f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-102. IMD2 Lower Across Temperature

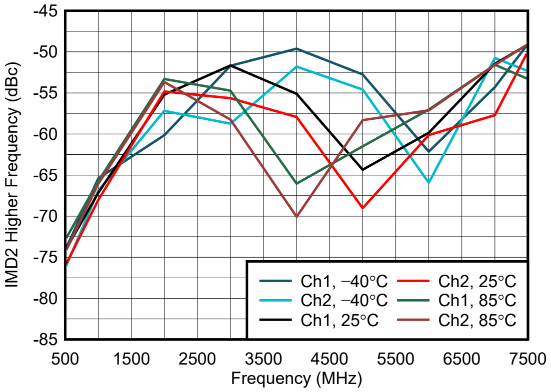


At ($f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-103. IMD2 Lower Across Supply Voltage

6.9 Typical Characteristics: S2D Configuration (continued)

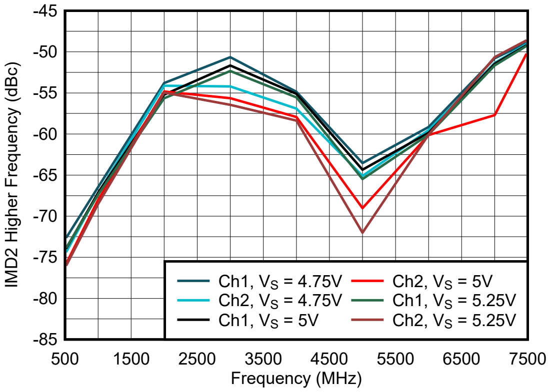
at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



At ($f_1 + f_2$) frequency where $f_1 < f_2$,

P_O = –5dBm/tone, 2MHz tone spacing

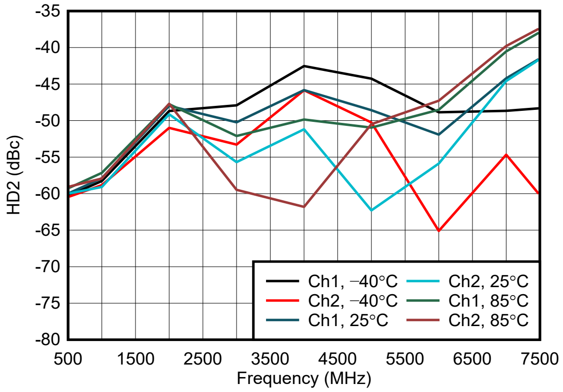
Figure 6-104. IMD2 Higher Across Temperature



At ($f_1 + f_2$) frequency where $f_1 < f_2$,

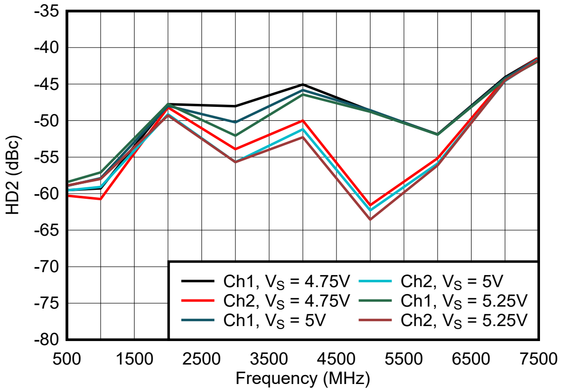
P_O = –5dBm/tone, 2MHz tone spacing

Figure 6-105. IMD2 Higher Across Supply Voltage



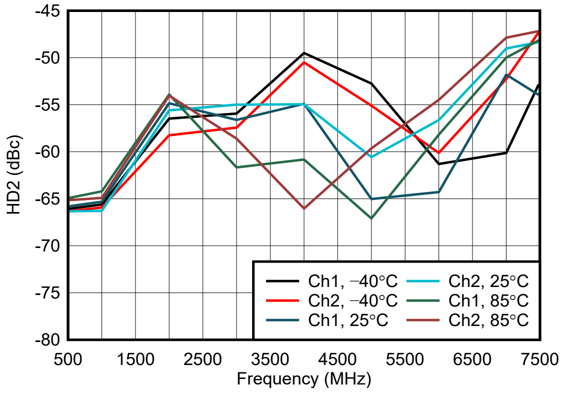
P_O = 7dBm

Figure 6-106. HD2 Across Temperature



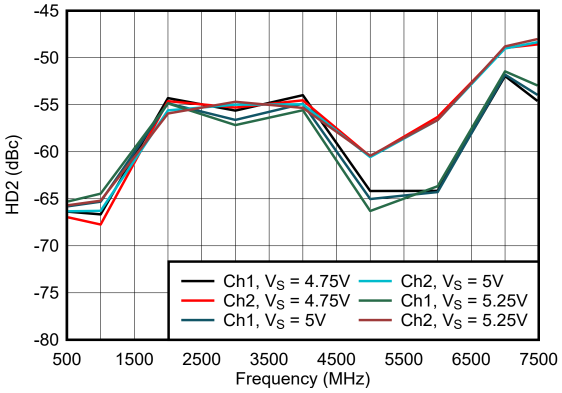
P_O = 7dBm

Figure 6-107. HD2 Across Supply Voltage



P_O = 1dBm

Figure 6-108. HD2 Across Temperature

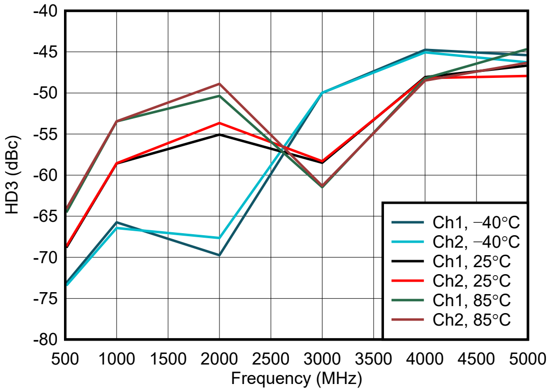


P_O = 1dBm

Figure 6-109. HD2 Across Supply Voltage

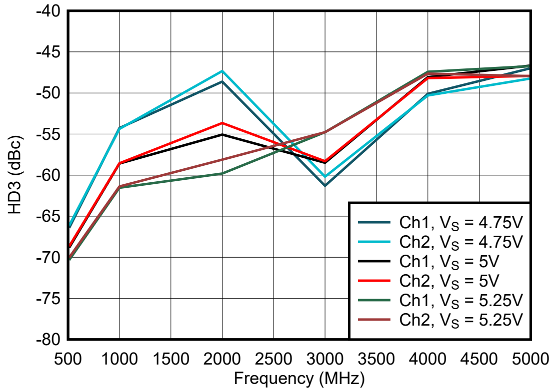
6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



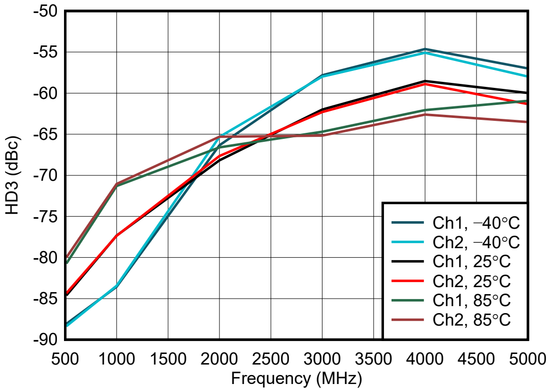
P_O = 7dBm

Figure 6-110. HD3 Across Temperature



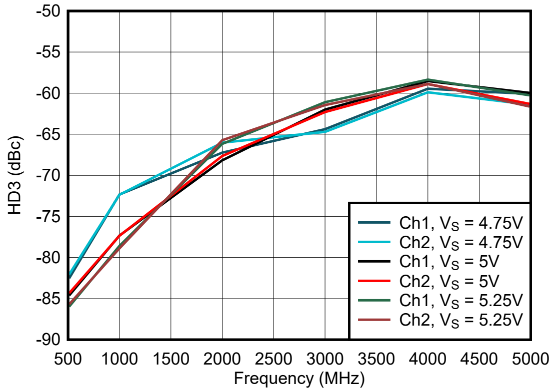
P_O = 7dBm

Figure 6-111. HD3 Across Supply Voltage



P_O = 1dBm

Figure 6-112. HD3 Across Temperature



P_O = 1dBm

Figure 6-113. HD3 Across Supply Voltage

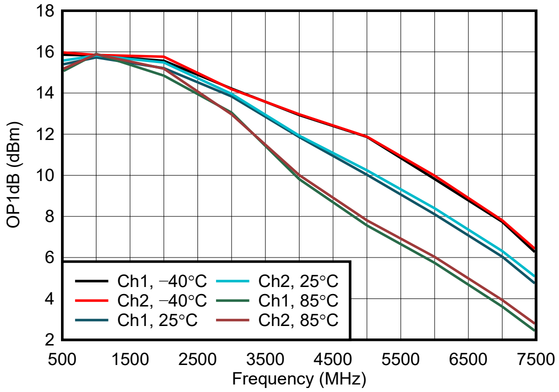


Figure 6-114. OP1dB Across Temperature

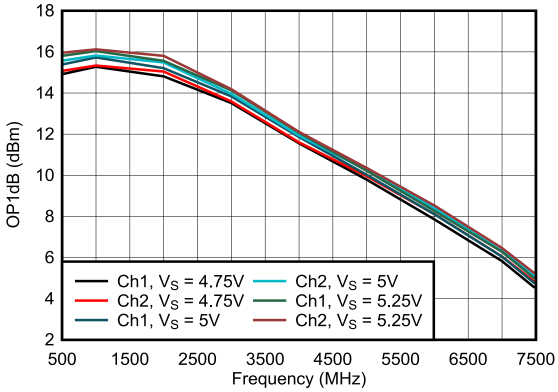


Figure 6-115. OP1dB Across Supply Voltage

6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)

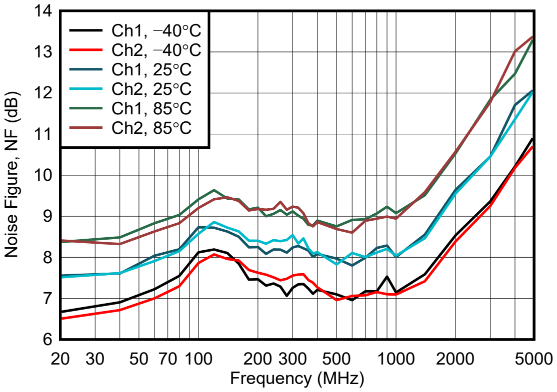


Figure 6-116. Noise Figure Across Temperature

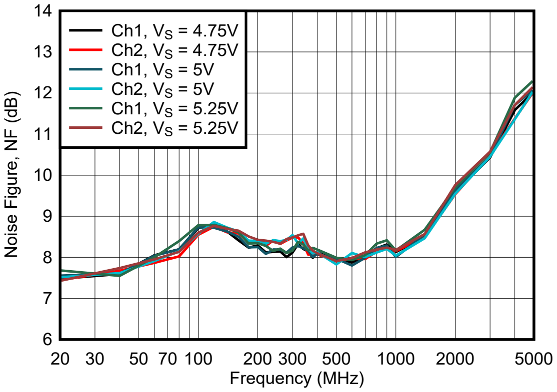
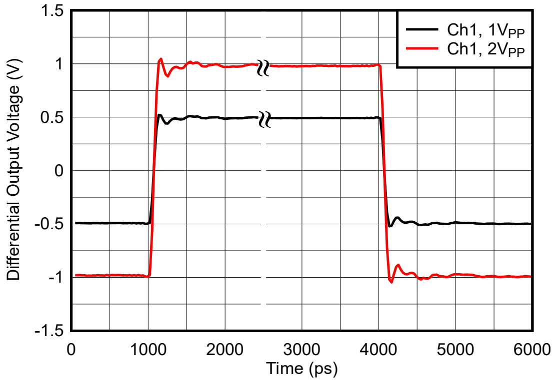
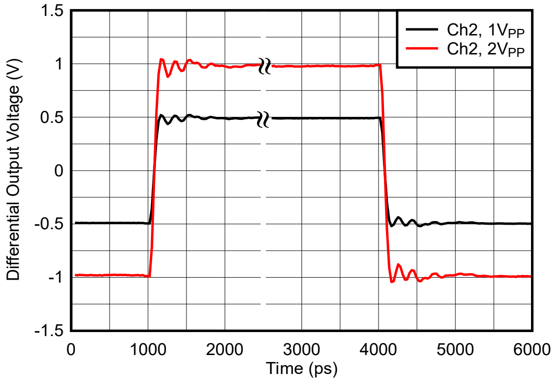


Figure 6-117. Noise Figure Across Supply Voltage



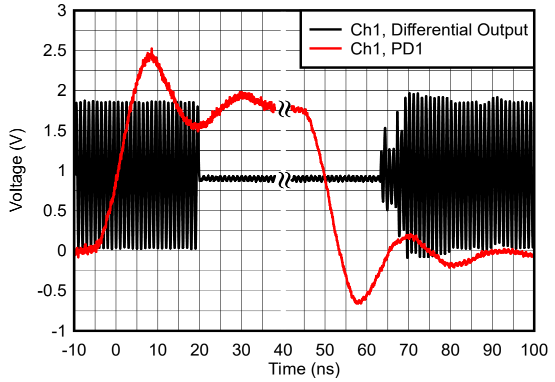
DC-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V

Figure 6-118. Step Response



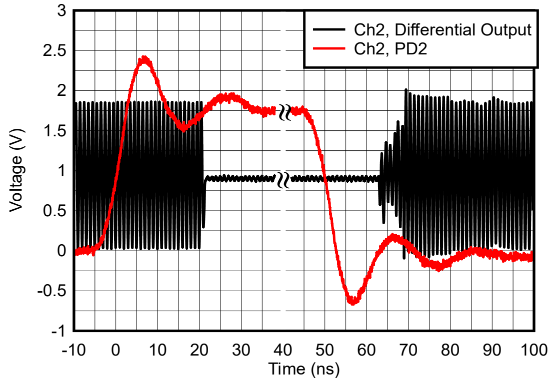
DC-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V

Figure 6-119. Step Response



DC-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V

Figure 6-120. Power Up and Power Down Timing



DC-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V

Figure 6-121. Power Up and Power Down Timing

6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)

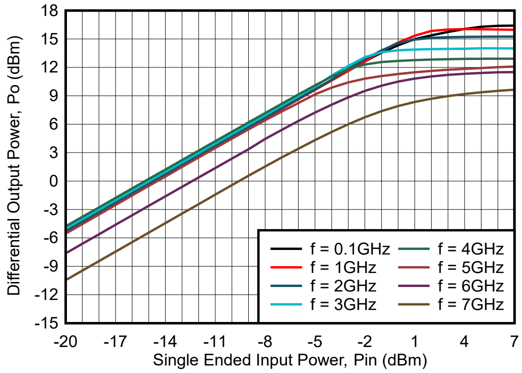


Figure 6-122. Differential Output Power Across Single-Ended Input Power, Ch1

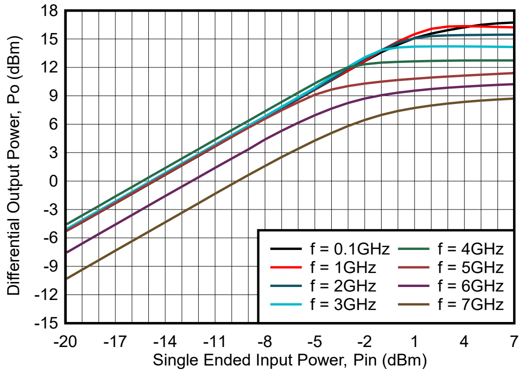
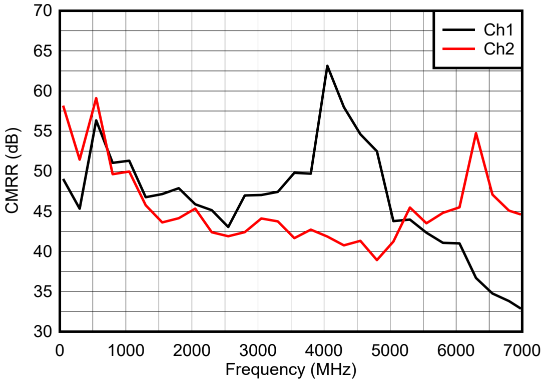
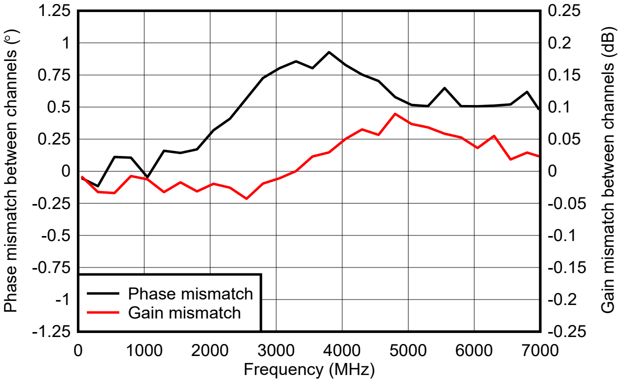


Figure 6-123. Differential Output Power Across Single-Ended Input Power, Ch2



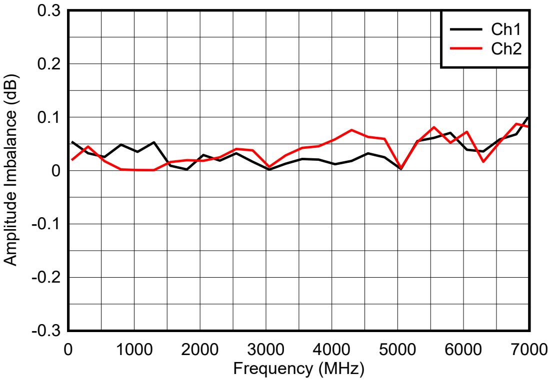
P_{IN} = –20dBm at each driven input pin with 50Ω source

Figure 6-124. Common-Mode Rejection Ratio (CMRR)



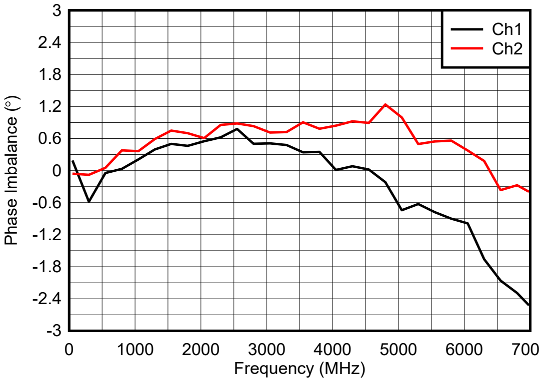
P_{IN} = –20dBm at each driven input pin with 50Ω source

Figure 6-125. Gain and Phase Mismatch Between Channels



P_{IN} = –20dBm at each driven input pin with 50Ω source

Figure 6-126. Amplitude Imbalance

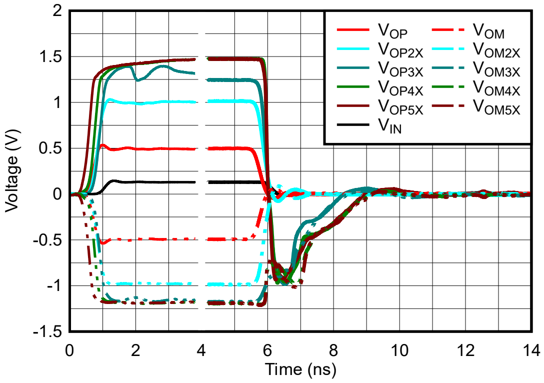


P_{IN} = –20dBm at each driven input pin with 50Ω source

Figure 6-127. Phase Imbalance

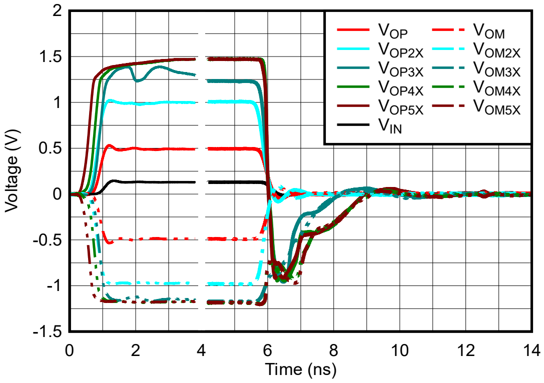
6.9 Typical Characteristics: S2D Configuration (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = mid-supply, S2D ac-coupled input/output configuration with C_{SH} = Open, R_{TERM} = 50Ω, Z_S = 50Ω, Z_L = 100Ω (see Figure 8-4), input and outputs de-embedded up to the device pins, and ambient temperatures shown (unless otherwise noted)



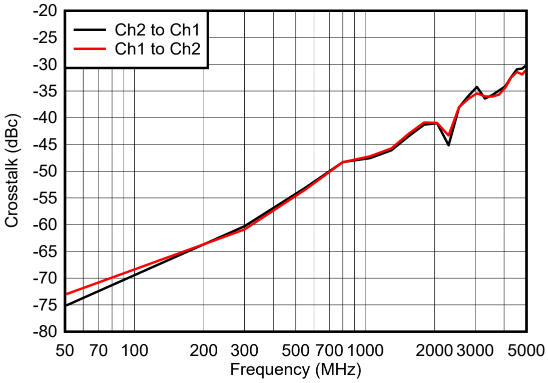
DC-coupled, V_{S+} = 2.5V, V_{S-} = –2.5V, 2 to 5 times output voltages are with an input voltage 2 to 5 times of VIN as shown, respectively

Figure 6-128. Overdrive Recovery Response, Ch1



DC-coupled, V_{S+} = 2.5V, V_{S-} = –2.5V, 2 to 5 times output voltages are with an input voltage 2 to 5 times of VIN as shown, respectively

Figure 6-129. Overdrive Recovery Response, Ch2



P_{IN} = –20dBm at each driven input pin with 50Ω source

Figure 6-130. Crosstalk

7 Detailed Description

7.1 Overview

The TRF1305A2, TRF1305B2, and TRF1305C2 (TRF1305x2) devices are dual-channel, high-performance fully differential RF amplifiers optimized for very wideband signals. This device family is primarily designed to interface with high-speed and RF data converters that often require differential input (ADCs) and output (DACs) signaling. The TRF1305x2 can be dc or ac coupled, and configured as single-ended input and differential output (S2D) or differential input and differential output (D2D). The devices feature an output common-mode pin (VOCM) that allows the flexibility to set a desired common-mode output voltage. The VOCM pin sets the same output common-mode voltage for both shared channels. The amplifier allows the data converters to interface with a dc-coupled IQ demodulator or modulator if used in a direct conversion system. The TRF1305x2 family comes in three fixed power gain variants (15dB, 10dB, and 5dB), and has a closed-loop feedback-amplifier architecture.

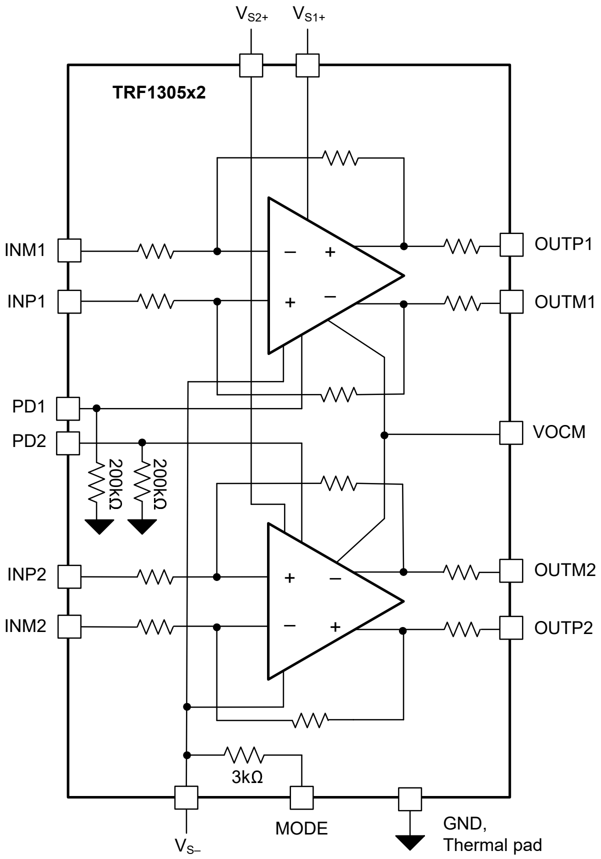
The devices are powered using two-rail supplies with a typical differential voltage of 5V between the positive and negative supplies, and usable in split- or single-supply configurations. A power-down feature is also available that allows each amplifier channel to be powered down individually.

The output of the amplifiers is low impedance. Use appropriate external series termination or resistive pad to match to an arbitrary impedance.

7.2 Functional Block Diagram

This section shows the functional block diagram of the dual-channel TRF1305x2. The output common-mode control pin is common for both channels.

There are certain common internal circuits that are powered by both VS1+ and VS2+. Therefore, short both VS1+ and VS2+ on the board and supply both with a voltage even if only one channel is used. The negative supply, V_{S-}, is shared by both the channels.



7.3 Feature Description

The TRF1305x2 includes the following key features:

- Two-rail floating supply with supply-independent thermal pads
  - Connect the thermal pads to GND
  - RF signals and PDx pins referenced to GND
- Single-supply or split-supply operation
- Supports single-ended and differential input configurations
- Performance-optimized preset fixed-gain variants
- Output common-mode control
- MODE pin: V_{ICM} range extension closer to V_{S+} or V_{S-} modes
- Digital-logic-controllable power-down option

7.3.1 Fully Differential RF Amplifier

The TRF1305x2 are voltage-feedback fully differential amplifiers (FDAs) with wide bandwidth. The amplifiers are designed for a differential power gain of 15dB, 10dB, or 5dB depending on the device variant. These amplifiers have excellent time-domain specifications with high slew rate, high input and output common-mode ranges, and fast transient settling time.

The output average voltage (common-mode) of the FDA device is controlled by a separate common-mode loop. The target output common-mode voltage is set by the VOCM input pin.

7.3.2 Output Common-Mode Control

Figure 7-1 shows a functional diagram of the output common-mode control. Internally, the VOCM pin potential is set by the LDO output voltage that is equal to V_{S-} + 2.5V connected through a 2.5kΩ resistor.

Floating the VOCM pin is allowed. The output common-mode voltage at the output pins, OUTPx and OUTMx, defaults to the LDO output voltage of V_{S-} + 2.5V when VOCM pin is floated. Floating the VOCM pin results in a V_{OCM} voltage equal to midsupply when V_S = 5V. If the VOCM pin is driven, then drive the pin from a low-impedance source. Limit the value of R_{OCM} to less than 25Ω for accurate reflection of the forced V_{OCM} voltage at the device outputs.

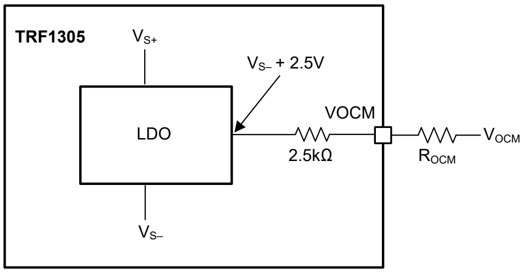


Figure 7-1. Output Common-Mode Control

7.3.3 Internal Resistor Configuration

Figure 7-2 shows the internal resistor configurations of TRF1305x2. Table 7-1 provides the values of these resistors for different gain variants.

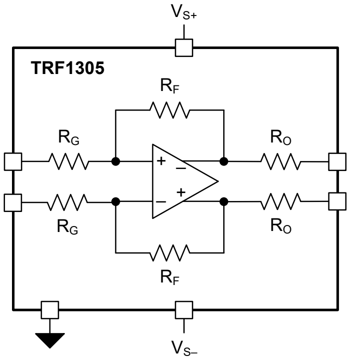


Figure 7-2. TRF1305x2 Internal Resistor Configuration

Table 7-1. Resistor Values

DEVICE NAME	GAIN (dB)	R_G (Ω)	R_F (Ω)	R_O (Ω)
TRF1305A2	15	6.25	258	4
TRF1305B2	10	12.5	161	4
TRF1305C2	5	17	97	4

7.4 Device Functional Modes

7.4.1 MODE Pin

The TRF1305x2 have additional useful features that are configurable using the MODE pin. To select the device mode, either connect a ±2% maximum tolerance pullup resistor between the MODE pin and VS2+, or force a voltage on the MODE pin. Internally, the MODE pin is referenced to $V_{S–}$ through a 3kΩ resistor (see Section 7.2). The selected mode applies to both channels.

Table 7-2 provides the value of the pullup resistor for each mode, the expected voltage (V_{MODE}) at the MODE pin when the pullup resistor is used, or the necessary V_{MODE} voltage to set the device mode and the mode configurations. The V_{MODE} voltage thresholds are approximately midway between the typical V_{MODE} voltage of the adjacent mode. If mode functionality is used, use a decoupling capacitor on the MODE pin.

Table 7-2. MODE Pin Configuration

MODE NUMBER	PULLUP RESISTOR TO VS2+ (±2% MAXIMUM TOLERANCE)	MODE PIN VOLTAGE, V_{MODE} (V)	V_{ICM} RANGE EXTENSION(1)
0	OPEN	$V_{S–}$	Default V_{ICM} range
1	25.6kΩ	$V_{S–}$ + 0.52V	Low side, extends V_{ICM} range closer to $V_{S–}$
2	12.8kΩ	$V_{S–}$ + 0.94V	High side, extends V_{ICM} range closer to V_{S+}
N/A	Do not use pullup resistor < 10kΩ, do not set V_{MODE} > $V_{S–}$ + 1.15V		

(1) Only available in D2D configuration.

To switch the mode without turning the supplies off, use a switch or MUX connected between the pullup resistor options and VS2+, or force a mode-appropriate V_{MODE} voltage. However, best practice is to power down the device using the power-down feature between mode changes; see also Section 7.4.2. The low-side V_{ICM} range extension mode sources current, and the high-side sinks current; see also the following section, *Input Common-Mode Extension*. Maintain that the external circuitry is ready to sink or source these currents before the device is put in the active mode from the powered-down state.

7.4.1.1 Input Common-Mode Extension

When configured in one of the V_{ICM} extension modes, the TRF1305A2 supports a V_{ICM} voltage closer to either V_{S+} or $V_{S–}$ voltage instead of the default specified input common-mode range in the *Electrical Characteristics*. The V_{ICM} extension mode functions only in D2D configuration.

When configured in the low-side V_{ICM} extension mode, the TRF1305A2 supports a 350mV lower input common-mode voltage than the default option. For example, the lower limit of the V_{ICM} voltage range extends from a default value of $V_{S–}$ + 1.5V to $V_{S–}$ + 1.15V for the TRF1305A2 variant, and the higher limit also shifts lower from a default value of $V_{S–}$ + 3.5V to $V_{S–}$ + 3.15V. At the lowest V_{ICM} voltage, approximately 15mA current is sunk by the external circuitry connected to the INPx and INMx pins.

When configured in the high-side V_{ICM} extension mode, the TRF1305A2 supports a 350mV higher input common-mode voltage than the default option. For example, the higher limit of V_{ICM} voltage range extends from a default value of $V_{S–}$ + 3.5V to $V_{S–}$ + 3.85V for the TRF1305A2 variant, and the lower limit also shifts up from a default of $V_{S–}$ + 1.5V to $V_{S–}$ + 1.85V. At the highest V_{ICM} voltage, approximately 15mA current is sourced by the external circuitry connected to the INPx and INMx pins.

Use resistors connected to supplies (or external current sources) to sink currents flowing out of the INPx and INMx pins during the low-side V_{ICM} extension mode, or to source currents flowing into the INPx and INMx pins during the high-side V_{ICM} extension mode.

7.4.2 Power-Down Mode

The TRF1305x2 have two bias modes, active and power-down, that are controlled by the voltage on the PD pin. The PD pin is referenced to GND through a 200kΩ resistor; see also Section 7.2. If the V_{S+} ≥ 3.3V configuration is used, ensure that the PD voltage does not exceed the *Absolute Maximum Ratings* in case the high PD voltage is derived from V_{S+}.

With PD1 and PD2, control each channel independently, and individually power down each channel. Both 1.8V and 3.3V digital logic are supported for power-down control.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Interface Considerations

8.1.1.1 Single-Ended Input

In the single-ended input configuration, one of the amplifier input pins is driven from a source while the other input is terminated with an external resistor. Figure 8-1 shows a dc-coupled, single-ended input configuration driven from and matched to a 50Ω source. Figure 8-1 shows how the non-driven INM pin is terminated with an external resistor to match to a source with the same 50Ω impedance at the INP pin.

C_{SH} in Figure 8-1 is typically open. The performance curves shown in Section 6.9 are with input de-embedded up to device input pin, and output de-embedded up to device output pins. Therefore, Sss11 shown in Section 6.9 represents the input return loss at the amplifier input. The input return loss (Sss11) at C_{SH} is improved by installing C_{SH} with a value of 0.3pF. Figure 8-3 shows this improvement without impacting the frequency flatness within the amplifier bandwidth in Figure 8-2. Using C_{SH} does not impact on noise figure and linearity.

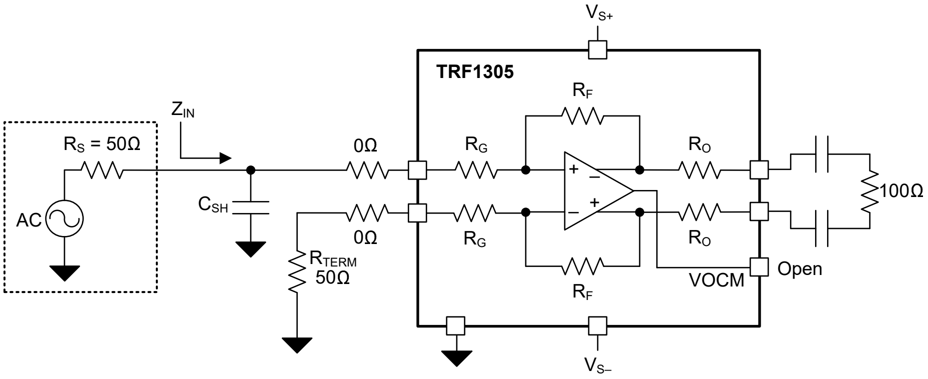
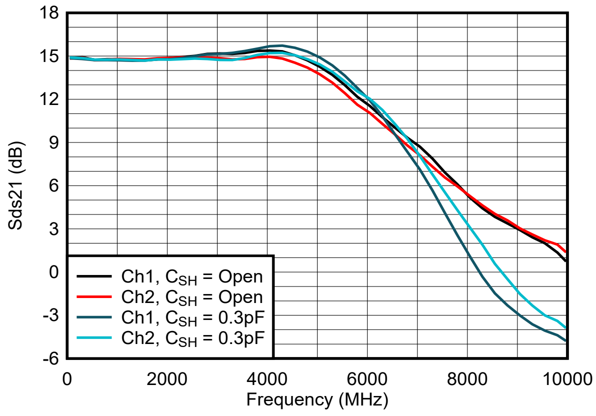
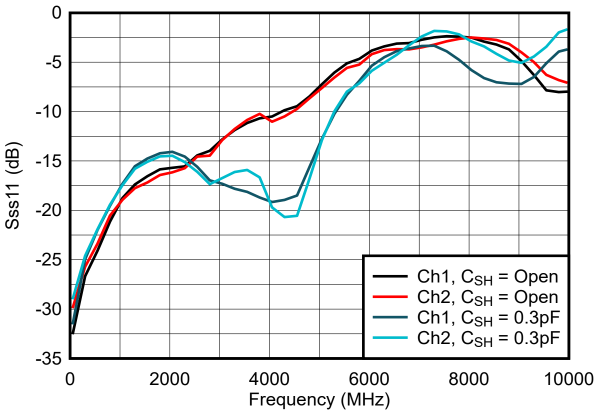


Figure 8-1. DC-Coupled, Single-Ended Input Matched to a 50Ω Source



At T_A = 25°C, V_S = 5V, input de-embedded up to C_{SH}

Figure 8-2. Power Gain (Sds21) Against C_{SH}



At T_A = 25°C, V_S = 5V, input de-embedded up to C_{SH}

Figure 8-3. Input Return Loss (Sss11) Against C_{SH}

Figure 8-4 shows how to configure the design in Figure 8-1 for single-ended, ac-coupled input by adding ac-coupling capacitors in series at the input and output.

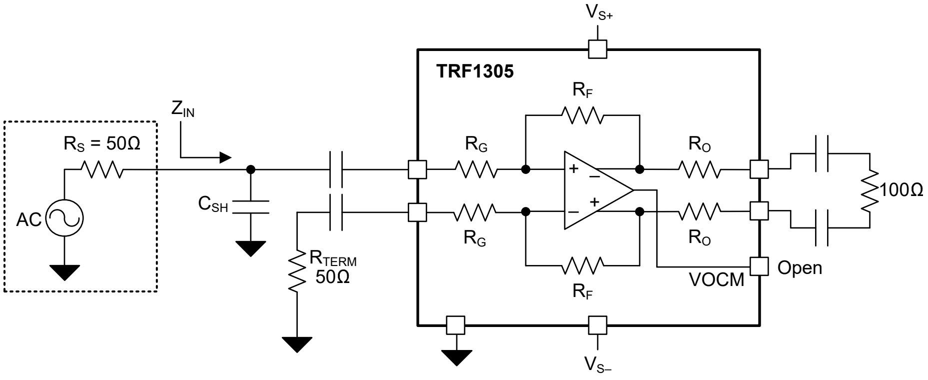


Figure 8-4. AC-Coupled, Single-Ended Input Matched to a 50Ω Source

8.1.1.2 Differential Input

Figure 8-5 shows how a simple network consisting of three resistors is used to match the differential input to a 100Ω differential source. Though the 1kΩ shunt resistor, R_{IN_SH}, does not have any impact at dc to low frequencies, the resistor is necessary to get the full wideband performance from TRF1305x2. Figure 8-6 shows the configuration for ac-coupled differential input designs. The resistors values shown in Figure 8-5 and Figure 8-6 work for all gain versions of the TRF1305x2 for an 100Ω input match to a 100Ω differential source.

Use high-frequency (RF) resistors (0201 preferred), for high-frequency (RF) matching.

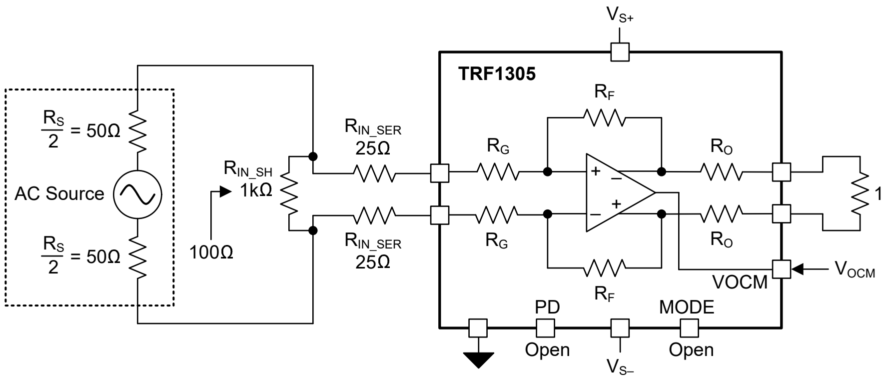


Figure 8-5. DC-Coupled Differential Input Matched to a 100Ω Differential Source

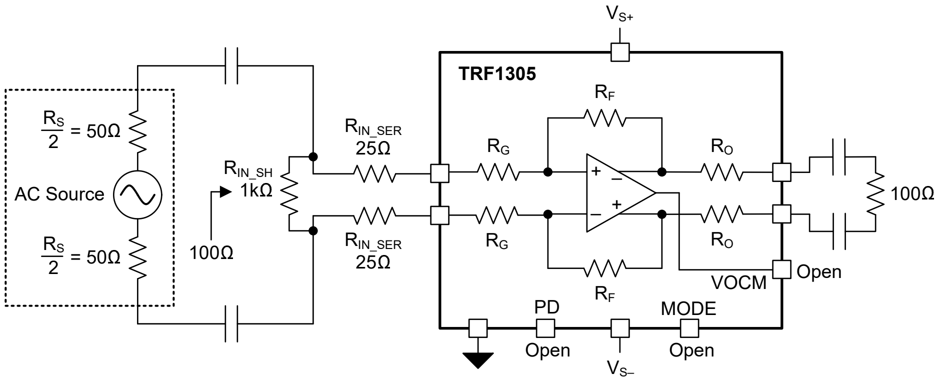


Figure 8-6. AC-Coupled Differential Input Matched to a 100Ω Differential Source

8.1.1.3 DC-Coupling Considerations

The TRF1305x2 accept a wide range of input dc common-mode (CM) voltages. Take into consideration the dc current loading of the source when the TRF1305x2 is dc coupled at the input. Figure 8-7 shows that when the input CM voltage, V_{ICM}, is different than the output CM voltage, V_{OCM}, a net dc current flow from or to the source occurs. Equation 1 shows the relationship that the source or sink current, I_{CM}, has with the input and output CM voltages:

$$I_{CM} = \frac{(V_{OCM} - V_{ICM})}{(R_F + R_G)} \qquad (1)$$

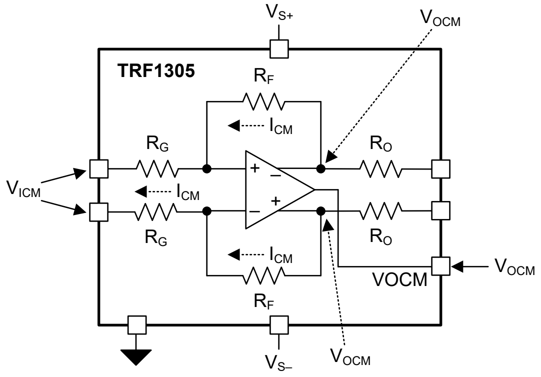


Figure 8-7. Net DC Current Flow When Input and Output Common-Mode Voltages are not Equal

8.1.2 Gain Adjustment With External Resistors in a Differential Input Configuration

The TRF1305x2 allow minor gain adjustments by configuring the input external resistive network that is part of the differential input configuration. Figure 8-8 shows the external input network that comprises of a shunt resistor, R_{IN_SH}, and two series input resistors, R_{IN_SER}, connected to the input pins of the amplifier.

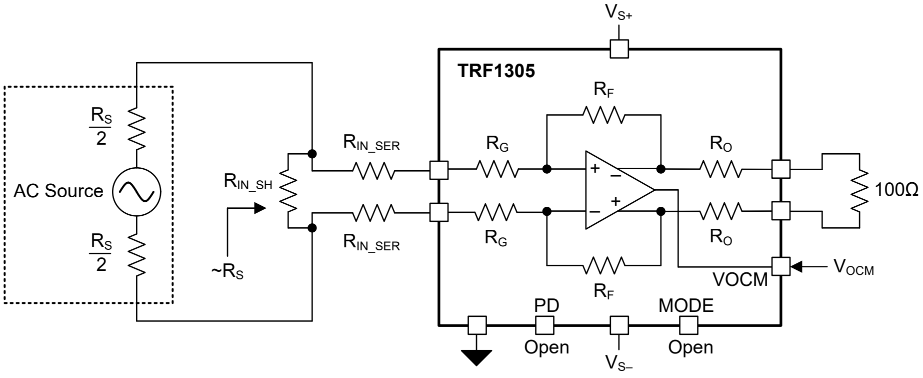


Figure 8-8. Gain Adjustment With External Resistor Network

Table 8-1 provides resistor configurations for a 100Ω differential source impedance.

Table 8-1. Resistor Table for R_S = 100Ω

TRF1305A2		
POWER GAIN (dB)	**R_{IN_SH} (Ω)**	**R_{IN_SER} (Ω)**
15	1000	25
14	365	29
13	233	33
12	176	38
11	145	43
10	125	49

Use external resistive attenuation network only for small gain adjustments because there is a dB-to-dB noise figure degradation with the resistive attenuators. Use an amplifier version that requires minimal attenuation for achieving the overall gain.

8.2 Typical Application

8.2.1 TRF1305A2 as ADC Driver in a Zero-IF Receiver

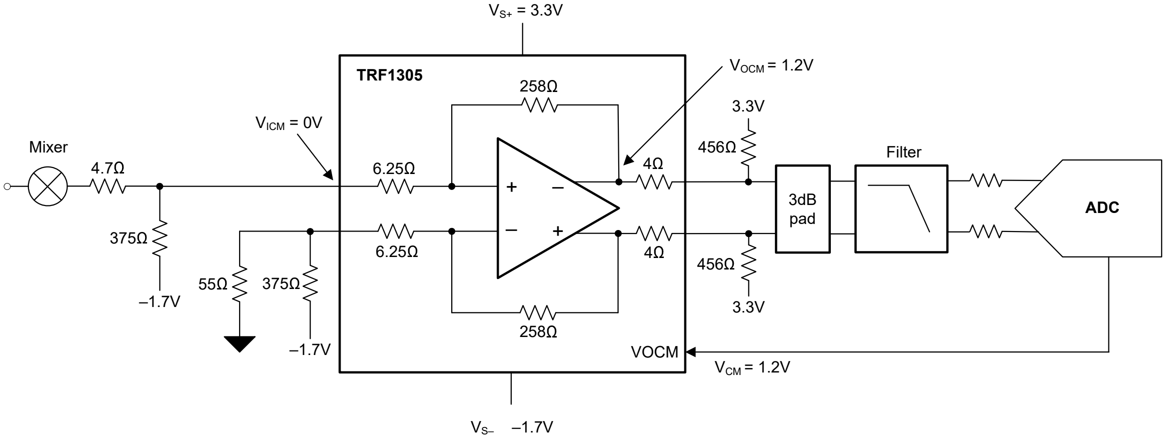


Figure 8-9. TRF1305A2 as ADC Driver in a Zero-IF Receiver

Consider a zero-IF (direct down conversion) application with an IQ demodulator interfaced to a pair of ADCs. In this case, the TRF1305A2 is used as an interface amplifier between the demodulator and the ADCs. The dc common-mode of the demodulator output and ADC input are different. The TRF1305A2 dc couples the demodulator to ADC without degrading the signal integrity of the signal chain.

8.2.1.1 Design Requirements

The primary design requirement for an IQ demodulator application is to interface a pair of passive mixers with an RF ADC. The mixers have a 0V common-mode voltage. The ADC requires an input common-mode voltage of 1.2V with full-scale swing of 1.35V_{PP}. Choose the power supplies, and design the input/output network for the TRF1305A2 as the ADC driver amplifier, to perform the dc level shifting and amplification function.

8.2.1.2 Detailed Design Procedure

The first step is to choose the TRF1305A2 supplies. Maintain that the midsupply voltage, $V_{MIDSUPPLY}$, is between the ADC common-mode (CM) voltage and the mixer CM voltage. $V_{MIDSUPPLY}$ is typically positioned closer to the ADC CM because the output CM range of the amplifier is less than the input CM range. Maintain that the dc of the signal at the input and output of the amplifier are within the valid operating common-mode voltage range. Use the MODE pin for cases where an extended range of the input CM is required.

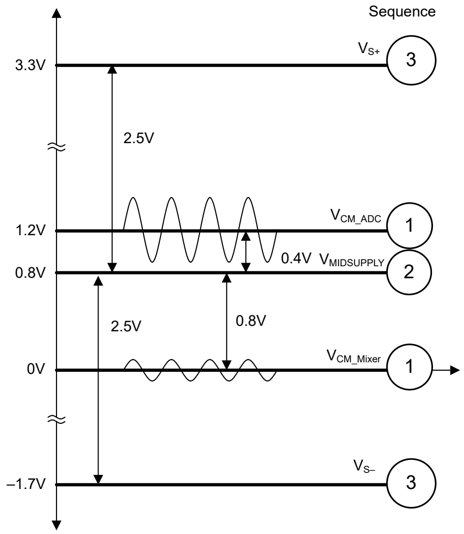


Figure 8-10. Choosing Supply Voltages With Given Common-Mode Voltages

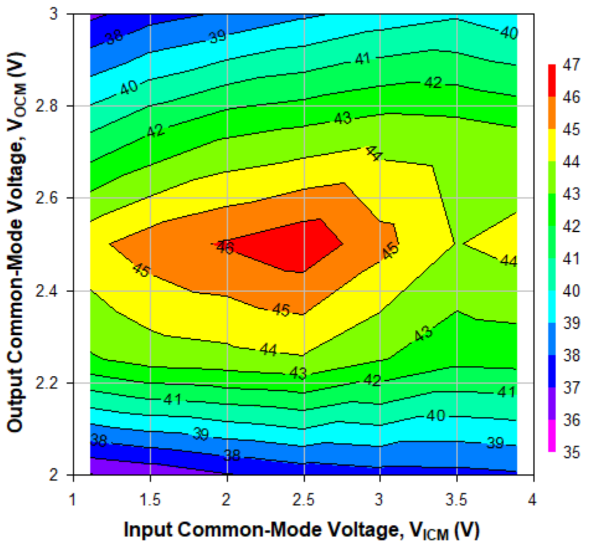
Figure 8-10 shows how $V_{MIDSUPPLY}$ is chosen to be 0.8V, so that the amplifier input has a CM offset from $V_{MIDSUPPLY}$ of 0.8V and output has a CM offset from $V_{MIDSUPPLY}$ of 0.4V (1.2V – 0.8V). The CM offsets are within the valid common-mode range of the amplifier, so the supplies of the TRF1305A2 are chosen to be V_{S+} = 3.3V (0.8V + 2.5V) and V_{S-} = −1.7V (0.8V – 2.5V). Further optimization in the choice of supply is possible by selecting the input and output CM voltages for the best OIP3 performance. Section 8.2.1.3 has contour graphs that show OIP3 across input and output common-mode voltages.

The output CM is greater than the input CM; therefore, a net 4.54mA ((1.2V – 0V) / (258Ω + 6.25Ω)) dc current flows from the output to input through the internal feedback resistors. Depending on the choice of the passive mixer, this current can required to be sunk outside the mixer so that the bias conditions of the mixer are not disturbed. A 375Ω pulldown resistor connected to the INP pin to −1.7V supply is adequate. If the 4.54mA dc current is sourced entirely from the amplifier, then the output headroom can be affected. Therefore, source the current externally from the supply using a pair of pullup resistors connected to the amplifier outputs; 456Ω pullup resistors from OUTP and OUTM to 3.3V are adequate.

The I-channel mixer output has a 50Ω port and is connected to the amplifier INP pin through a small (4.7Ω) series resistor. The INM pin is terminated to ground through a 55Ω resistor and to −1.7V through a 375Ω resistor. This configuration allows the amplifier to have the same input impedance at each of the INP and INM input pins. The impedance of the mixer is close to 43Ω and provides better than a −20dB return loss (theoretically). Be aware that there is some drop in the gain due to these resistor networks. The values of the resistors chosen in Figure 8-9 are a good starting point; in practice, some adjustment is often needed to simultaneously meet the dc conditions and the RF performance.

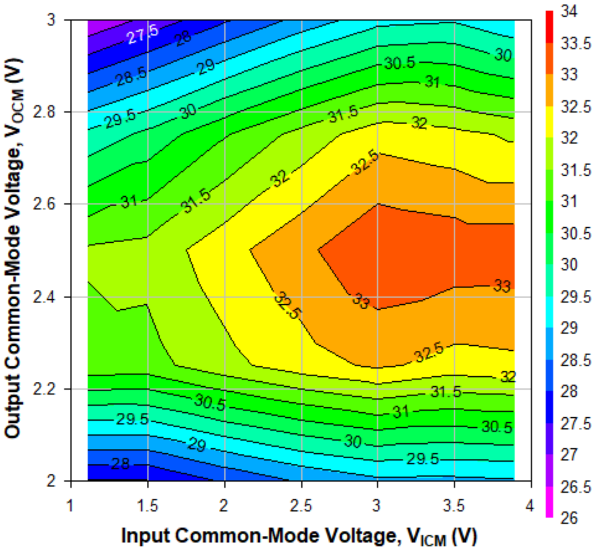
At the amplifier output, a 3dB pad with a 100Ω differential impedance is used to match to the antialiasing filter with a 100Ω differential input impedance. The filter output is connected to ADC with appropriate matching. Figure 8-9 only shows the I-channel; the Q-channel has an identical configuration.

8.2.1.3 Application Curves



f = 500MHz, P_O/tone = 1dBm, 2MHz tone spacing, Ch1

Figure 8-11. OIP3 Across Input and Output Common-Mode Voltage



f = 2GHz, P_O/tone = 1dBm, 2MHz tone spacing, Ch1

Figure 8-12. OIP3 Across Input and Output Common-Mode Voltage

8.3 Power Supply Recommendations

8.3.1 Supply Voltages

For the TRF1305x2, short both the VS1+ and VS2+ supply pins together to the same voltage for proper device operation. The typical differential supply between VS+ and VS– is 5V. The VS+ and VS– supply pins can be floated with respect to the thermal pad within the specified range listed in the *Absolute Maximum Ratings* and *Recommended Operating Conditions*.

8.3.2 Single-Supply Operation

The VS– pin is connected to ground in the single-supply configuration. Single-supply operation is most convenient in ac-coupled configurations because the dc common-mode voltages of the source at the inputs and the driven circuit at the outputs are inherently decoupled.

8.3.3 Split-Supply Operation

In split-supply configuration, choose the V_{S+} and $V_{S–}$ voltages to be within the ranges specified in the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. The TRF1305x2 allows choosing negative voltages for the $V_{S–}$ supply, thereby allowing the flexibility to choose input and output common-mode voltages according to the input network and output network requirements.

8.3.4 Supply Decoupling

The VS+ and VS– supply pins are decoupled individually to ground using external capacitors. For the TRF1305x2, VS+ decoupling can be split between VS1+ to GND and VS2+ to GND separately for ease of board layout. Place the decoupling capacitors close to the device supply pins.

8.4 Layout

8.4.1 Layout Guidelines

The TRF1305x2 devices are wideband closed-loop feedback amplifiers. When designing with wideband RF amplifiers that have high gain, take certain board layout precautions to maintain stability and optimized performance. Use a multilayer board to maintain signal integrity, power integrity, and thermal performance.

Route the RF input and output lines as grounded coplanar waveguide (GCPW) lines. Ground pins are the reference for the RF signals. Maintain that the second layer of the PCB has a continuous ground layer without any ground cutouts in the vicinity of the amplifier. To minimize phase imbalance, match the length of the output differential lines of both channels. Length matching the input traces is also important, especially if the input configuration is differential. Use small-footprint, passive components wherever possible.

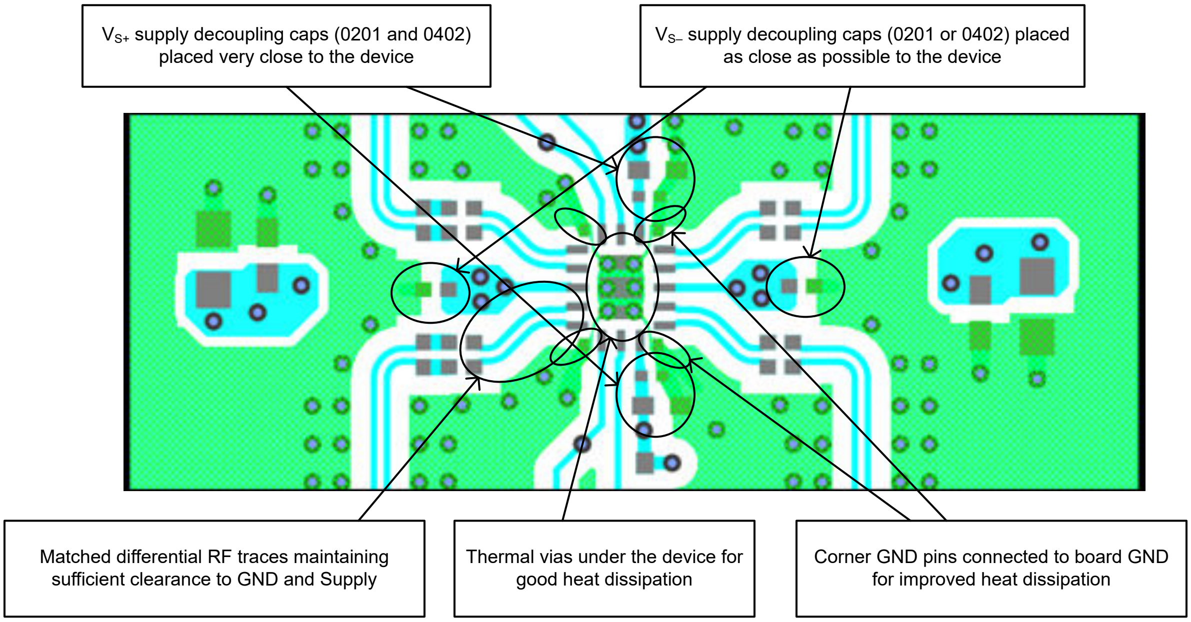
For good heat dissipation, connect the device thermal pad to the board ground planes using thermal vias under the device. For improved heat dissipation, connect the device thermal pad to the top layer ground plane of the board.

8.4.1.1 Thermal Considerations

The TRF1305x2 are packaged in a WQFN-FCRLF package that has excellent thermal properties. Connect the thermal pads underneath the devices to the thermally dissipative ground plane on the board. For good thermal design, use thermal vias to connect the thermal pad plane on the top layer of the PCB to the ground planes in the inner layers.

8.4.2 Layout Example

Figure 8-13 shows an example layout for the TRF1305x2 with a differential input configuration. Key areas are highlighted in the figure.



V_{S+} supply decoupling caps (0201 and 0402) placed very close to the device

V_{S-} supply decoupling caps (0201 or 0402) placed as close as possible to the device

Matched differential RF traces maintaining sufficient clearance to GND and Supply

Thermal vias under the device for good heat dissipation

Corner GND pins connected to board GND for improved heat dissipation

Figure 8-13. Layout Example: TRF1305x2 With Differential Input

The TRF1305A2 can be evaluated using EVM boards that can be ordered from the TRF1305A2 product folder. For more information about the evaluation board construction and test setup, see the *TRF1305x2 EVM User's Guide*.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TRF1305x2-D2D EVM User's Guide*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

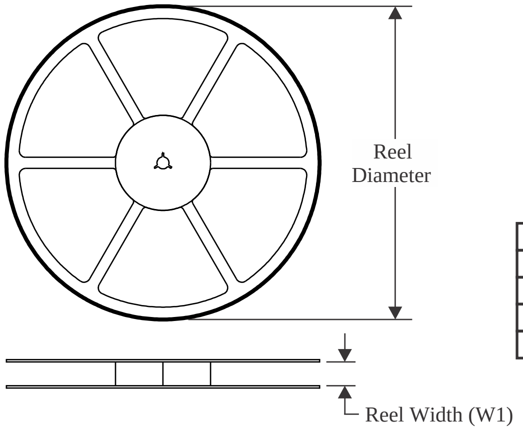
DATE	REVISION	NOTES
October 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

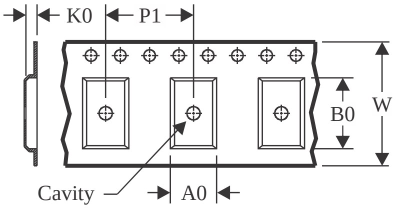
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

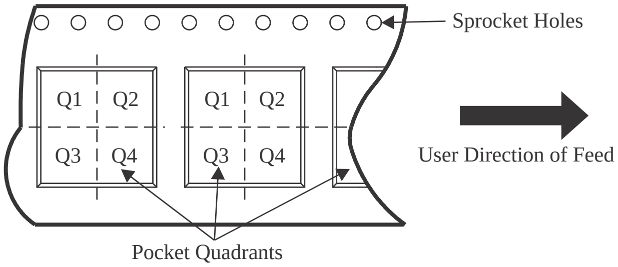


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

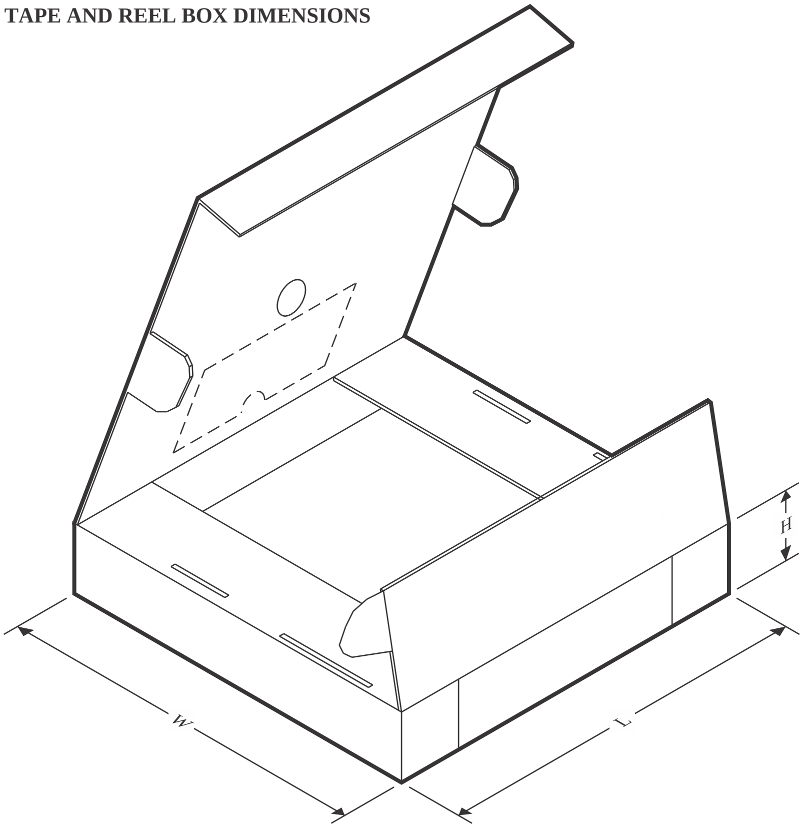
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

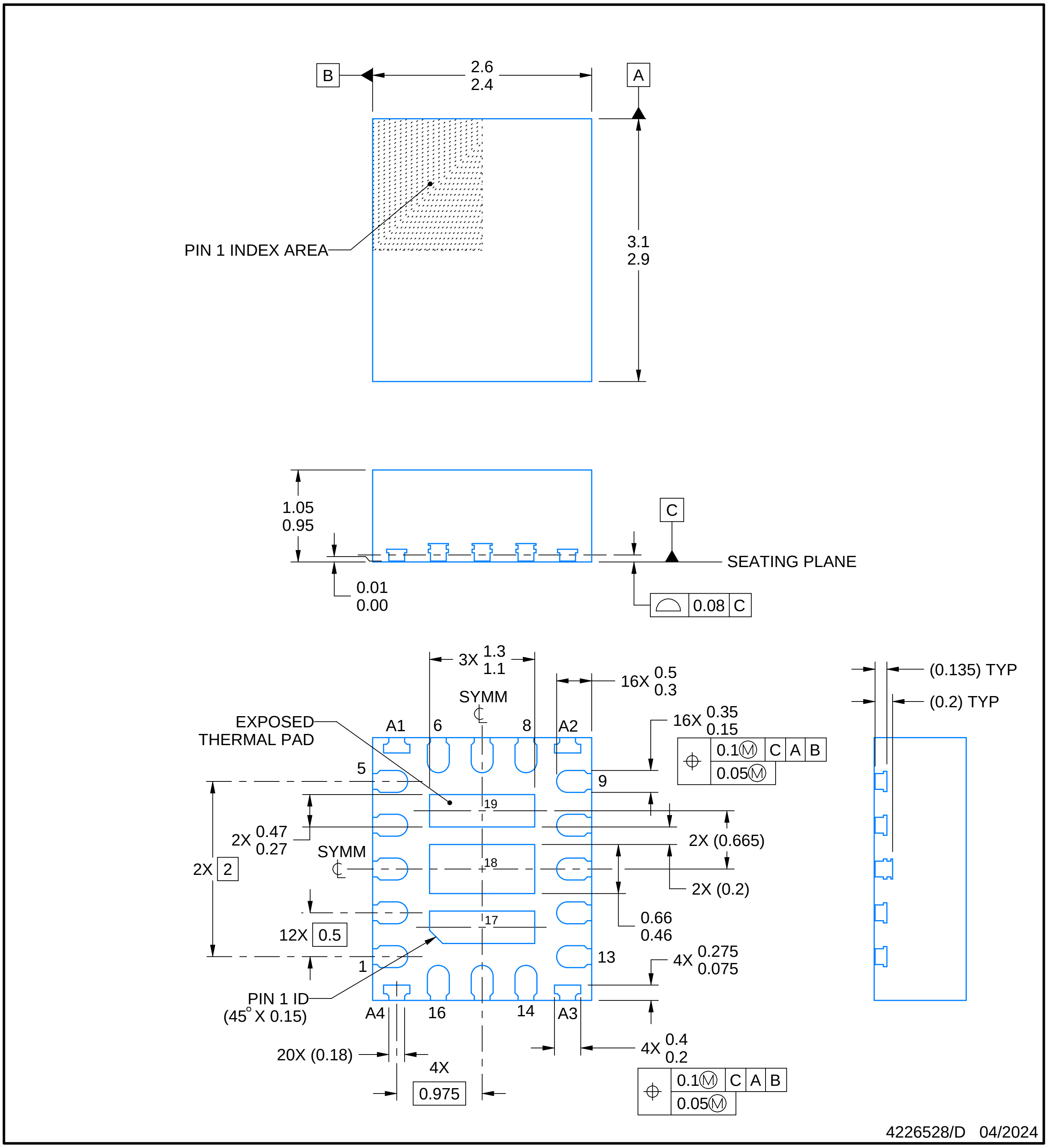
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1305A2RYPR	VQFN-FCRLF	RYP	16	2000	330.0	12.4	2.8	3.3	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



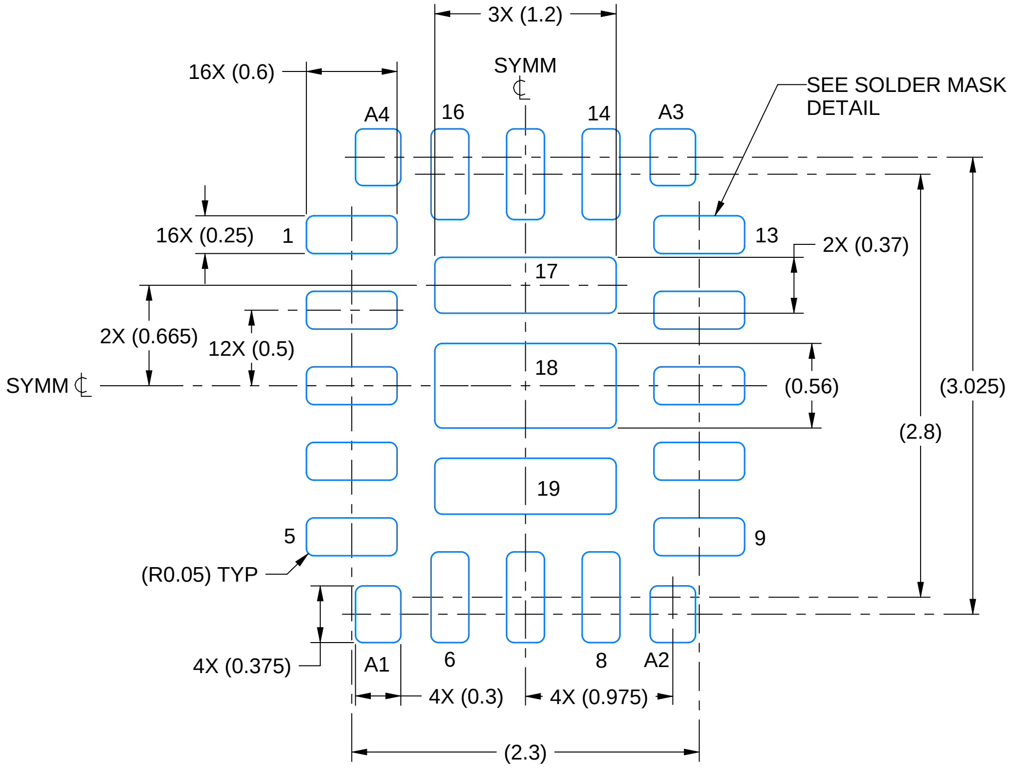
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1305A2RYPR	VQFN-FCRLF	RYP	16	2000	338.0	355.0	50.0

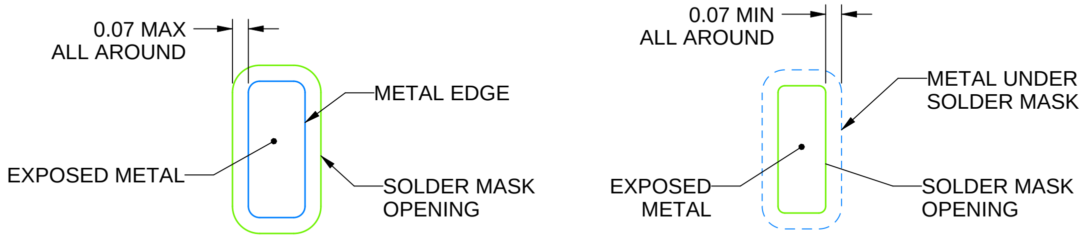


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



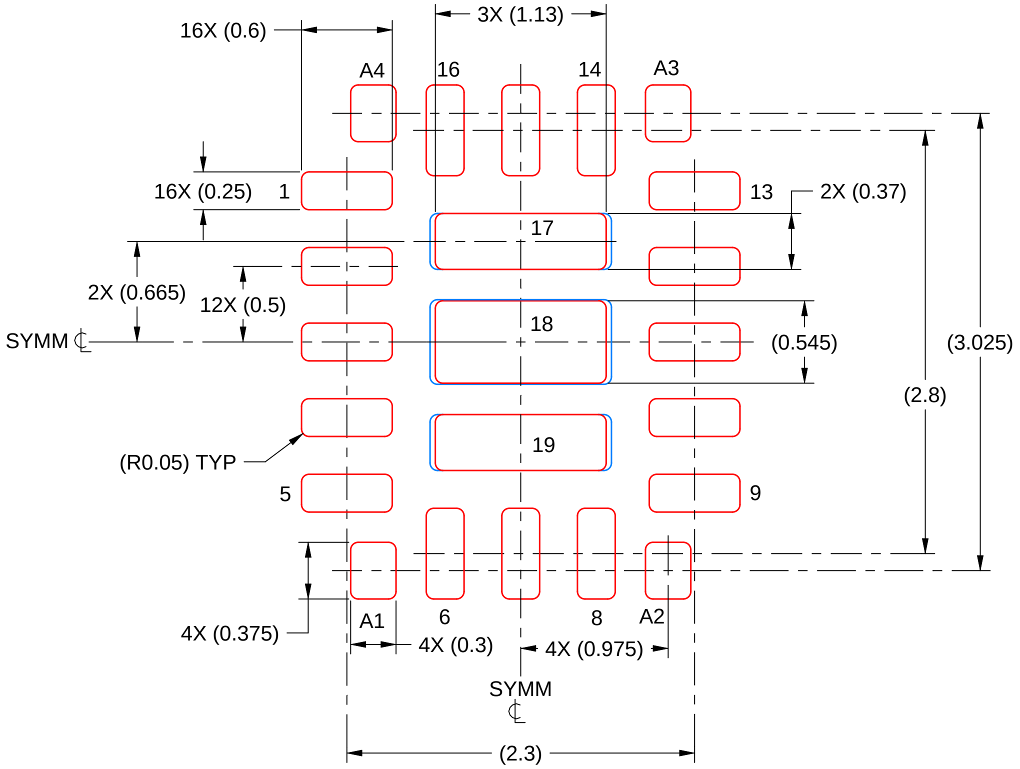
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 17 & 19: 94%
PAD 18: 92%

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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