TPS7A14C 1A, Low V_{IN}, Low V_{OUT}, Fast-Settling, Low-Dropout Regulator

1 Features

- Ultra-low input voltage range: 0.7V to 2.2V
- High efficiency:
  - Dropout voltage at 1A: 80mV (max)
- Excellent load transient response
- Accuracy over load, line, and temperature:
  - +10mV (max) to −23mV (min)
- High PSRR:
  - 60dB at 1kHz (V_{OUT} = 0.8V, I_{OUT} = 500mA)
- Available in fixed-output voltages:
  - 0.5V to 2.0V (in 25mV steps)
- V_{BIAS} range: 2.2V to 5.5V
- Package:
  - 6-pin WCSP: 1.16mm × 0.71mm
- Active output discharge

2 Applications

- Camera modules
- Wireless headphones and earbuds
- Smart watch and fitness trackers
- Smart phones and tablets
- Portable medical devices
- Solid state drives (SSDs)

3 Description

The TPS7A14C is a small, ultra low-dropout regulator (LDO) with excellent transient response. This device sources 1A with outstanding ac performance (load and line transient responses). The input voltage range is 0.7V to 2.2V, and the output range is 0.5V to 2.0V with excellent accuracy over load, line, and temperature.

The primary power path is through the IN pin, which is connected to a power supply as low as 50mV above the output voltage. All electrical characteristics are specified for input voltages 100mV greater than the output voltage, thereby yielding high practical efficiency. This regulator supports very low input voltages by using a higher, externally supplied V_{BIAS} rail that powers the internal circuitry of the LDO.

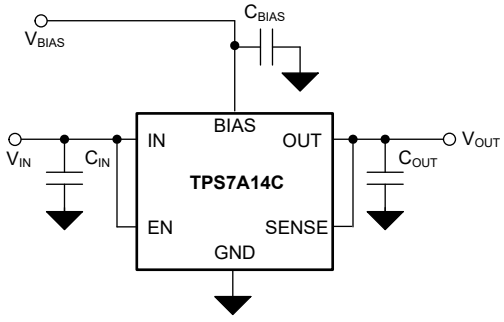
The TPS7A14C is equipped with an active pulldown circuit to quickly discharge the output when disabled, and provides a known start-up state.

The TPS7A14C is available in an ultra-small 0.71mm × 1.16mm, 6-bump WCSP package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS7A14C	YBK (WCSP, 6)	1.16mm × 0.71mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

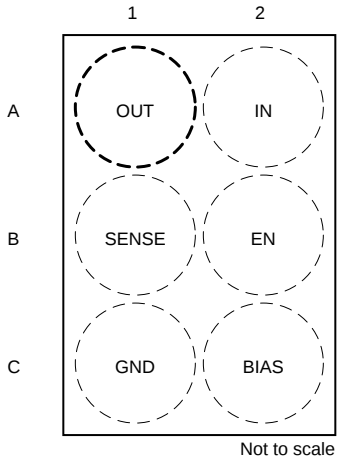


Figure 4-1. YBK Package, 6-Pin WCSP (Top View)

Table 4-1. Pin Functions: YBK Package

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	OUT	Output	Regulated output pin. Place the output capacitor as close to OUT as possible.
A2	IN	Input	Input pin. Place the input capacitor as close to IN as possible.
B1	SENSE	Input	SENSE input. This pin is a feedback input to the regulator for SENSE connections. Connecting SENSE to the load helps eliminate voltage errors resulting from trace resistance between OUT and the load.
B2	EN	Input	Enable pin. Driving this pin to logic high enables the LDO. Driving this pin to logic low disables the LDO. If enable functionality is not required, connect EN to IN or BIAS.
C1	GND	—	Ground pin. Connect this pin to ground.
C2	BIAS	Input	BIAS pin. This pin enables operation in low-input voltage, low-output voltage (LILO) conditions. For best performance, use a ceramic capacitor from BIAS to ground. Place the bias capacitor as close to BIAS as possible.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	2.4	V
	Enable, V_{EN}	–0.3	6.0	
	Bias, V_{BIAS}	–0.3	6.0	
	Sense, V_{SENSE}	–0.3	V_{IN} + 0.3 (2)	
	Output, V_{OUT}	–0.3	V_{IN} + 0.3 (2)	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is 2.4V or (V_{IN} + 0.3V), whichever is less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.7		2.2	V
V_{BIAS}	Bias voltage	Greater of 2.2 or $V_{OUT(NOM)}$ + 1.4		5.5	V
V_{OUT}	Output voltage	0.5		2.0	V
I_{OUT}	Peak output current	0		1	A
C_{IN}	Input capacitance (2)	1	4.7		µF
C_{BIAS}	Bias capacitance (3)	0.1	0.47		µF
C_{OUT}	Output capacitance(4)	4.7		10	µF
ESL	Trace inductance between OUT and C_{OUT}			1.5	nH
ESR	Output capacitor ESR + trace ESR	11		50	mΩ
T_J	Operating junction temperature	–40		125	℃

(1) All voltages are with respect to GND.
(2) An input capacitor is required to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients. A larger input capacitor is sometimes required depending on the source impedance and system requirements.
(3) A BIAS input capacitor is not required for LDO stability. However, a capacitor with a derated value of at least 0.1µF is recommended to maintain transient, PSRR, and noise performance.
(4) This value assumes that the total ESR (the sum of the output capacitor ESR and the trace resistance between OUT and the output capacitor) is equal to or greater than 11mΩ. Larger ESR (up to the maximum ESR value specified in this table) allows smaller output capacitance. For best transient and settling performance, the product of the total ESR in mΩ and the effective output capacitance in µF needs to be at least 51.

5.4 Thermal Information

THERMAL METRIC(1)		TPS7A14C DSBGA 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.1V, V_{BIAS} = greater of 2.2V or $V_{OUT(NOM)}$ + 1.4V, I_{OUT} = 1mA, V_{EN} = 1.0V, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{BIAS} = 0.1µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Accuracy over temperature	Greater of 2.2V or ($V_{OUT(NOM)}$ + 1.4V) ≤ V_{BIAS} ≤ 5.5V, 1mA ≤ I_{OUT} ≤ 1A	T_J = –40°C to +125°C	–23		10	mV
V_{OUT}	Accuracy over temperature	Greater of 2.2V or ($V_{OUT(NOM)}$ + 1.4V) ≤ V_{BIAS} ≤ 5.5V, 1mA ≤ I_{OUT} ≤ 1A	T_J = –40°C to +85°C	–19		8	mV
ΔV_{OUT} / ΔV_{IN}	V_{IN} line regulation	$V_{OUT(NOM)}$ + 0.1V ≤ V_{IN} ≤ 2.2V		–2.5		2.5	mV
ΔV_{OUT} / ΔV_{BIAS}	V_{BIAS} line regulation	$V_{OUT(NOM)}$ + 1.4V ≤ V_{BIAS} ≤ 5.5V		–2.5	±0.15	2.5	mV
ΔV_{OUT} / ΔI_{OUT}	Load regulation	1mA ≤ I_{OUT} ≤ 1A			13		mV
$I_{Q(BIAS)}$	Bias pin current	I_{OUT} = 0mA				68	µA
		I_{OUT} = 0mA, T_J = –40°C to +85°C			40	57	
		I_{OUT} = 1A				17	mA
		I_{OUT} = 1A, T_J = –40°C to +85°C			10	15	
$I_{Q(IN)}$	Input pin current(1)	I_{OUT} = 0mA				118	µA
		I_{OUT} = 0mA, T_J = –40°C to +85°C				80	
I_{GND}	Ground pin current	I_{OUT} = 1A				800	µA
		I_{OUT} = 1A, T_J = –40°C to +85°C			520	750	
$I_{SHDN(BIAS)}$	V_{BIAS} shutdown current	V_{IN} = 2.2V, V_{BIAS} = 5.5V, V_{EN} ≤ 0.2V			0.36	9	µA
		V_{IN} = 2.2V, V_{BIAS} = 5.5V, V_{EN} ≤ 0.2V, T_J = –40°C to +85°C			0.36	3.8	
$I_{SHDN(IN)}$	V_{IN} shutdown current	V_{IN} = 1.8V, V_{BIAS} = 5.5V, V_{EN} ≤ 0.2V			0.09	32	µA
		V_{IN} = 1.8V, V_{BIAS} = 5.5V, V_{EN} ≤ 0.2V, T_J = –40°C to +85°C			0.09	9.2	
I_{CL}	Output current limit	V_{OUT} = 0.95 × $V_{OUT(NOM)}$		1.035	1.5	2.45	A
I_{SC}	Short circuit current limit	V_{OUT} = 0V			490		mA
$V_{DO(IN)}$	V_{IN} dropout voltage(2)	V_{IN} = 0.95 x $V_{OUT(NOM)}$, I_{OUT} = 1A	T_J = –40°C to + 125°C		30	80	mV
$V_{DO(BIAS)}$	V_{BIAS} dropout voltage(2)	V_{BIAS} = greater of 2.2V or $V_{OUT(NOM)}$ + 0.6V. I_{OUT} = 1 A			0.76	1.1	V

5.5 Electrical Characteristics (continued)

specified at T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.1V, V_{BIAS} = greater of 2.2V or $V_{OUT(NOM)}$ + 1.4V, I_{OUT} = 1mA, V_{EN} = 1.0V, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{BIAS} = 0.1µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} PSRR	V_{IN} power-supply rejection ratio	f = 100Hz, V_{IN} = 1.05V, V_{OUT} = 0.8V, C_{OUT} = 9µF	I_{OUT} = 3mA		90		dB
			I_{OUT} = 500mA		68		
			I_{OUT} = 1A		64		
		f = 1kHz,V_{IN} = 1.05V, V_{OUT} = 0.8V, C_{OUT} = 9µF	I_{OUT} = 3mA		90		
			I_{OUT} = 500mA		60		
			I_{OUT} = 1A		57		
		f = 10kHz, V_{IN} = 1.05V, V_{OUT} = 0.8V, C_{OUT} = 9µF	I_{OUT} = 3mA		87		
			I_{OUT} = 500mA		60		
			I_{OUT} = 1A		57		
		f = 100kHz, V_{IN} = 1.05V, V_{OUT} = 0.8V, C_{OUT} = 9µF	I_{OUT} = 3mA		80		
			I_{OUT} = 500mA		62		
			I_{OUT} = 1A		58		
		f = 1MHz, V_{IN} = 1.05V, V_{OUT} = 0.8V, C_{OUT} = 9µF	I_{OUT} = 3mA		75		
			I_{OUT} = 500mA		57		
			I_{OUT} = 1A		57		
V_{BIAS} PSRR	V_{BIAS} power-supply rejection ratio	f = 1kHz	I_{OUT} = 500mA		65		dB
		f = 100kHz			50		
		f = 1MHz			25		
V_n	Output voltage noise	Bandwidth = 10Hz to 100kHz, V_{OUT} = 0.8V, I_{OUT} = 3mA			6		μV_{RMS}
		Bandwidth = 10Hz to 100kHz, V_{OUT} = 0.8V, I_{OUT} = 500mA			5.9		
		Bandwidth = 10Hz to 100kHz, V_{OUT} = 0.8V, I_{OUT} = 1A			5.9		
$V_{UVLO(BIAS)}$	Bias supply UVLO	V_{BIAS} rising		1.15	1.42	1.7	V
		V_{BIAS} falling		1.0	1.3	1.63	
$V_{UVLO\_HYST(BIAS)}$	Bias supply UVLO hysteresis	V_{BIAS} hysteresis			45		mV
$V_{UVLO(IN)}$	Input supply UVLO	V_{IN} rising		584	603	623	mV
		V_{IN} falling		530	552	566	
$V_{UVLO\_HYST(IN)}$	Input supply hysteresis	V_{IN} hysteresis			52		mV
t_{STR}	Start-up time(3)				260		µs
$V_{EN(HI)}$	EN pin logic high voltage(4)			0.6		6	V
$V_{EN(LOW)}$	EN pin logic low voltage(4)			0		0.25	V
I_{EN}	EN pin current	EN = 5.5V		-25	10	25	nA
		EN = 5.5V, T_J = –40°C to +85°C		-20	10	20	
$R_{PULLDOWN}$	Pulldown resistor	V_{IN} = 0.9V, $V_{OUT(nom)}$ = 0.8V, V_{BIAS} = 3.3V, V_{EN} = 0V, P version only			36		Ω
T_{SD}	Thermal shutdown temperature	Shutdown, temperature rising			165		°C
		Reset, temperature falling			140		

(1) This is the current flowing from V_{IN} to GND.
(2) Dropout is not measured for V_{OUT} < 0.6V. V_{BIAS} dropout applies only for V_{BIAS} of 2.2V or greater.
(3) Startup time = time from EN assertion to 0.95 × $V_{OUT(NOM)}$.
(4) An input voltage within the minimum to maximum range is interpreted as the correct logic level.

5.6 Typical Characteristics

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.8V, V_{IN} = $V_{OUT(NOM)}$ + 0.1V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4V, I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, and C_{BIAS} = 0.47µF (unless otherwise noted)

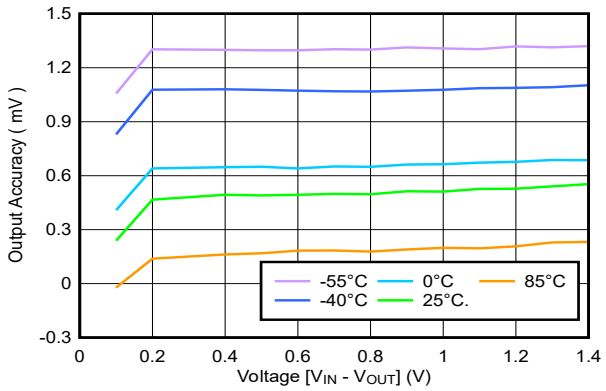


Figure 5-1. Output Voltage Accuracy vs V_{IN}

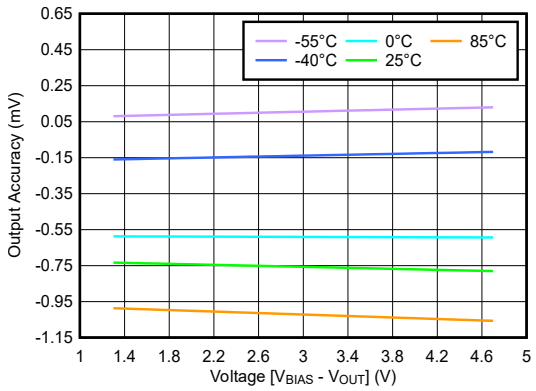


Figure 5-2. Output Voltage Accuracy vs V_{BIAS}

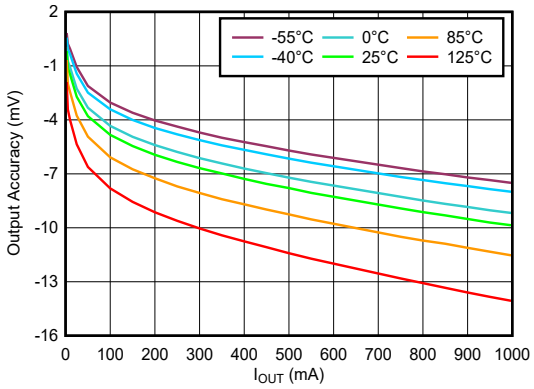


Figure 5-3. Output Voltage Accuracy vs I_{OUT}

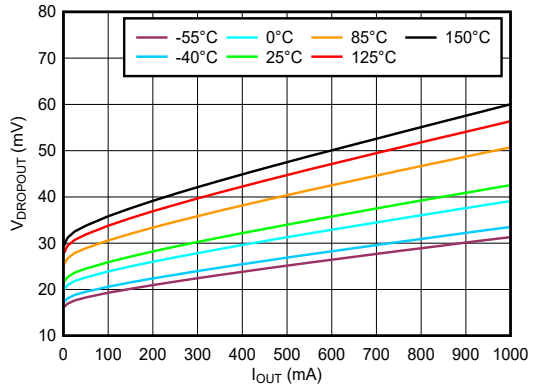


Figure 5-4. V_{IN} Dropout Voltage vs I_{OUT}

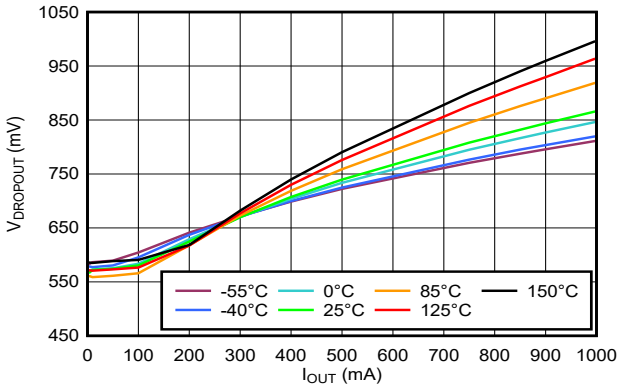


Figure 5-5. V_{BIAS} Dropout Voltage vs I_{OUT}

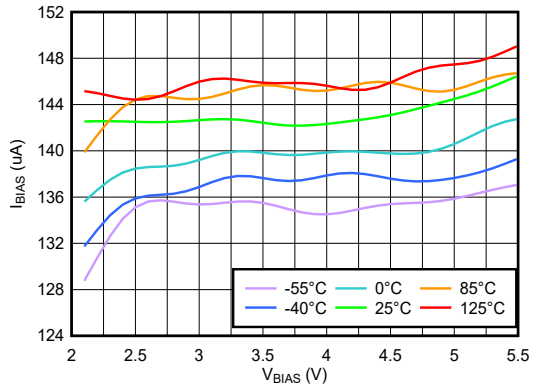
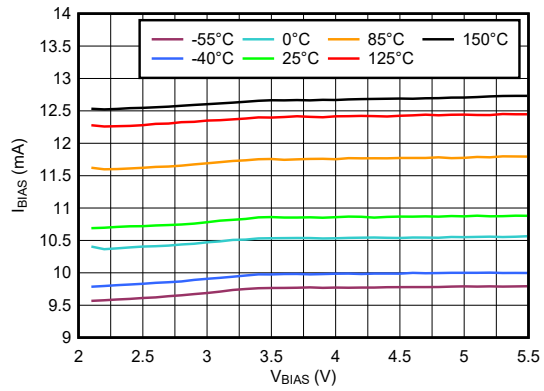


Figure 5-6. V_{BIAS} Input Current vs V_{BIAS}

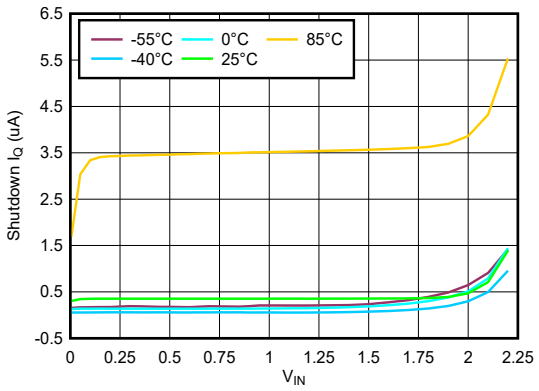
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.8V, V_{IN} = $V_{OUT(NOM)}$ + 0.1V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4V, I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, and C_{BIAS} = 0.47µF (unless otherwise noted)



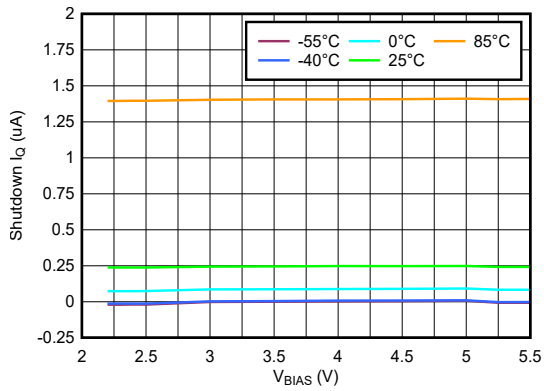
I_{OUT} = 1A

Figure 5-7. V_{BIAS} Input Current vs V_{BIAS}



I_{OUT} = 0mA

Figure 5-8. V_{IN} Shutdown I_Q vs V_{IN}



I_{OUT} = 0A, V_{IN} = 1V

Figure 5-9. V_{BIAS} Shutdown I_Q vs V_{BIAS}

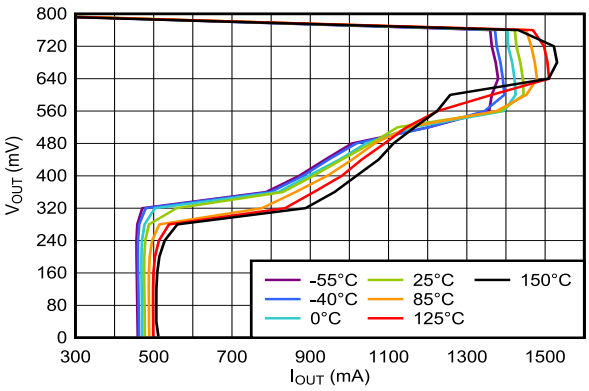


Figure 5-10. V_{OUT} Foldback Current Limit vs Output Current

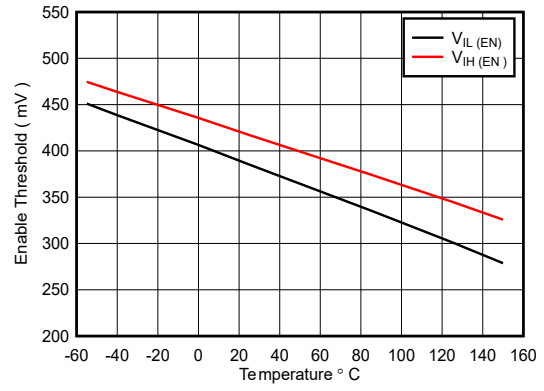


Figure 5-11. Enable Threshold vs Temperature

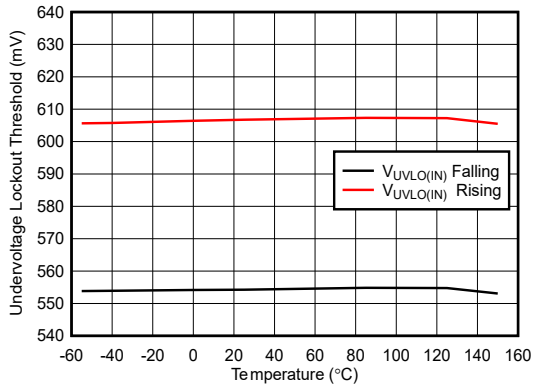


Figure 5-12. V_{IN} UVLO vs Temperature

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.8V, V_{IN} = $V_{OUT(NOM)}$ + 0.1V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4V, I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, and C_{BIAS} = 0.47µF (unless otherwise noted)

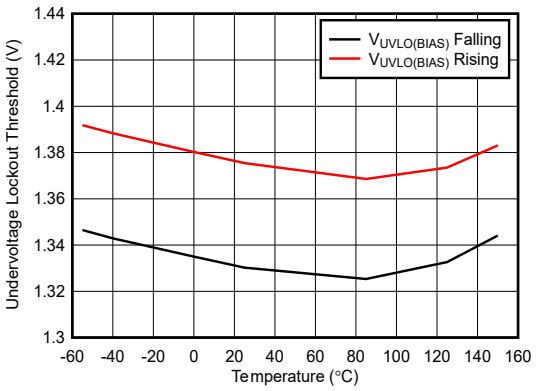
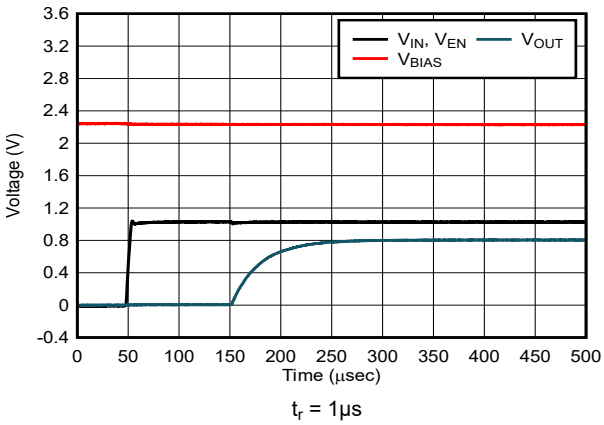
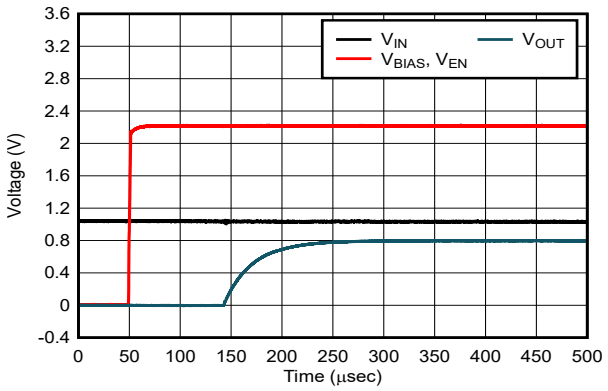


Figure 5-13. V_{BIAS} UVLO vs Temperature



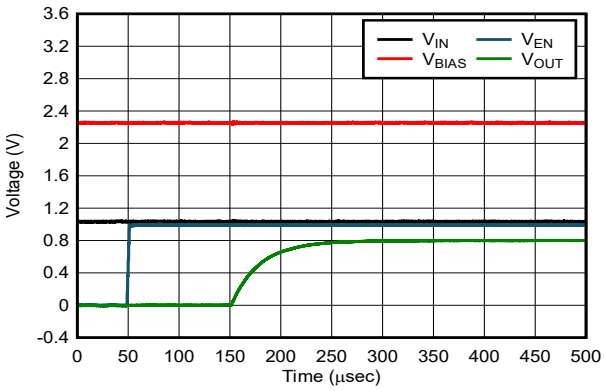
t_r = 1µs

Figure 5-14. Start-Up With V_{BIAS} Before V_{IN}



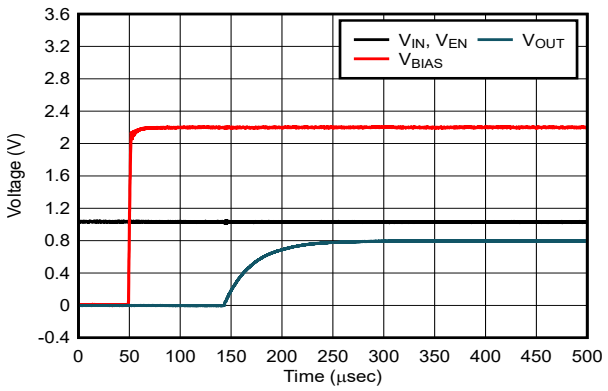
t_r = 1µs

Figure 5-15. Start-Up With V_{IN} Before V_{BIAS} and V_{EN}



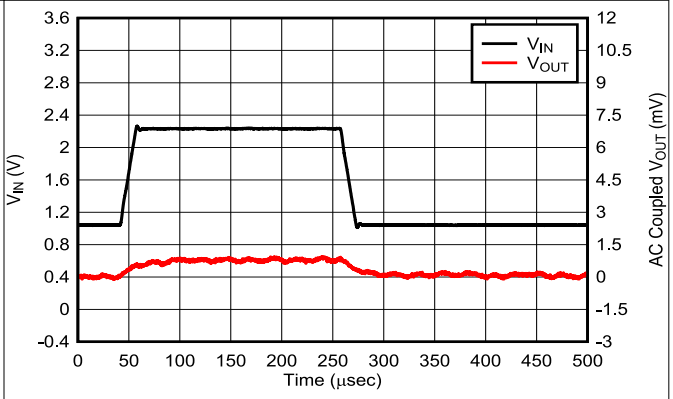
t_r = 1µs

Figure 5-16. Start-Up With V_{IN} and V_{BIAS} Before V_{EN}



t_r = 1µs

Figure 5-17. Start-Up With V_{IN} and V_{EN} Before V_{BIAS}

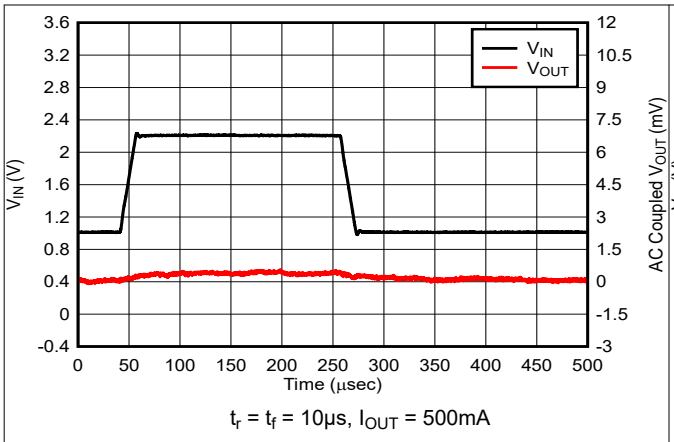


t_r = t_f = 10µs, I_{OUT} = 1mA

Figure 5-18. Line Transient From 1V to 2.2V

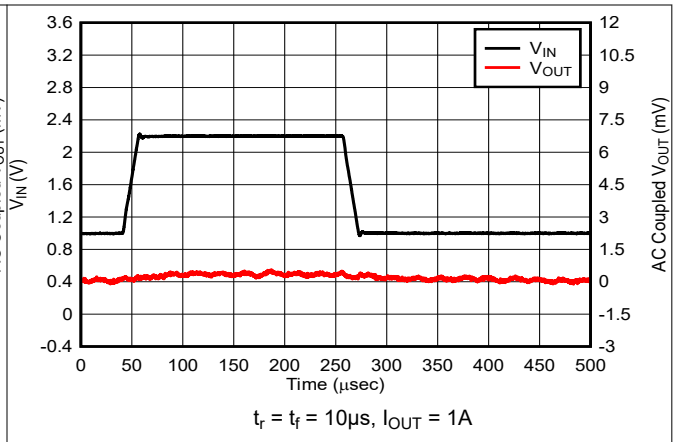
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.8V, V_{IN} = $V_{OUT(NOM)}$ + 0.1V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4V, I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, and C_{BIAS} = 0.47µF (unless otherwise noted)



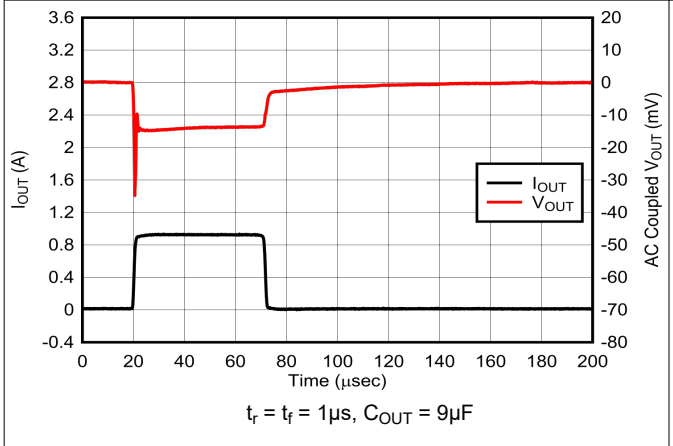
t_r = t_f = 10µs, I_{OUT} = 500mA

Figure 5-19. Line Transient From 1V to 2.2V



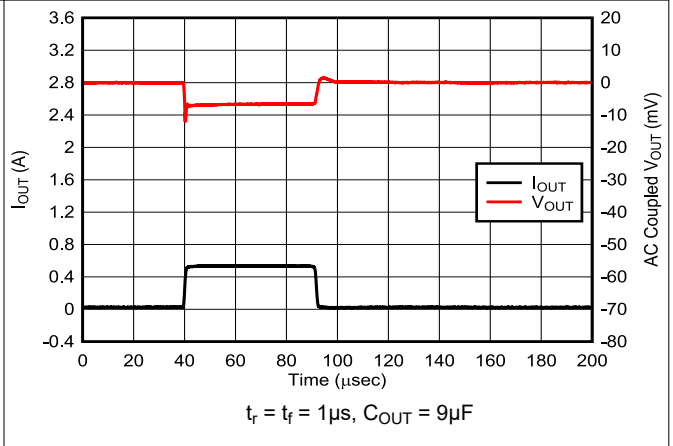
t_r = t_f = 10µs, I_{OUT} = 1A

Figure 5-20. Line Transient From 1V to 2.2V



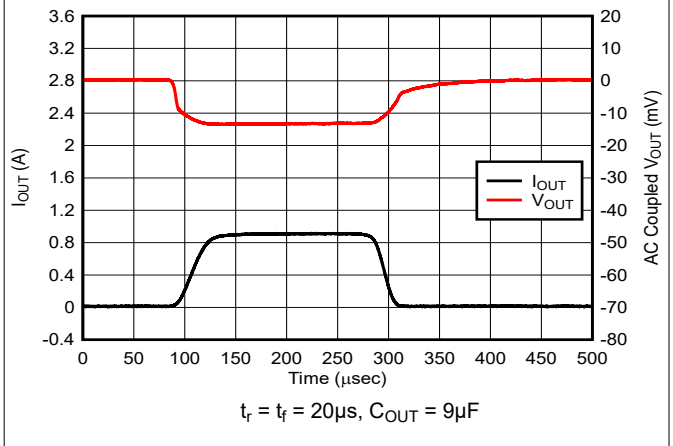
t_r = t_f = 1µs, C_{OUT} = 9µF

Figure 5-21. Load Transient From 100µA to 1A



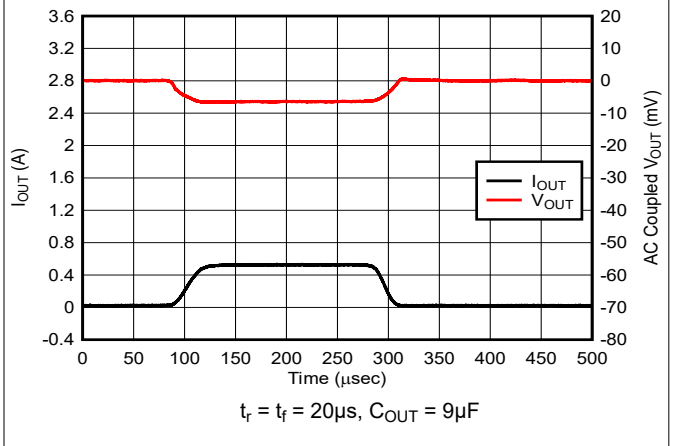
t_r = t_f = 1µs, C_{OUT} = 9µF

Figure 5-22. Load Transient From 10mA to 500mA



t_r = t_f = 20µs, C_{OUT} = 9µF

Figure 5-23. Load Transient From 100µA to 1A

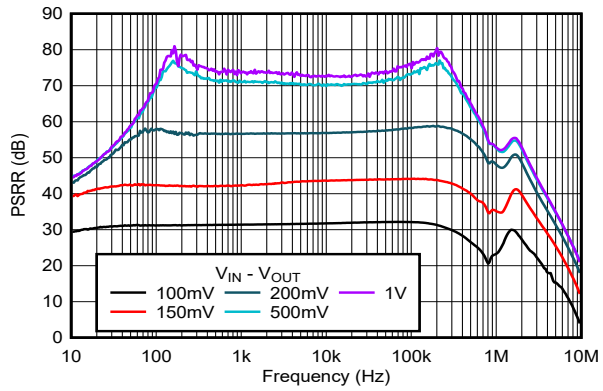


t_r = t_f = 20µs, C_{OUT} = 9µF

Figure 5-24. Load Transient From 10mA to 500A

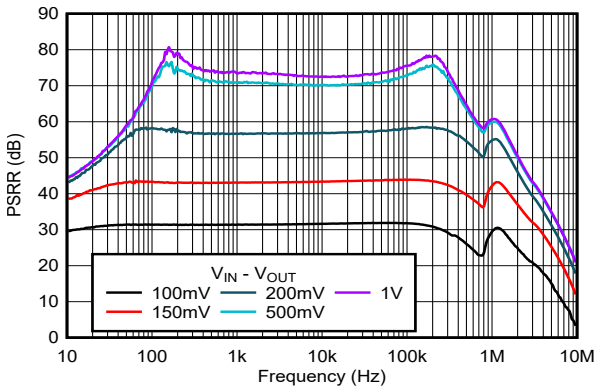
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, $V_{OUT(NOM)}$ = 0.8V, V_{IN} = $V_{OUT(NOM)}$ + 0.1V, V_{BIAS} = $V_{OUT(NOM)}$ + 1.4V, I_{OUT} = 1mA, V_{EN} = V_{IN}, C_{IN} = 4.7µF, C_{OUT} = 4.7µF, and C_{BIAS} = 0.47µF (unless otherwise noted)



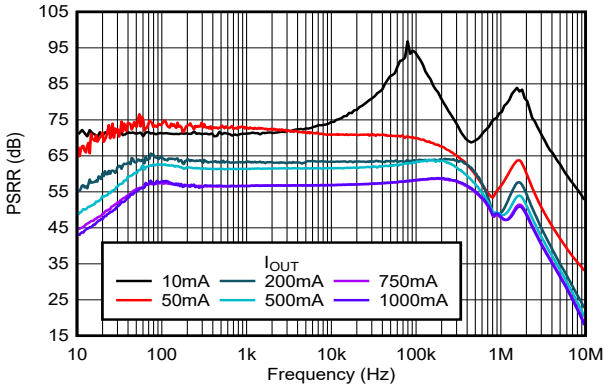
C_{OUT} = 4.7µF, I_{OUT} = 1A

Figure 5-25. PSRR vs Frequency and V_{IN} – V_{OUT}



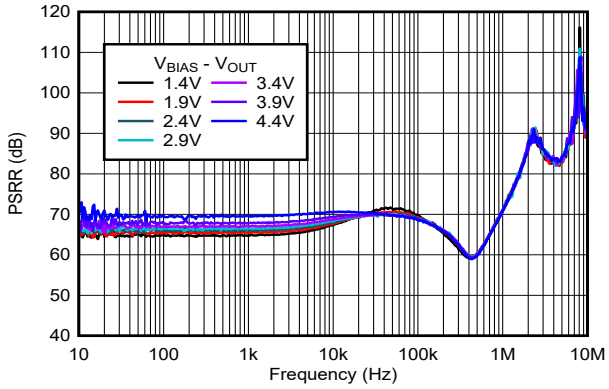
C_{OUT} = 9µF, I_{OUT} = 1A

Figure 5-26. PSRR vs Frequency and V_{IN} - V_{OUT}



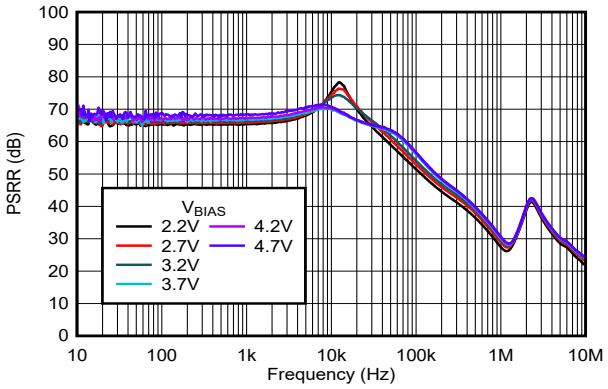
C_{OUT} = 4.7µF, V_{OUT} = 0.8V, V_{IN} = 1V

Figure 5-27. PSRR vs Frequency and I_{OUT}



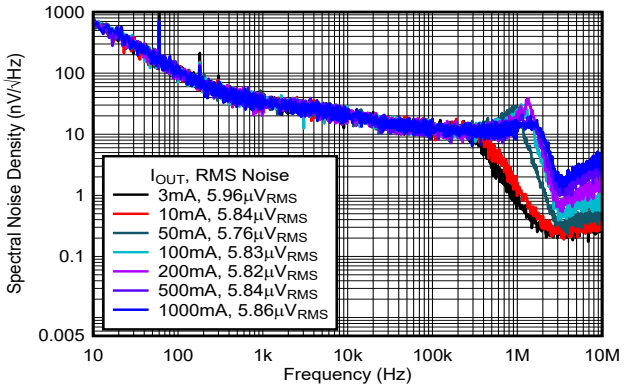
C_{BIAS} = 0µF, C_{OUT} = 4.7µF, I_{OUT} = 1mA

Figure 5-28. PSRR vs Frequency and V_{BIAS} – V_{OUT}



C_{BIAS} = 0µF, C_{OUT} = 4.7µF, I_{OUT} = 500mA

Figure 5-29. PSRR vs Frequency and V_{BIAS} – V_{OUT}



V_{OUT} = 0.8V

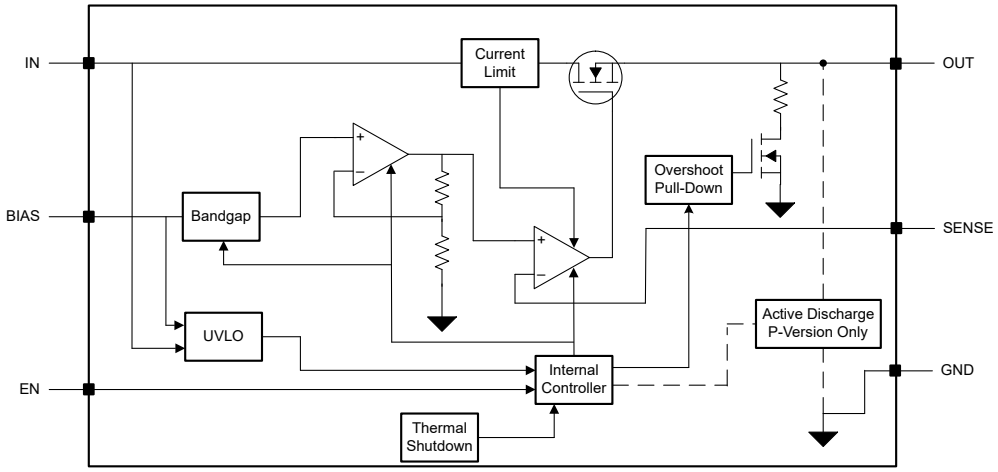
Figure 5-30. Output Noise vs Frequency and I_{OUT}

6 Detailed Description

6.1 Overview

The TPS7A14C is a low-input, ultra-low dropout, low-quiescent-current linear regulator optimized for excellent transient performance. The low operating V_{IN} – V_{OUT}, combined with the BIAS pin, dramatically improves the efficiency of low-voltage output applications. The device improves efficiency by powering the voltage reference and control circuitry and using a pre-regulated, low-voltage input supply (IN) for the main power path. This low-dropout regulator (LDO) offers foldback current limit, shutdown, thermal protection, and an optional active discharge.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Excellent Transient Response

The TPS7A14C responds quickly to a change on the input supply (line transient) or the output current (load transient). This quick response is made possible by the LDO's high input impedance and low output impedance across frequency. This same capability also means that this LDO has a high power-supply rejection ratio (PSRR).

The choice of external component values optimizes the transient response. See the *Input, Output, and Bias Capacitor Requirements* section for proper capacitor selection.

6.3.2 Global Undervoltage Lockout (UVLO)

The TPS7A14C uses two undervoltage lockout circuits: one on the BIAS pin and one on the IN pin. These circuits prevent the device from turning on before both V_{BIAS} and V_{IN} rise above the lockout voltages. As shown in Figure 6-1, the two UVLO signals are connected internally through an AND gate. This gate turns off the device when the voltage on either input is below the respective UVLO thresholds.

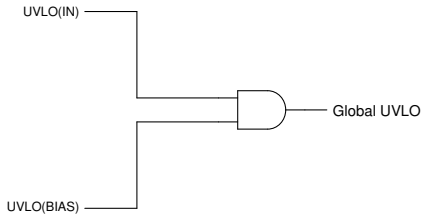


Figure 6-1. Global UVLO Circuit

6.3.3 Enable Input

The enable input (EN) is active high. Applying a voltage greater than $V_{EN(HI)}$ to EN enables the regulator output voltage, and applying a voltage less than $V_{EN(LOW)}$ to EN disables the regulator output. If independent control of the output voltage is not needed, connect EN to either IN or BIAS.

6.3.4 Internal Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ is approximately 60% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-2 shows a diagram of the foldback current limit.

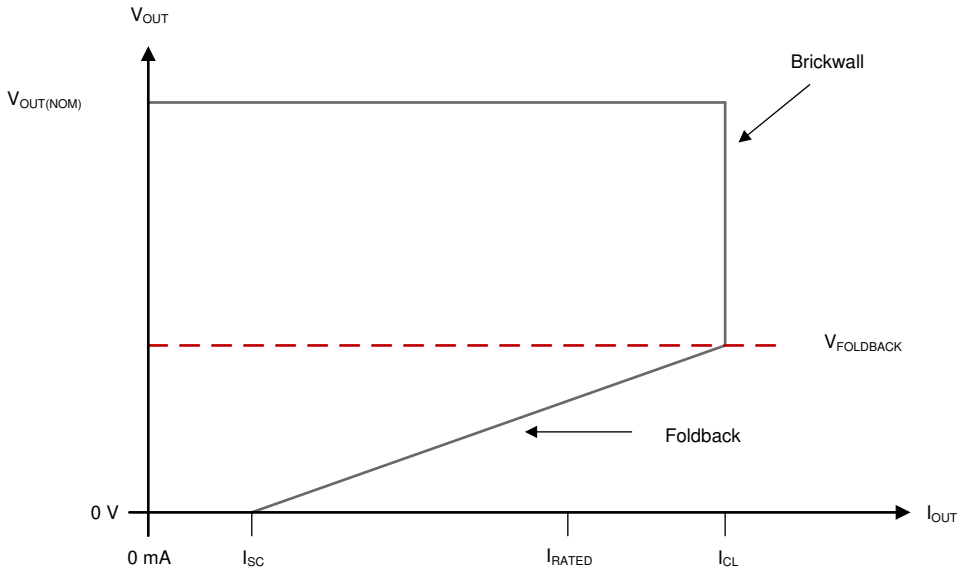


Figure 6-2. Foldback Current Limit

6.3.5 Active Discharge

The active discharge function uses an internal MOSFET that connects a resistor ($R_{PULLDOWN}$) to ground. This function is used when the LDO is disabled to actively discharge the output voltage. The active discharge circuit is activated by driving EN to logic low to disable the device. This circuit is also activated when the voltage at IN or BIAS is below the UVLO threshold or when the regulator is in thermal shutdown.

The discharge time after disabling the device depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the pulldown resistor.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed. Reverse current potentially flows from the output to the input, causing damage to the device. Limit reverse current to no more than 5% of the rated output current for a short period of time.

6.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$. The thermal shutdown circuit resets (turns on) the LDO when the temperature falls to $T_{SD(reset)}$.

The thermal time constant of the semiconductor die is fairly short. The device cycles on and off when thermal shutdown is reached until the power dissipation is reduced. Power dissipation during start up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the regulator into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER				
	V_{IN}	V_{BIAS}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} \geq V_{OUT\ (nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{BIAS} \geq V_{OUT} + V_{DO(BIAS)}$	$V_{EN} \geq V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT\ (nom)} + V_{DO(IN)}$	$V_{BIAS} < V_{OUT} + V_{DO(BIAS)}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$ for shutdown
Disabled mode (any true condition disables the device)	$V_{IN} < V_{UVLO(IN)}$	$V_{BIAS} < V_{BIAS(UVLO)}$	$V_{EN} < V_{IL(EN)}$	—	$T_J \geq T_{SD}$ for shutdown

6.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The bias voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. Similarly, if the bias voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode as well. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state, defined as when the device is in dropout, ($V_{IN} < V_{OUT} + V_{DO}$ or $V_{BIAS} < V_{OUT} + V_{DO}$ directly after being in normal regulation state, but not during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short time when the device pulls the pass transistor back into the linear region.

6.4.3 Disable Mode

Shut down the LDO output by forcing the voltage of the enable pin to less than $V_{IL(EN)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off and internal circuits are shut down. Under this condition, the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Successfully implementing an LDO in a system depends on the system requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

7.1.1 Recommended Capacitor Types

The regulator is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and bias pins. Multilayer ceramic capacitors are the industry standard for use with LDOs, but use good judgment. Ceramic capacitors that use X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance. Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage, ac bias, temperature, humidity, and physical stress. Generally, assume that effective capacitance decreases by as much as 50% to 75% from the nominal capacitor value. Confirm the worst-case capacitance with the capacitor manufacturer based on the expected operating conditions.

7.1.2 Input, Output, and Bias Capacitor Requirements

A minimum input ceramic capacitor is required for stability. A minimum output ceramic capacitor is also required for stability, see the *Recommended Operating Conditions* table for the minimum capacitors values.

The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use a higher value capacitor if large load or line transients with fast rise time are anticipated. Additionally, use a higher-value capacitor if the device is located several inches from the input power source. Dynamic performance of the device is improved with the use of an output capacitor larger than the minimum value specified in the *Recommended Operating Conditions* table.

Although a bias capacitor is not required, good design practice is to connect a 0.1µF or larger ceramic capacitor from BIAS to GND. This capacitor counteracts reactive bias source if the source impedance is not sufficiently low. Place the input, output, and bias capacitors as close as possible to the device to minimize trace parasitics.

Confirm that the BIAS source is not susceptible to fast voltage drops when the LDO load current is near the maximum value. An example voltage drop is a 2V drop in less than 1µs. A fast drop in BIAS voltage can cause the output voltage to fall briefly. If such a condition is expected, use a BIAS capacitor large enough to slow the voltage ramp rate to less than 0.5V/µs. For smaller or slower BIAS transients, verify any output voltage dips are less than 5% of the nominal voltage.

Confirm the output capacitance is within the range listed in the *Recommended Operating Conditions* table for stable operation and fast settling.

7.1.3 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ at the rated output current (I_{RATED}), where the pass transistor is fully on. V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. Dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

Using a bias rail enables the TPS7A14C to achieve a lower dropout voltage between IN and OUT. However, maintain a minimum bias voltage above the nominal programmed output voltage. Figure 5-13 specifies the minimum V_{BIAS} headroom required to maintain output regulation.

7.1.4 Behavior During Transition From Dropout Into Regulation

Some applications can have transients that place this device into dropout, especially when this device can be powered from a battery with relatively high ESR. The load transient saturates the output stage of the error amplifier when the pass transistor is driven fully on, making the pass transistor function like a resistor from V_{IN} to V_{OUT}. The error amplifier response time to this load transient is extended because the error amplifier must first recover from saturation and then must place the pass transistor back into active mode. During this recovery period, V_{OUT} overshoots because the pass transistor is functioning as a resistor from V_{IN} to V_{OUT}.

When V_{IN} ramps up slowly for start up, the slow ramp-up voltage can place the device in dropout. As with many other LDOs, the output can overshoot on recovery from this condition. However, this condition is easily avoided through the use of the enable signal.

If operating under these conditions, apply a higher dc load current or increase the output capacitance to reduce the overshoot. These approaches provide a path to absorb the excess charge.

7.1.5 Device Enable Sequencing Requirement

Any sequencing order of the IN, BIAS, and EN pin voltages is acceptable and does not cause damage to the device. Start up is always monotonic regardless of the sequencing order or the ramp rates of the IN, BIAS, and EN pins. See the *Recommended Operating Conditions* table for proper voltage ranges of the IN, BIAS, and EN pins.

7.1.6 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current while output voltage regulation is maintained. See Figure 5-21 and Figure 5-23 for typical load transient response plots. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions in Figure 7-1 are broken down as described in this section. Regions A, E, and H are where the output voltage is in steady-state operation.

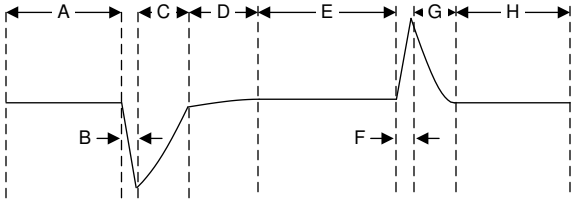


Figure 7-1. Load Transient Waveform

During transitions from a light load to a heavy load, the following behavior can be observed:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the following behavior can be observed:

- The initial voltage rise results from the LDO sourcing a large current, and leads to an increase in the output capacitor charge (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

7.1.7 Undervoltage Lockout Circuit Operation

The V_{IN} UVLO circuit prevents the regulator from operating until the input supply voltage rises above the minimum operational voltage. This circuit also disables the regulator when the input supply collapses. Similarly, the V_{BIAS} UVLO circuit prevents the regulator from operating until the bias supply voltage rises above the minimum operational voltage. This circuit also shuts down the regulator when the bias supply collapses.

Figure 7-2 shows the UVLO circuit response to various input or bias voltage events. The diagram is separated into the following parts:

- Region A: The output remains off while the input or bias voltage is below the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output potentially falls out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls as a result of the load and active discharge circuit. The device is re-enabled when the UVLO rising threshold is reached and a normal start up follows.
- Region F: Normal operation followed by the input or bias falling to the UVLO falling threshold.
- Region G: The device is disabled when the input or bias voltages fall below the UVLO falling threshold to 0V. The output falls as a result of the load and active discharge circuit.

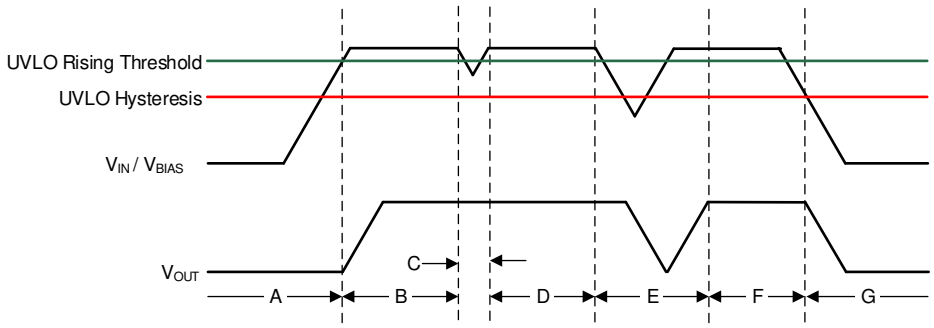


Figure 7-2. Typical V_{IN} or V_{BIAS} UVLO Circuit Operation

7.1.8 Power Dissipation (P_D)

Circuit reliability requires proper consideration of device power dissipation, location of the device on the printed circuit board, and correct sizing of the thermal plane. Verify the PCB area around the regulator is as free as possible of other heat-generating devices that cause added thermal stresses.

The following equation calculates the maximum allowable power dissipation for the device in a given package:

$$P_{D\text{-}MAX} = [(T_J - T_A) / R_{\theta JA}] \quad (2)$$

The following equation represents the actual power being dissipated in the device:

$$P_D = ((I_{GND(IN)} + I_{IN}) \times V_{IN} + I_{GND(BIAS)} \times V_{BIAS}) - (I_{OUT} \times V_{OUT}) \quad (3)$$

If the load current is much greater than $I_{GND(IN)}$ and $I_{GND(BIAS)}$, Equation 3 is simplified as:

$$P_D = (V_{IN} – V_{OUT}) × I_{OUT} \quad (4)$$

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A14C allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path depends on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable junction temperature (T_J) determines the maximum power dissipation for the device. According to Equation 5, maximum power dissipation and T_J are most often related by the $R_{\theta JA}$ of the combined PCB and device package and the T_A. $R_{\theta JA}$ is the junction-to-ambient thermal resistance and T_A is the temperature of the ambient air. The equation is rearranged in Equation 6 for output current.

$$T_J = T_A + (R_{\theta JA} × P_D) \quad (5)$$

$$I_{OUT} = (T_J – T_A) / [R_{\theta JA} × (V_{IN} – V_{OUT})] \quad (6)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Electrical Characteristics* table is determined by the JEDEC standard, PCB, and copper-spreading area. $R_{\theta JA}$ is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is the sum of the YBK package $R_{\theta JC(bot)}$ thermal resistance plus the thermal resistance contribution by the PCB copper. $R_{\theta JC(bot)}$ is the junction-to-case (bottom) thermal parameter.

7.1.9 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics. These thermal metrics estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($Ψ_{JT}$ and $Ψ_{JB}$) are used in accordance with Equation 7 and are given in the *Electrical Characteristics* table.

$$Ψ_{JT} : T_J = T_T + Ψ_{JT} × P_D \text{ and } Ψ_{JB} : T_J = T_B + Ψ_{JB} × P_D \quad (7)$$

where:

- P_D is the power dissipated as explained in Equation 3 and the *Power Dissipation (P_D)* section
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

7.1.10 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is provided in Figure 7-3 and can be separated into the following regions:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} – V_{OUT}$) at a given output current level; see the *Dropout Operation* section for more details.
- The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - Equation 6 provides the shape of the slope. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO, thus when $V_{IN} – V_{OUT}$ increases the output current must decrease.

- The rated input voltage range governs both the minimum and maximum of V_{IN} – V_{OUT}.

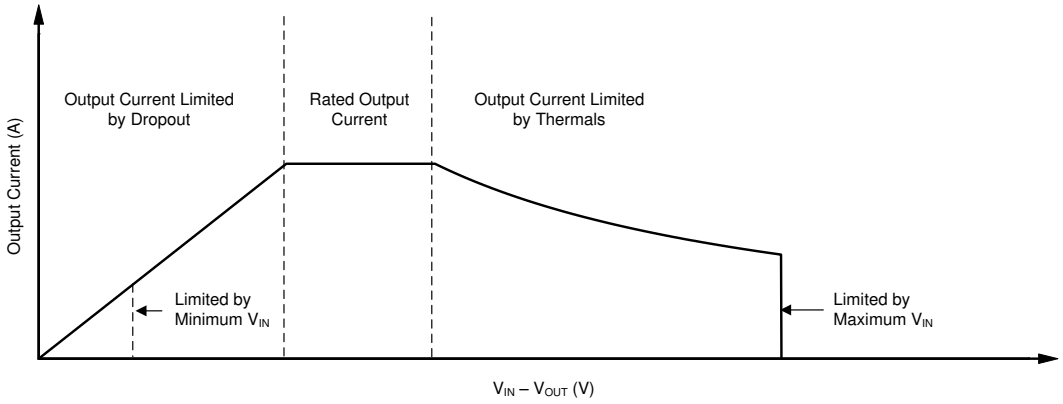


Figure 7-3. Continuous Operation Diagram With Description of Regions

7.2 Typical Application

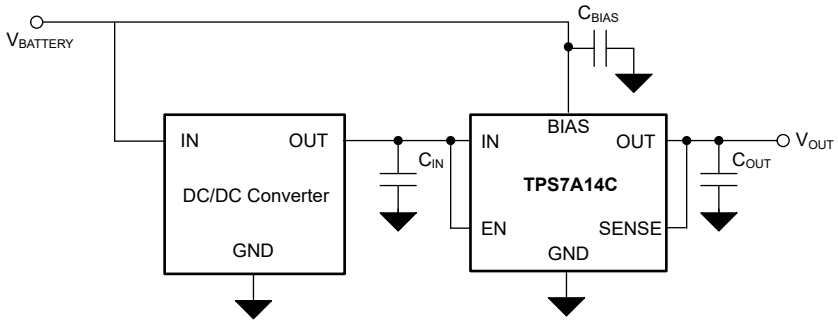


Figure 7-4. High-Efficiency Supply From a Rechargeable Battery

7.2.1 Design Requirements

Table 7-1 lists the parameters for this design example.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	0.95V
V_{BIAS}	2.4V to 5.5V
V_{OUT}	0.8V
I_{OUT}	600mA (typical), 900mA (peak)

7.2.2 Detailed Design Procedure

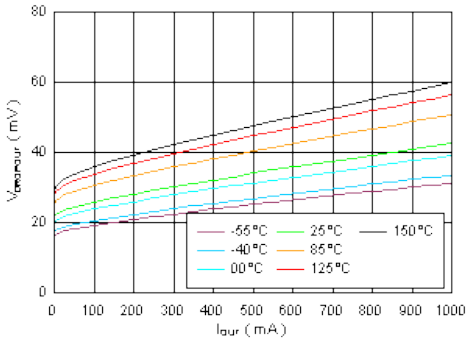
This design example is powered by a rechargeable battery that serves as a building block in many portable applications. Noise-sensitive portable electronics require an efficient, small-size design for the power supply. Using a bias rail in the TPS7A14C allows the main power path of the LDO to operate at a lower input voltage. This feature reduces the voltage drop across the pass transistor and maximizes device efficiency. Because the voltage drop across the pass transistor is potentially so low, the efficiency of the TPS7A14C approximates that of a dc/dc converter. Equation 8 calculates the efficiency for this design.

$$\text{Efficiency} = \eta = P_{OUT} / P_{IN} \times 100\% = (V_{OUT} \times I_{OUT}) / (V_{IN} \times I_{IN} + V_{BIAS} \times I_{BIAS}) \times 100\% \quad (8)$$

Equation 8 reduces to Equation 9 because the design example load current is much greater than the quiescent current of the bias rail.

$$\text{Efficiency} = \eta = (V_{OUT} \times I_{OUT}) / (V_{IN} \times I_{IN}) \times 100\% \quad (9)$$

7.2.3 Application Curve



$V_{BIAS} = V_{OUT(NOM)} + 1.4V$, $V_{EN} = V_{IN}$, $C_{IN} = 4.7\mu F$, $C_{OUT} = 4.7\mu F$, and $C_{BIAS} = 0.47\mu F$

Figure 7-5. V_{IN} Dropout Voltage vs I_{OUT}

7.3 Power Supply Recommendations

This device is designed to operate from a 0.7V to 2.2V input supply voltage range and a 2.2V to 5.5V bias supply voltage range. Verify the input and bias supplies are well regulated and free of spurious noise. To confirm the output voltage is well regulated and dynamic performance is optimum, verify the input and bias supplies satisfy the following equations:

$$V_{OUT(nom)} + V_{DO} \text{ and } V_{BIAS} = V_{OUT(nom)} + V_{DO(BIAS)} \quad (10)$$

7.4 Layout

7.4.1 Layout Guidelines

For correct printed circuit board (PCB) layout, follow these guidelines:

- Place input, output, and bias capacitors as close to the device as possible
- Use copper planes for device connections to optimize thermal performance
- Place thermal vias around the device to distribute heat

7.4.2 Layout Example

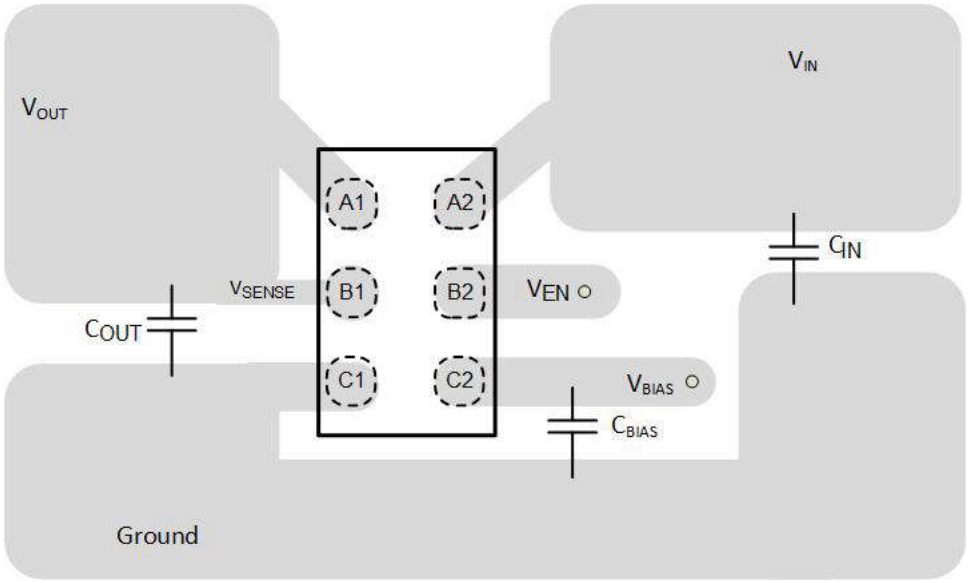


Figure 7-6. Recommended Layout (YBK Package)

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.2 Device Nomenclature

Table 8-1. Available Options

PRODUCT(1) (2)	DESCRIPTION
TPS7A14C**xx(x)(P)yyyz**	**xx(x)** is the nominal output voltage. Two or more digits are used in the ordering number (for example, 09 = 0.9V, 95 = 0.95V, 125 = 1.25V). **P** indicates an active pull down; if there is no P, then the device does not have the active pull-down feature. **yyy** is the package designator. **z** is the package quantity. R indicates reel (12000 pieces for YBK package).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.5V to 2.0V in 25mV increments are available. Contact the factory for details and availability.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-1112 DSBGA Wafer Level Chip Scale Package* application report
- Texas Instruments, *TPS7A14EVM-058 Evaluation Module* user guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

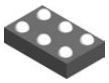
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

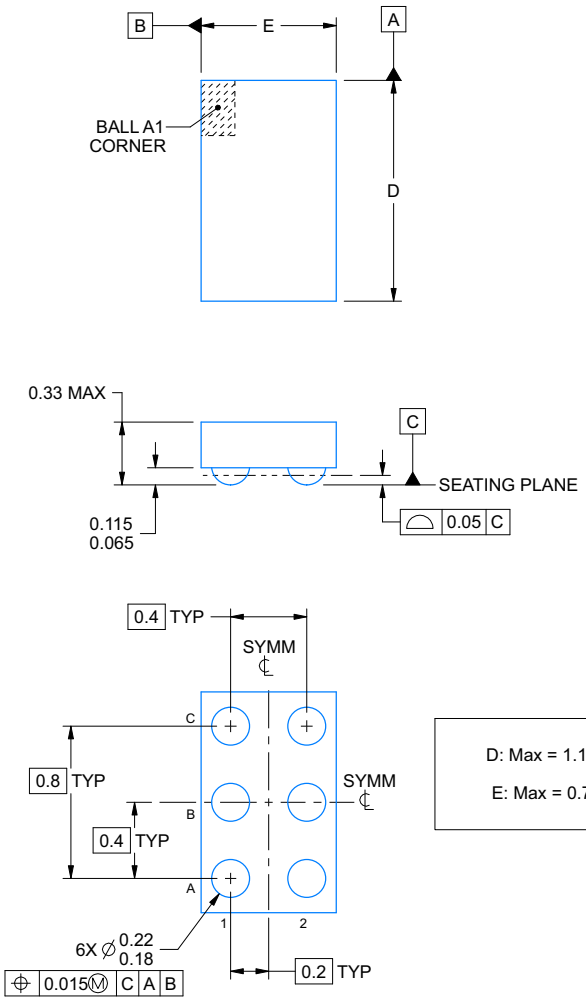


PACKAGE OUTLINE

YBK0006-C02

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

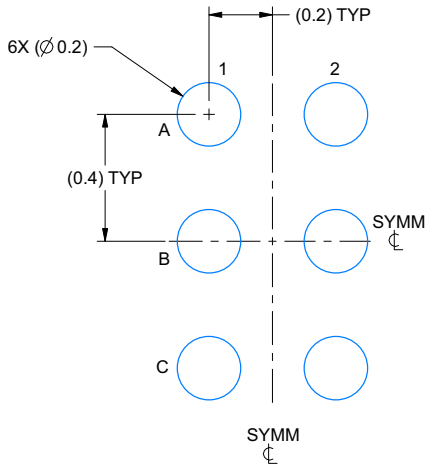
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

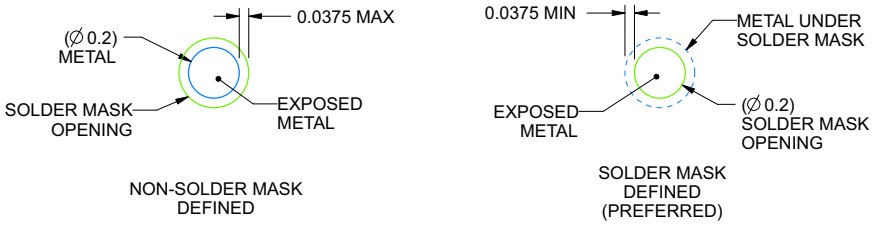
YBK0006-C02

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4228735/A 05/2022

NOTES: (continued)

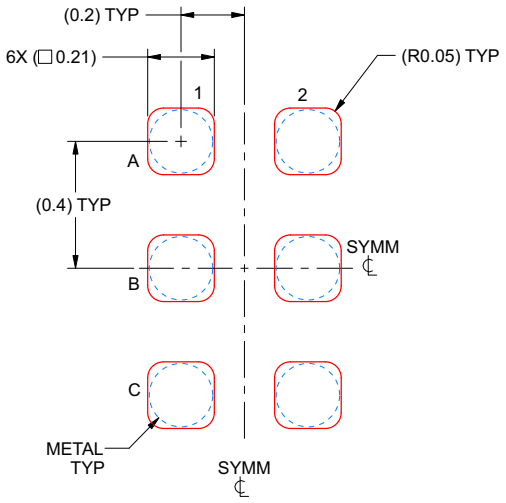
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBK0006-C02

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

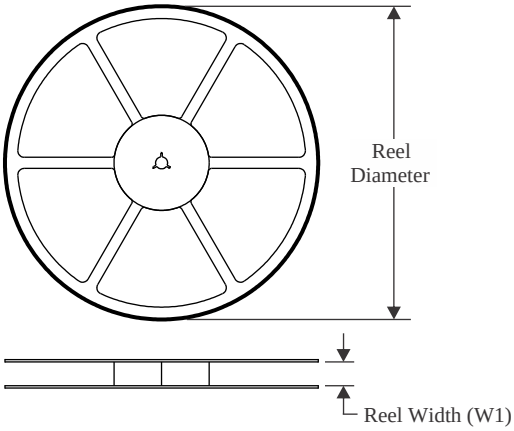
4228735/A 05/2022

NOTES: (continued)

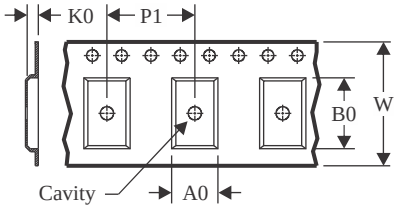
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

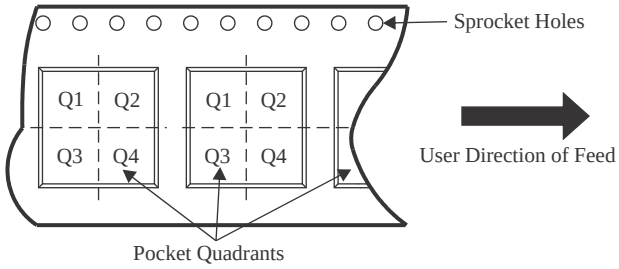


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

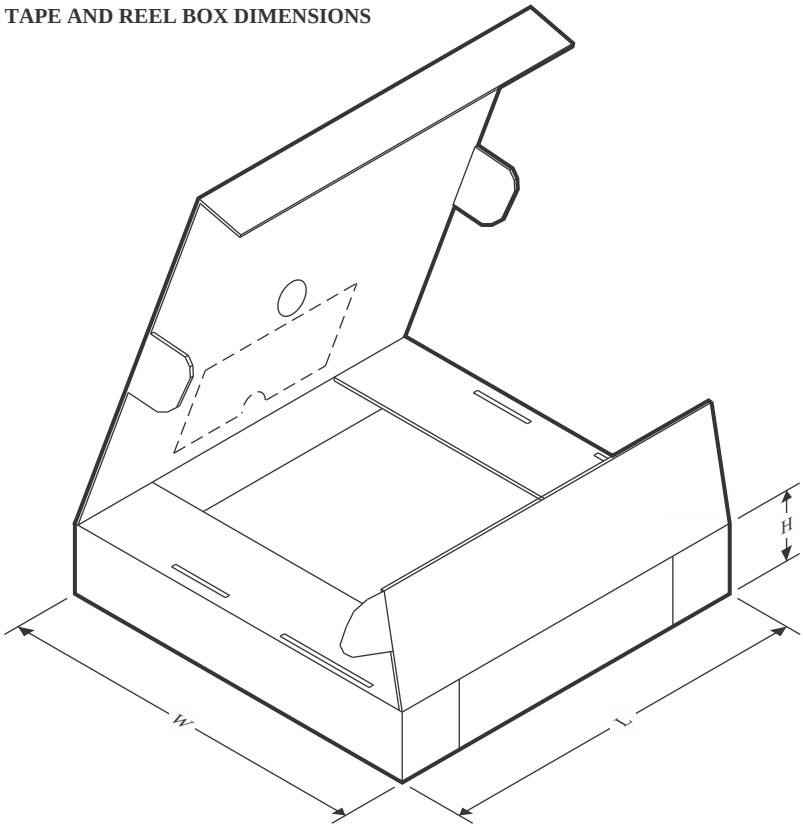
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A14C08PYBKR	DSBGA	YBK	6	12000	180.0	8.4	0.81	1.26	0.36	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A14C08PYBKR	DSBGA	YBK	6	12000	182.0	182.0	20.0

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